Gen2 256Gb TLC 3D NAND Flash

Client Datasheet (Package)

Rev 0.2

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Features

Open NAND Flash Interface (ONFI) 4.0 Compliant					
Triple Level Cell (TLC) Technology					
Organization					
Page Size	16K bytes + 2048 bytes				
Block Size	1152 pages				
Plane Size	1006 blocks				
Device Capacity	256Gb (2 planes/die)				
Performance					
Page Read in SLC	34µs (typ)				
Page Program in SLC	200µs (typ)				
Block Erase in SLC	3.3ms (typ)				
Page Read in TLC	57/74/57µs (typ)				
Page Program in TLC (one-pass)	760µs (typ)				
Block Erase in TLC	9ms (typ)				
Clock Rate	20 ns (SDR, TM5); 5 ns (NV-DDR2, TM8); 2.5 ns (NV-DDR3, TM10)				
Power Consumption					
Page Read Current On V_{CC}	35mA (typ)				
Page Program Current On V_{CC}	32mA (typ)				
Erase Current on V_{CC}	25mA (typ)				
Standby Current on V_{CC}	76µA (typ)				
Standby Current on V_{CCQ}	12µA (typ)				
Operating Voltage Range					
V_{CC}	2.35 ~ 3.6 V				
V_{CCQ}	1.7 ~ 1.95 V/1.14 ~ 1.26 V				
Operating Temperature Range					
Client	0 ~ 70 °C				
Package					
BGA	132-ball/272-ball				
Command Sets					
Reset	Read Status Enhanced	Block Erase	Multi-Plane Operation	Read Status Enhanced II	
Synchronous Reset	Read Parameter Page	Copyback Read	Volume Select	Change Read Column Enhanced	
Reset LUN	Page Read	Copyback Program	ODT Configure	LUN Set Features	Fast Partial Page Read
Hard Reset	Page Program	Program Suspend	ZQ Calibration Short	LUN Get Features	SLC Mode Access
Read ID	Change Write Column	Program Resume	ZQ Calibration Long	Erased Page Check	SLC Mode Abort
Read Unique ID	Change Row Address	Erase Suspend	Set Features	Cache Read	Cache Program
Read Status	Change Read Column	Erase Resume	Get Features		

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Tables

1. Introduction

1.1. General Description

YMTC® 256Gb 3D NAND Flash device is compliant with ONFI 4.0 specifications and able to work in the SDR, NV-DDR2 and NV-DDR3 data interfaces. Commands, addresses and data are all transferred through a multiplexed 8-bit bus.

This 3D NAND flash device can be packaged in BGA and supports a maximum data rate up to 800MB/s.

This NAND flash device adopts the advanced 3D TLC technology from YMTC. The die capacity is up to 256Gb, which makes it an ideal memory solution for mobile and computing applications that require high storage capacities.

1.2. Abbreviation Definitions

Table 1. Abbreviation Sets

Acronym and Abbreviation	Description
SDR	Single data rate.
DDR	Double data rate.
WL	Word line, the smallest addressable unit for read operations.
LUN	Logical unit number, the minimum unit that can independently execute commands and report status. There are one or more LUNs per CE_n.
SR[x]	Status read. SR refers to the status register contained within a particular LUN. SR[x] refers to bit x in the status register for the associated LUN.

1.3. Diagram Legend

Table 2. Waveform Element Sets

Element	Description
	Command
	Address
	Column address in x cycle
	Row address in x cycle
	Data input
	Data output

1.4. Product List

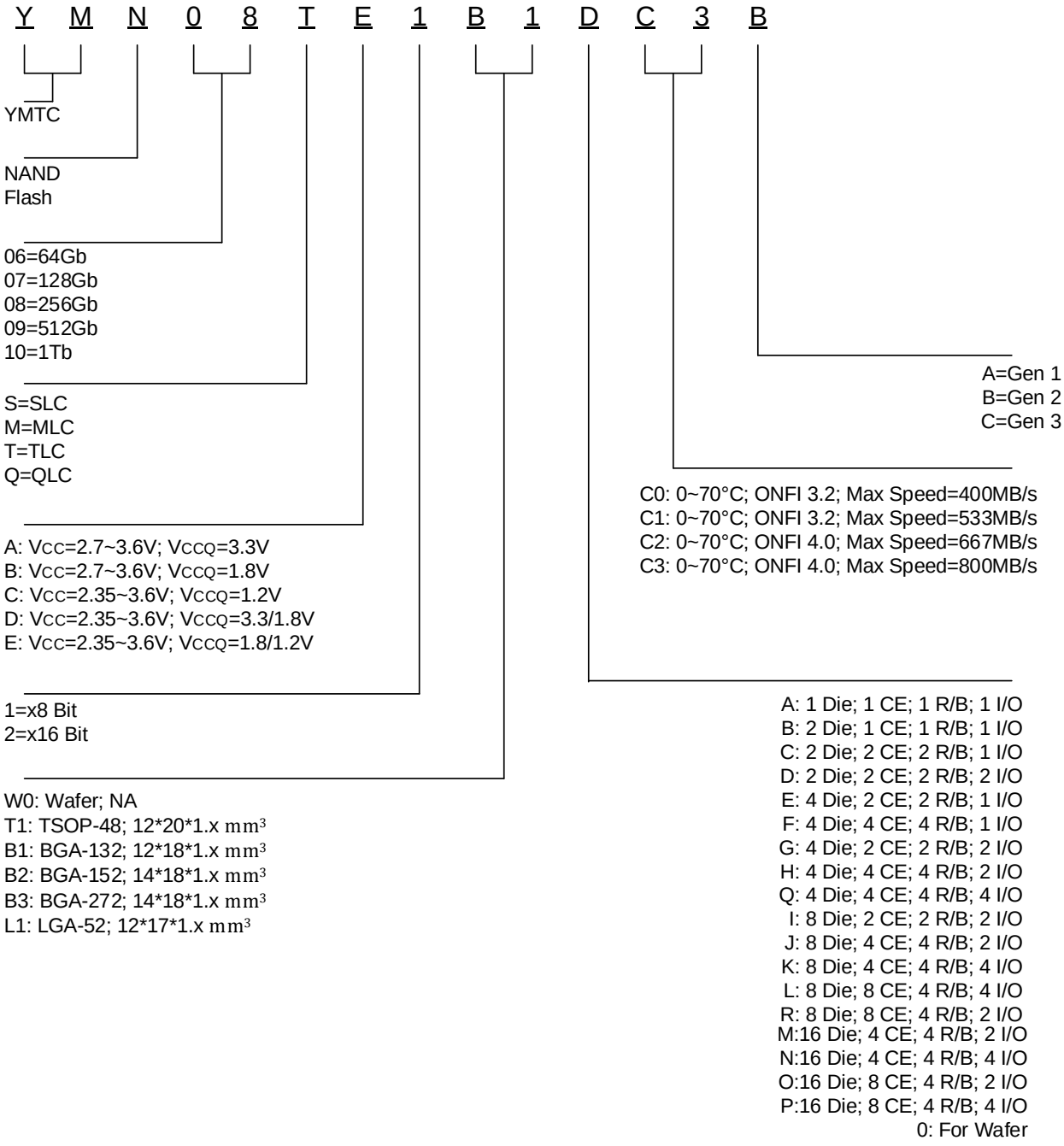
Table 3. Product List

Part Number	Density	V_{CC}	V_{CCQ}	I/O Speed	# of CE & RB & IO	Package	Notes
YMN08TE1W00C3B	256Gbit	2.35~3.6V	1.8V/1.2V	800MB/s	N/A	N/A	
YMN08TE1B1DC3B	64GB (256Gbit x2)	2.35~3.6V	1.8V/1.2V	800MB/s	2CE & 2RB & 2IO	BGA132	
YMN08TE1B1HC3B	128GB (256Gbit x4)	2.35~3.6V	1.8V/1.2V	800MB/s	4CE & 4RB & 2IO	BGA132	
YMN08TE1B1RC3B	256GB (256Gbit x8)	2.35~3.6V	1.8V/1.2V	800MB/s	8CE & 4RB & 2IO	BGA132	
YMN08TE1B3QC3B	128GB (256Gbit x4)	2.35~3.6V	1.8V/1.2V	800MB/s	4CE & 4RB & 4IO	BGA272	
YMN08TE1B3KC3B	256GB (256Gbit x8)	2.35~3.6V	1.8V/1.2V	800MB/s	4CE & 4RB & 4IO	BGA272	
YMN08TE1B3LC3B	256GB (256Gbit x8)	2.35~3.6V	1.8V/1.2V	800MB/s	8CE & 4RB & 4IO	BGA272	
YMN08TE1B3PC3B	512GB (256Gbit x16)	2.35~3.6V	1.8V/1.2V	800MB/s	8CE & 4RB & 4IO	BGA272	

1.5. Part Number

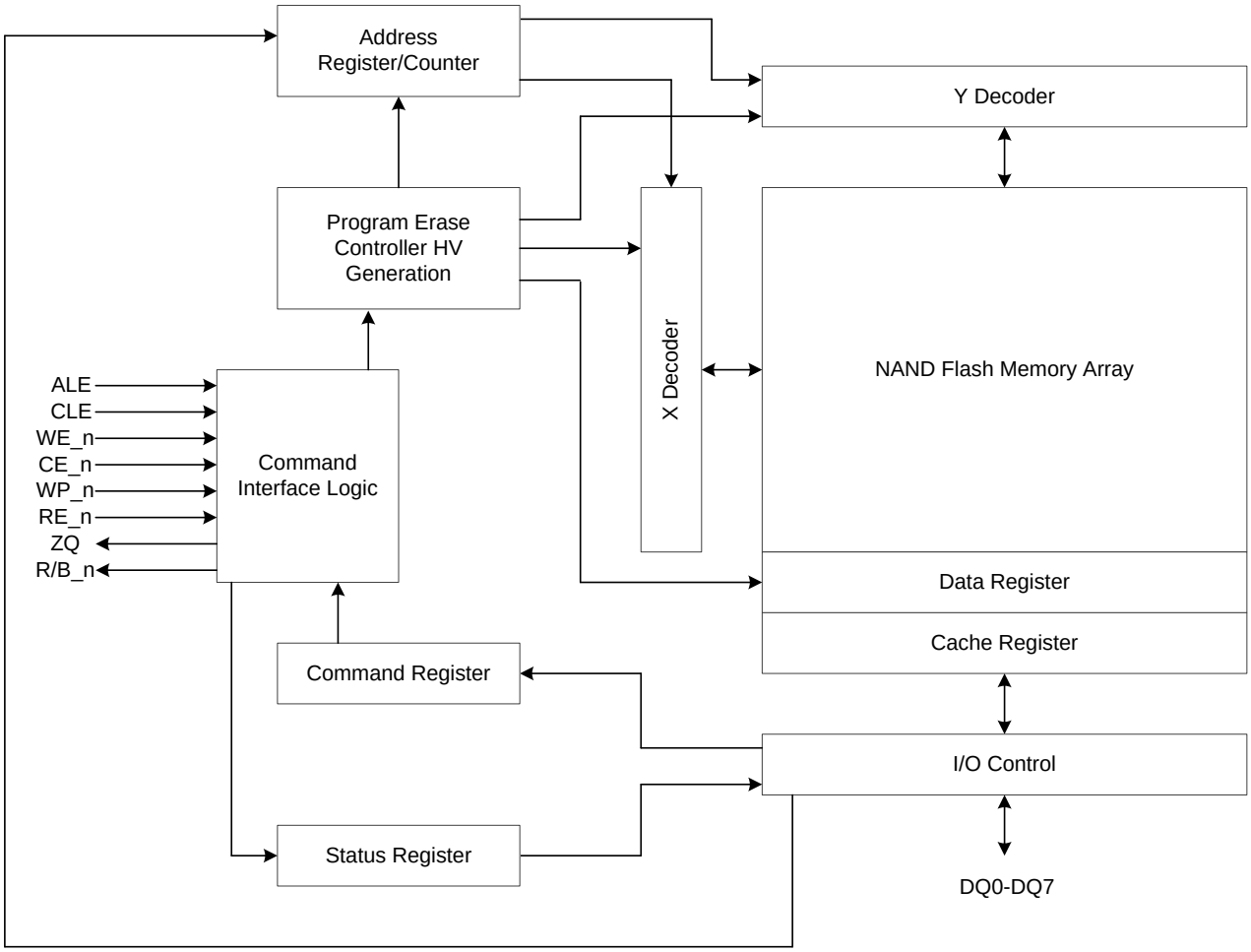
YMTC NAND Flash devices are offered in different configurations and densities. To check part numbers, refer to the figure below. To compare features and specifications by device type, visit www.ymtc.com. Contact technical support for devices not found.

Figure 1. Part Number Information



1.6. Functional Block

Figure 2. Functional Block Diagram



2. Package Information

2.1. Package Types

Figure 3. Pad Assignments of BGA 132 (Top View)

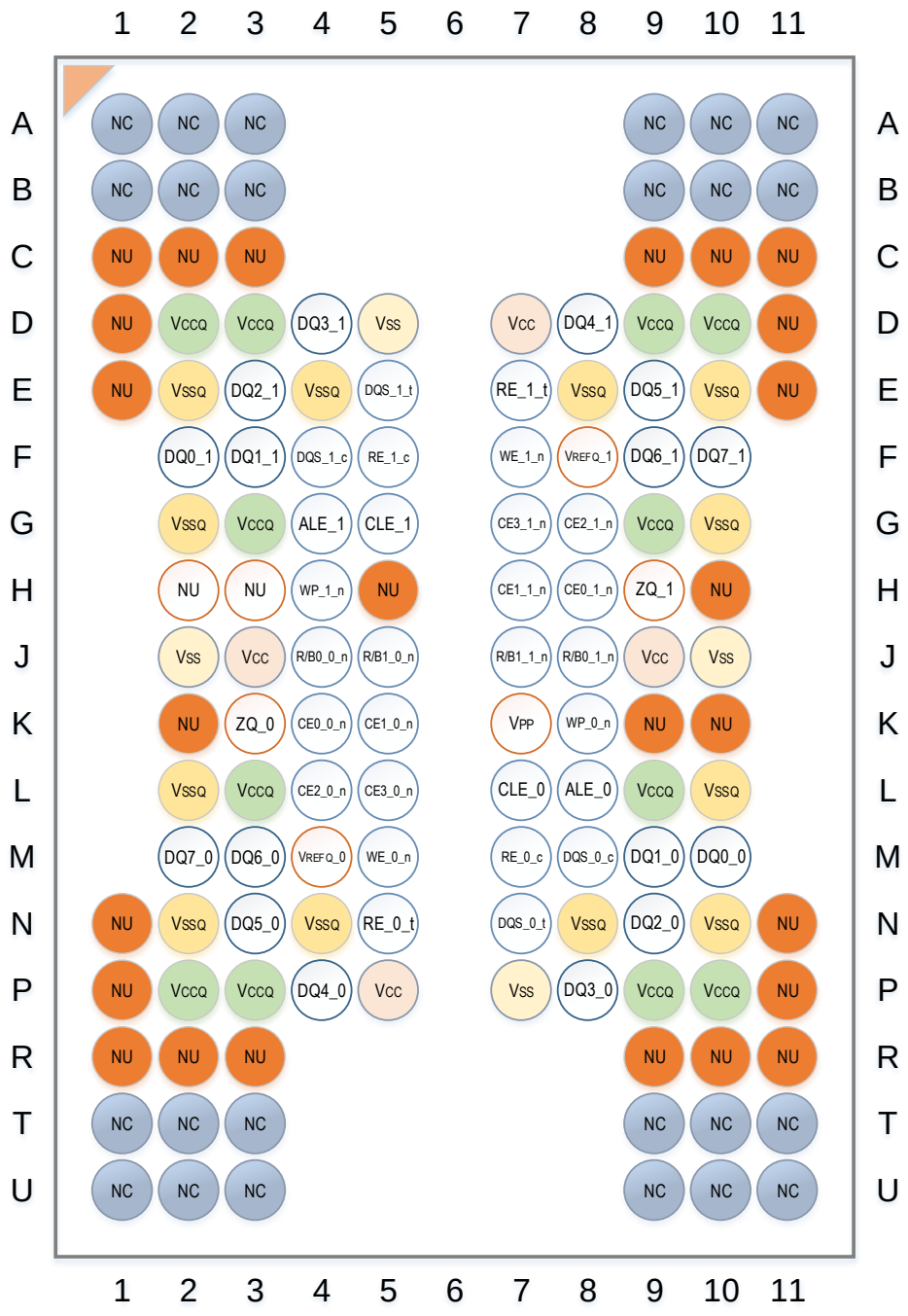
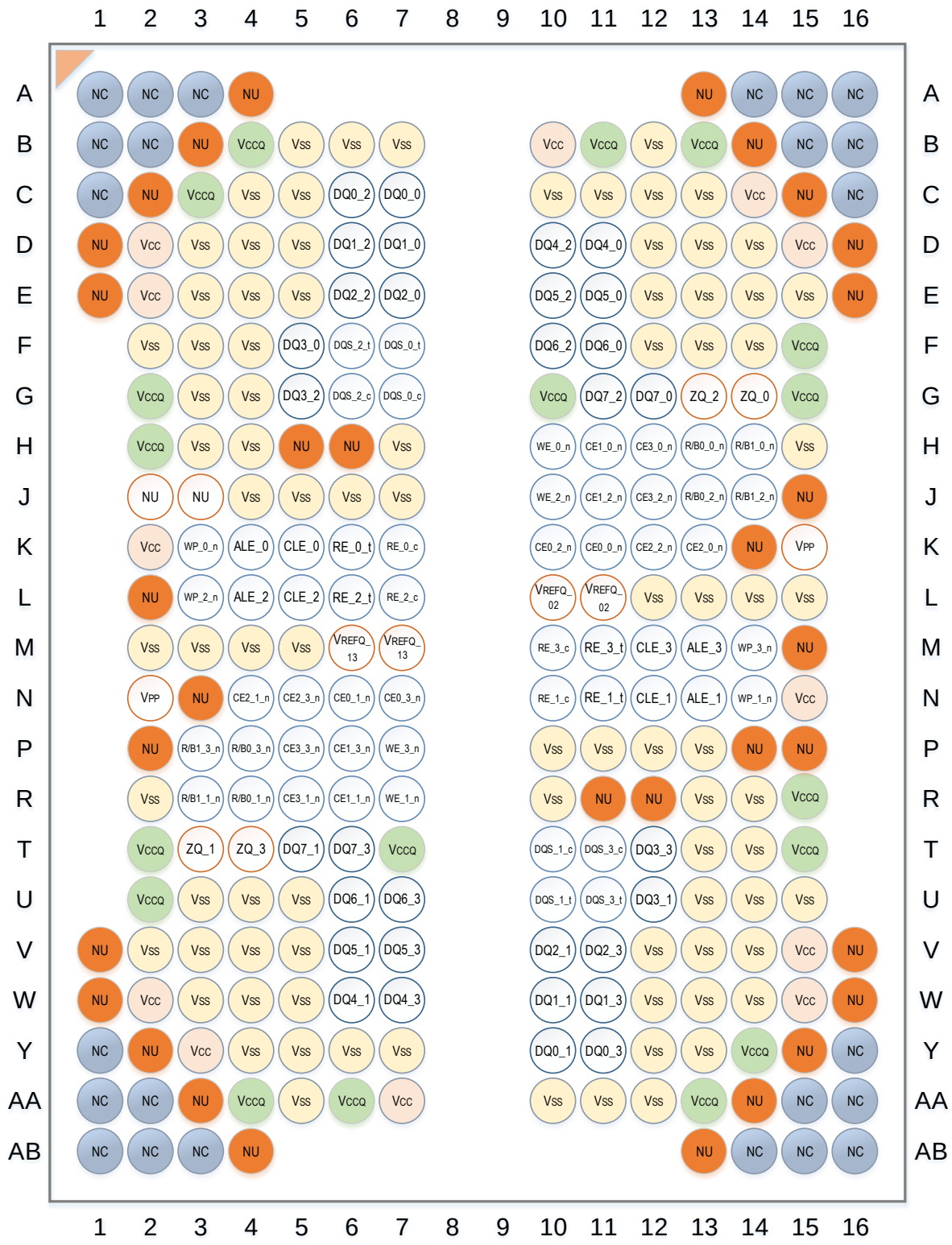


Figure 4. Pad Assignments of BGA 272 (Top View)



2.2. Package Signals

Table 4. BGA132 Signals: DDP/QDP

Signal	DDP (2CE/2RB/2IO)		QDP (4CE/4RB/2IO)			
	Die 0	Die 1	Die 0	Die 1	Die 2	Die 3
CE_n	CE0_0_n	CE0_1_n	CE0_0_n	CE0_1_n	CE1_0_n	CE1_1_n
ALE	ALE_0	ALE_1	ALE_0	ALE_1	ALE_0	ALE_1
CLE	CLE_0	CLE_1	CLE_0	CLE_1	CLE_0	CLE_1
RE_n	RE_0_t	RE_1_t	RE_0_t	RE_1_t	RE_0_t	RE_1_t
RE_c	RE_0_c	RE_1_c	RE_0_c	RE_1_c	RE_0_c	RE_1_c
WE_n	WE_0_n	WE_1_n	WE_0_n	WE_1_n	WE_0_n	WE_1_n
WP_n	WP_0_n	WP_1_n	WP_0_n	WP_1_n	WP_0_n	WP_1_n
R/B_n	R/B0_0_n	R/B0_1_n	R/B0_0_n	R/B0_1_n	R/B1_0_n	R/B1_1_n
DQ[7:0]	DQ[7:0]_0	DQ[7:0]_1	DQ[7:0]_0	DQ[7:0]_1	DQ[7:0]_0	DQ[7:0]_1
DQS	DQS_0_t	DQS_1_t	DQS_0_t	DQS_1_t	DQS_0_t	DQS_1_t
DQS_c	DQS_0_c	DQS_1_c	DQS_0_c	DQS_1_c	DQS_0_c	DQS_1_c
ZQ	ZQ_0	ZQ_1	ZQ_0	ZQ_1	ZQ_0	ZQ_1
V_{REFQ}	V_{REFQ}_0	V_{REFQ}_1	V_{REFQ}_0	V_{REFQ}_1	V_{REFQ}_0	V_{REFQ}_1

Table 5. BGA132 Signals: ODP

Signal	ODP (4CE/4RB/2IO)							
	Die 0	Die 1	Die 2	Die 3	Die 4	Die 5	Die 6	Die 7
CE_n	CE0_0_n	CE0_1_n	CE1_0_n	CE1_1_n	CE0_0_n	CE0_1_n	CE1_0_n	CE1_1_n
ALE	ALE_0	ALE_1	ALE_0	ALE_1	ALE_0	ALE_1	ALE_0	ALE_1
CLE	CLE_0	CLE_1	CLE_0	CLE_1	CLE_0	CLE_1	CLE_0	CLE_1
RE_n	RE_0_t	RE_1_t	RE_0_t	RE_1_t	RE_0_t	RE_1_t	RE_0_t	RE_1_t
RE_c	RE_0_c	RE_1_c	RE_0_c	RE_1_c	RE_0_c	RE_1_c	RE_0_c	RE_1_c
WE_n	WE_0_n	WE_1_n	WE_0_n	WE_1_n	WE_0_n	WE_1_n	WE_0_n	WE_1_n
WP_n	WP_0_n	WP_1_n	WP_0_n	WP_1_n	WP_0_n	WP_1_n	WP_0_n	WP_1_n
R/B_n	R/B0_0_n	R/B0_1_n	R/B1_0_n	R/B1_1_n	R/B0_0_n	R/B0_1_n	R/B1_0_n	R/B1_1_n
DQ[7:0]	DQ[7:0]_0	DQ[7:0]_1	DQ[7:0]_0	DQ[7:0]_1	DQ[7:0]_0	DQ[7:0]_1	DQ[7:0]_0	DQ[7:0]_1
DQS	DQS_0_t	DQS_1_t	DQS_0_t	DQS_1_t	DQS_0_t	DQS_1_t	DQS_0_t	DQS_1_t
DQS_c	DQS_0_c	DQS_1_c	DQS_0_c	DQS_1_c	DQS_0_c	DQS_1_c	DQS_0_c	DQS_1_c
ZQ	ZQ_0	ZQ_1	ZQ_0	ZQ_1	ZQ_0	ZQ_1	ZQ_0	ZQ_1
V_{REFQ}	V_{REFQ}_0	V_{REFQ}_1	V_{REFQ}_0	V_{REFQ}_1	V_{REFQ}_0	V_{REFQ}_1	V_{REFQ}_0	V_{REFQ}_1

Table 6. BGA132 Signals: ODP

Signal	ODP (8CE/4RB/2IO)							
	Die 0	Die 1	Die 2	Die 3	Die 4	Die 5	Die 6	Die 7
CE_n	CE0_0_n	CE0_1_n	CE1_0_n	CE1_1_n	CE2_0_n	CE2_1_n	CE3_0_n	CE3_1_n
ALE	ALE_0	ALE_1	ALE_0	ALE_1	ALE_0	ALE_1	ALE_0	ALE_1
CLE	CLE_0	CLE_1	CLE_0	CLE_1	CLE_0	CLE_1	CLE_0	CLE_1
RE_n	RE_0_t	RE_1_t	RE_0_t	RE_1_t	RE_0_t	RE_1_t	RE_0_t	RE_1_t
RE_c	RE_0_c	RE_1_c	RE_0_c	RE_1_c	RE_0_c	RE_1_c	RE_0_c	RE_1_c
WE_n	WE_0_n	WE_1_n	WE_0_n	WE_1_n	WE_0_n	WE_1_n	WE_0_n	WE_1_n
WP_n	WP_0_n	WP_1_n	WP_0_n	WP_1_n	WP_0_n	WP_1_n	WP_0_n	WP_1_n
R/B_n	R/B0_0_n	R/B0_1_n	R/B1_0_n	R/B1_1_n	R/B0_0_n	R/B0_1_n	R/B1_0_n	R/B1_1_n
DQ[7:0]	DQ[7:0]_0	DQ[7:0]_1	DQ[7:0]_0	DQ[7:0]_1	DQ[7:0]_0	DQ[7:0]_1	DQ[7:0]_0	DQ[7:0]_1
DQS	DQS_0_t	DQS_1_t	DQS_0_t	DQS_1_t	DQS_0_t	DQS_1_t	DQS_0_t	DQS_1_t
DQS_c	DQS_0_c	DQS_1_c	DQS_0_c	DQS_1_c	DQS_0_c	DQS_1_c	DQS_0_c	DQS_1_c
ZQ	ZQ_0	ZQ_1	ZQ_0	ZQ_1	ZQ_0	ZQ_1	ZQ_0	ZQ_1
V_{REFQ}	V_{REFQ}_0	V_{REFQ}_1	V_{REFQ}_0	V_{REFQ}_1	V_{REFQ}_0	V_{REFQ}_1	V_{REFQ}_0	V_{REFQ}_1

Table 7. BGA272 Signals: QDP

Signal	QDP (4CE/4RB/4IO)			
	Die 0	Die 1	Die 2	Die 3
CE_n	CE0_0_n	CE0_1_n	CE0_2_n	CE0_3_n
ALE	ALE_0	ALE_1	ALE_2	ALE_3
CLE	CLE_0	CLE_1	CLE_2	CLE_3
RE_n	RE_0_t	RE_1_t	RE_2_t	RE_3_t
RE_c	RE_0_c	RE_1_c	RE_2_c	RE_3_c
WE_n	WE_0_n	WE_1_n	WE_2_n	WE_3_n
WP_n	WP_0_n	WP_1_n	WP_2_n	WP_3_n
R/B_n	R/B0_0_n	R/B0_1_n	R/B0_2_n	R/B0_3_n
DQ[7:0]	DQ[7:0]_0	DQ[7:0]_1	DQ[7:0]_2	DQ[7:0]_3
DQS	DQS_0_t	DQS_1_t	DQS_2_t	DQS_3_t
DQS_c	DQS_0_c	DQS_1_c	DQS_2_c	DQS_3_c
ZQ	ZQ_0	ZQ_1	ZQ_2	ZQ_3
V_{REFQ}	V_{REFQ}_02	V_{REFQ}_13	V_{REFQ}_02	V_{REFQ}_13

Table 8. BGA272 Signals: ODP

Signal	ODP (4CE/4RB/4IO)							
	Die 0	Die 1	Die 2	Die 3	Die 4	Die 5	Die 6	Die 7
CE_n	CE0_0_n	CE0_1_n	CE0_2_n	CE0_3_n	CE0_0_n	CE0_1_n	CE0_2_n	CE0_3_n
ALE	ALE_0	ALE_1	ALE_2	ALE_3	ALE_0	ALE_1	ALE_2	ALE_3
CLE	CLE_0	CLE_1	CLE_2	CLE_3	CLE_0	CLE_1	CLE_2	CLE_3
RE_n	RE_0_t	RE_1_t	RE_2_t	RE_3_t	RE_0_t	RE_1_t	RE_2_t	RE_3_t
RE_c	RE_0_c	RE_1_c	RE_2_c	RE_3_c	RE_0_c	RE_1_c	RE_2_c	RE_3_c
WE_n	WE_0_n	WE_1_n	WE_2_n	WE_3_n	WE_0_n	WE_1_n	WE_2_n	WE_3_n
WP_n	WP_0_n	WP_1_n	WP_2_n	WP_3_n	WP_0_n	WP_1_n	WP_2_n	WP_3_n
R/B_n	R/B0_0_n	R/B0_1_n	R/B0_2_n	R/B0_3_n	R/B0_0_n	R/B0_1_n	R/B0_2_n	R/B0_3_n
DQ[7:0]	DQ[7:0]_0	DQ[7:0]_1	DQ[7:0]_2	DQ[7:0]_3	DQ[7:0]_0	DQ[7:0]_1	DQ[7:0]_2	DQ[7:0]_3
DQS	DQS_0_t	DQS_1_t	DQS_2_t	DQS_3_t	DQS_0_t	DQS_1_t	DQS_2_t	DQS_3_t
DQS_c	DQS_0_c	DQS_1_c	DQS_2_c	DQS_3_c	DQS_0_c	DQS_1_c	DQS_2_c	DQS_3_c
ZQ	ZQ_0	ZQ_1	ZQ_2	ZQ_3	ZQ_0	ZQ_1	ZQ_2	ZQ_3
V_{REFQ}	V_{REFQ}_02	V_{REFQ}_13	V_{REFQ}_02	V_{REFQ}_13	V_{REFQ}_02	V_{REFQ}_13	V_{REFQ}_02	V_{REFQ}_13

Table 9. BGA272 Signals: ODP

Signal	ODP (8CE/4RB/4IO)							
	Die 0	Die 1	Die 2	Die 3	Die 4	Die 5	Die 6	Die 7
CE_n	CE0_0_n	CE0_1_n	CE0_2_n	CE0_3_n	CE1_0_n	CE1_1_n	CE1_2_n	CE1_3_n
ALE	ALE_0	ALE_1	ALE_2	ALE_3	ALE_0	ALE_1	ALE_2	ALE_3
CLE	CLE_0	CLE_1	CLE_2	CLE_3	CLE_0	CLE_1	CLE_2	CLE_3
RE_n	RE_0_t	RE_1_t	RE_2_t	RE_3_t	RE_0_t	RE_1_t	RE_2_t	RE_3_t
RE_c	RE_0_c	RE_1_c	RE_2_c	RE_3_c	RE_0_c	RE_1_c	RE_2_c	RE_3_c
WE_n	WE_0_n	WE_1_n	WE_2_n	WE_3_n	WE_0_n	WE_1_n	WE_2_n	WE_3_n
WP_n	WP_0_n	WP_1_n	WP_2_n	WP_3_n	WP_0_n	WP_1_n	WP_2_n	WP_3_n
R/B_n	R/B0_0_n	R/B0_1_n	R/B0_2_n	R/B0_3_n	R/B0_0_n	R/B0_1_n	R/B0_2_n	R/B0_3_n
DQ[7:0]	DQ[7:0]_0	DQ[7:0]_1	DQ[7:0]_2	DQ[7:0]_3	DQ[7:0]_0	DQ[7:0]_1	DQ[7:0]_2	DQ[7:0]_3
DQS	DQS_0_t	DQS_1_t	DQS_2_t	DQS_3_t	DQS_0_t	DQS_1_t	DQS_2_t	DQS_3_t
DQS_c	DQS_0_c	DQS_1_c	DQS_2_c	DQS_3_c	DQS_0_c	DQS_1_c	DQS_2_c	DQS_3_c
ZQ	ZQ_0	ZQ_1	ZQ_2	ZQ_3	ZQ_0	ZQ_1	ZQ_2	ZQ_3
V_{REFQ}	V_{REFQ}_02	V_{REFQ}_13	V_{REFQ}_02	V_{REFQ}_13	V_{REFQ}_02	V_{REFQ}_13	V_{REFQ}_02	V_{REFQ}_13

Table 10. BGA272 Signals: HDP

Signal	HDP (8CE/4RB/4IO)							
	Die 0	Die 1	Die 2	Die 3	Die 4	Die 5	Die 6	Die 7
CE_n	CE0_0_n	CE0_1_n	CE0_2_n	CE0_3_n	CE1_0_n	CE1_1_n	CE1_2_n	CE1_3_n
ALE	ALE_0	ALE_1	ALE_2	ALE_3	ALE_0	ALE_1	ALE_2	ALE_3
CLE	CLE_0	CLE_1	CLE_2	CLE_3	CLE_0	CLE_1	CLE_2	CLE_3
RE_n	RE_0_t	RE_1_t	RE_2_t	RE_3_t	RE_0_t	RE_1_t	RE_2_t	RE_3_t
RE_c	RE_0_c	RE_1_c	RE_2_c	RE_3_c	RE_0_c	RE_1_c	RE_2_c	RE_3_c
WE_n	WE_0_n	WE_1_n	WE_2_n	WE_3_n	WE_0_n	WE_1_n	WE_2_n	WE_3_n
WP_n	WP_0_n	WP_1_n	WP_2_n	WP_3_n	WP_0_n	WP_1_n	WP_2_n	WP_3_n
R/B_n	R/B0_0_n	R/B0_1_n	R/B0_2_n	R/B0_3_n	R/B0_0_n	R/B0_1_n	R/B0_2_n	R/B0_3_n
DQ[7:0]	DQ[7:0]_0	DQ[7:0]_1	DQ[7:0]_2	DQ[7:0]_3	DQ[7:0]_0	DQ[7:0]_1	DQ[7:0]_2	DQ[7:0]_3
DQS	DQS_0_t	DQS_1_t	DQS_2_t	DQS_3_t	DQS_0_t	DQS_1_t	DQS_2_t	DQS_3_t
DQS_c	DQS_0_c	DQS_1_c	DQS_2_c	DQS_3_c	DQS_0_c	DQS_1_c	DQS_2_c	DQS_3_c
ZQ	ZQ_0	ZQ_1	ZQ_2	ZQ_3	ZQ_0	ZQ_1	ZQ_2	ZQ_3
V_{REFQ}	V_{REFQ}_02	V_{REFQ}_13	V_{REFQ}_02	V_{REFQ}_13	V_{REFQ}_02	V_{REFQ}_13	V_{REFQ}_02	V_{REFQ}_13

Signal	HDP (8CE/4RB/4IO)							
	Die 8	Die 9	Die 10	Die 11	Die 12	Die 13	Die 14	Die 15
CE_n	CE0_0_n	CE0_1_n	CE0_2_n	CE0_3_n	CE1_0_n	CE1_1_n	CE1_2_n	CE1_3_n
ALE	ALE_0	ALE_1	ALE_2	ALE_3	ALE_0	ALE_1	ALE_2	ALE_3
CLE	CLE_0	CLE_1	CLE_2	CLE_3	CLE_0	CLE_1	CLE_2	CLE_3
RE_n	RE_0_t	RE_1_t	RE_2_t	RE_3_t	RE_0_t	RE_1_t	RE_2_t	RE_3_t
RE_c	RE_0_c	RE_1_c	RE_2_c	RE_3_c	RE_0_c	RE_1_c	RE_2_c	RE_3_c
WE_n	WE_0_n	WE_1_n	WE_2_n	WE_3_n	WE_0_n	WE_1_n	WE_2_n	WE_3_n
WP_n	WP_0_n	WP_1_n	WP_2_n	WP_3_n	WP_0_n	WP_1_n	WP_2_n	WP_3_n
R/B_n	R/B0_0_n	R/B0_1_n	R/B0_2_n	R/B0_3_n	R/B0_0_n	R/B0_1_n	R/B0_2_n	R/B0_3_n
DQ[7:0]	DQ[7:0]_0	DQ[7:0]_1	DQ[7:0]_2	DQ[7:0]_3	DQ[7:0]_0	DQ[7:0]_1	DQ[7:0]_2	DQ[7:0]_3
DQS	DQS_0_t	DQS_1_t	DQS_2_t	DQS_3_t	DQS_0_t	DQS_1_t	DQS_2_t	DQS_3_t
DQS_c	DQS_0_c	DQS_1_c	DQS_2_c	DQS_3_c	DQS_0_c	DQS_1_c	DQS_2_c	DQS_3_c
ZQ	ZQ_0	ZQ_1	ZQ_2	ZQ_3	ZQ_0	ZQ_1	ZQ_2	ZQ_3
V_{REFQ}	V_{REFQ}_02	V_{REFQ}_13	V_{REFQ}_02	V_{REFQ}_13	V_{REFQ}_02	V_{REFQ}_13	V_{REFQ}_02	V_{REFQ}_13

2.3. Package Dimensions

Figure 5. BGA 132 Dimensions (Unit: mm)

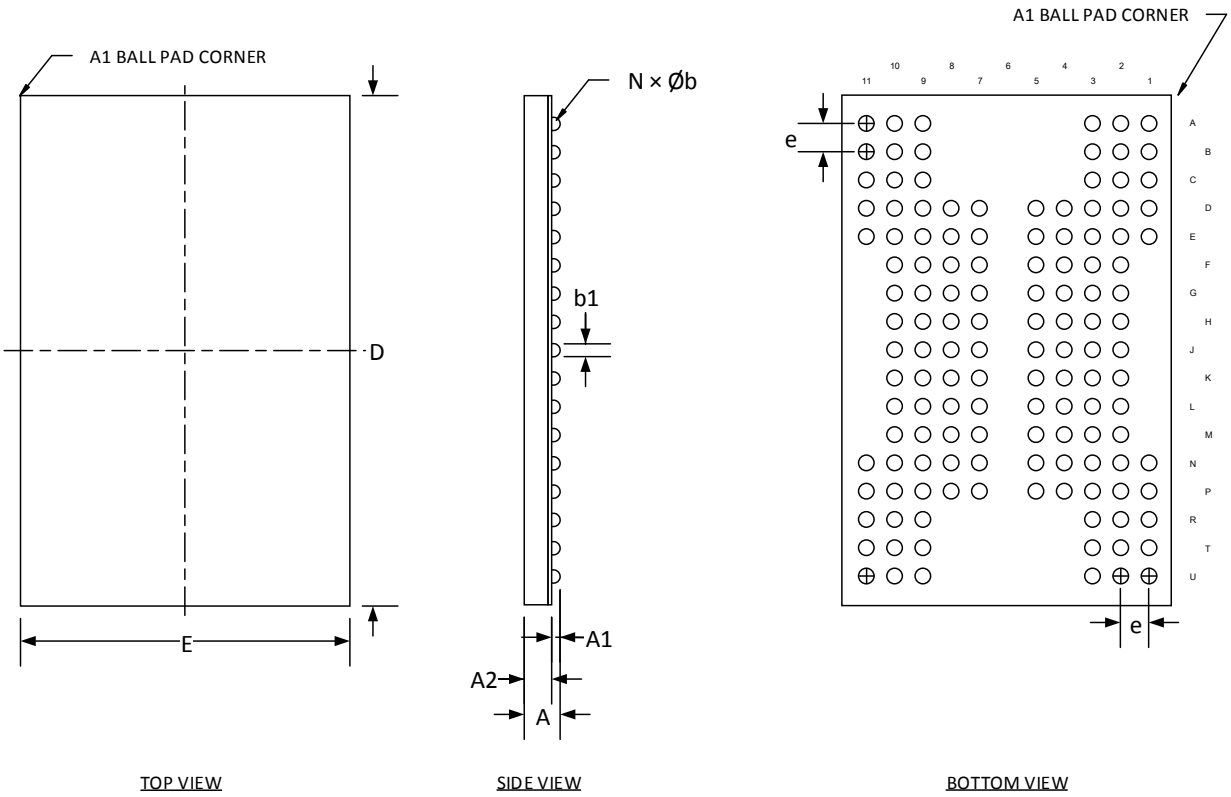


Table 11. BGA 132 Dimensions (Unit: mm)

Symbol	Dimension (Unit: mm)		
	MIN	NOM	MAX
N	132		
D	17.90	18.00	18.10
E	11.90	12.00	12.10
A	-	-	1.20 (DDP/QDP) 1.35 (ODP)
A1	0.25		
A2			0.95 (DDP/QDP) 1.1 (ODP)
B	-	0.47	-
b1	-	0.55	-
E	1.00 BASIC		

Figure 6. BGA 272 Dimensions (Unit: mm)

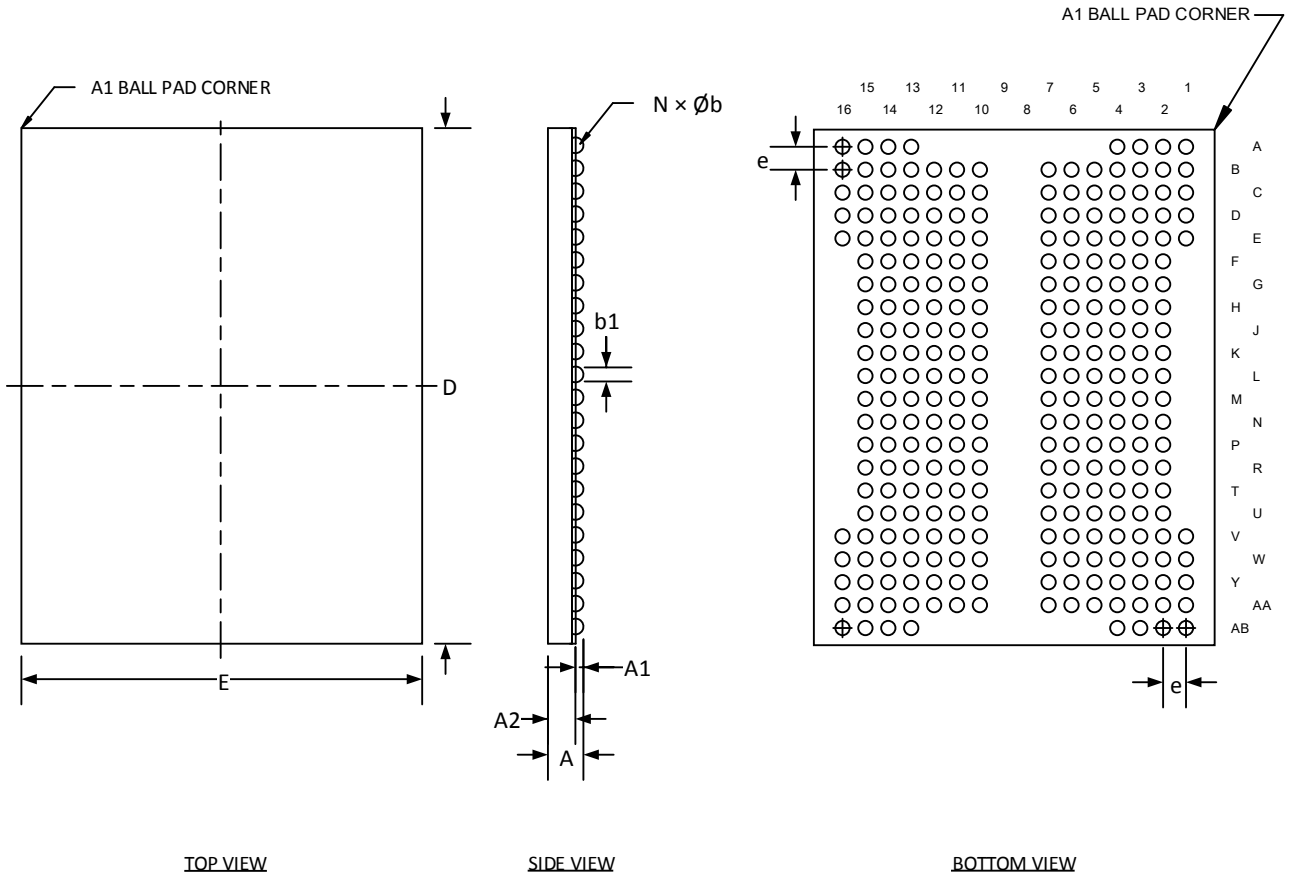


Table 12. BGA 272 Dimensions (Unit: mm)

Symbol	Dimension (Unit: mm)		
	MIN	NOM	MAX
N	272		
D	17.90	18.00	18.10
E	13.90	14.00	14.10
A	-	-	1.20 (QDP) 1.35 (ODP/HDP)
A1	0.25		
A2			0.95 (QDP) 1.1 (ODP/HDP)
B	-	0.47	-
b1	-	0.55	-
E	0.8 BASIC		

2.4. Signal Description

Table 13. Signal Description (SDR)

Signal	Type	Description
CE_n	Input	**Chip Enable** The CE_n signal controls device selection. When CE_n is low, the device is selected. When CE_n is high and the device is in ready state, the device goes to standby state. If the device is in busy state, CE_n High is ignored.
ALE	Input	**Address Latch Enable** The ALE signal controls the activating path for address to internal address registers. Address is latched at the rising edge of WE_n with ALE High.
CLE	Input	**Command Latch Enable** The CLE signal controls the activating path for command to internal command registers. Command is latched at the rising edge of WE_n with CLE High.
RE_n	Input	**Read Enable** The RE_n signal controls series data out from device to host when the device is active. Data is output at the falling edge of RE_n.
WE_n	Input	**Write Enable** The WE_n signal controls the latching of commands, addresses and data input at the rising edge of WE_n.
WP_n	Input	**Write Protect** The WP_n signal disables program and erase operations when it is low. This could be used to prevent inadvertent program and erase operations during power transitions.
R/B_n	Output	**Ready/Busy** The R/B_n signal indicates the device status. When low, it indicates that one or more operations are in progress, for example, program or erase operation. This signal is an open drain output and requires an external pull-up.
DQ[7:0]	Input/Output	**Data Inputs/Outputs** These DQs are bidirectional signals which transfer commands, addresses and data to device, and outputs data during read operations. When the device is deselected or when output buffer is disabled, DQ pins float to High-Z.
ZQ	-	**Reference Pin for ZQ Calibration** The ZQ signal is used on ZQ calibration and shall be connected to Vss through R_{ZQ} resistor.
V_{CC}	Supply	**Core Power Supply** The V_{CC} signal is the power supply to the device.
V_{CCQ}	Supply	**Input/Output Power Supply** The V_{CCQ} signal is the power supply for input/output signals.

Signal	Type	Description
V_{SS}	Supply	**Core Ground** The V_{SS} signal is the power supply ground.
V_{SSQ}	Supply	**Input/Output Ground** The V_{SSQ} signal is the power supply ground for input/output signals.
V_{PP}	Supply	**High Voltage Power** The V_{PP} signal is an optional external high voltage power supply to the device. It may be used to enhance program and erase operations.
NC	-	**No Connection** It indicates that this pin has no internal connection and can be used as a support for external wiring without disturbing the function of the device.
NU	-	**No Use** It indicates that this pin must be left unconnected.

Table 14. Signal Description (NV-DDR2/NV-DDR3)

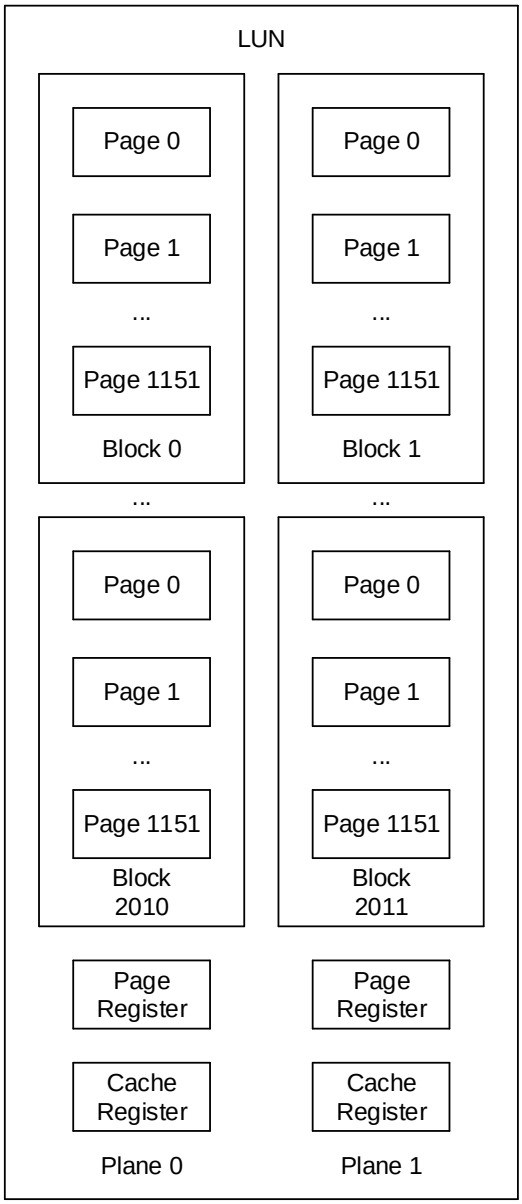
Signal	Type	Description
CE_n	Input	**Chip Enable** The CE_n signal controls device selection. When CE_n is low, the device is selected. When CE_n is high and the device is in ready state, the device goes to standby state. If the device is in busy state, CE_n High is ignored.
ALE	Input	**Address Latch Enable** The ALE signal controls the activating path for address to internal address registers. Address is latched at the rising edge of WE_n with ALE High.
CLE	Input	**Command Latch Enable** The CLE signal controls the activating path for command to internal command registers. Command is latched at the rising edge of WE_n with CLE High.
RE_n (RE_t)	Input	**Read Enable** The RE_n (RE_t) signal controls series data out from device to host when the device is active. Data is output at the both rising and falling edge of RE_n (RE_t).
RE_c	Input	**Read Enable Complement** The RE_c signal is the complementary signal to RE_t, used in differential interface.
WE_n	Input	**Write Enable** The WE_n signal controls the latching of commands and addresses at the rising edge of WE_n.
WP_n	Input	**Write Protect** The WP_n signal disables program and erase operations when it is low. This could be used to prevent inadvertent program and erase operations during power transitions.
R/B_n	Output	**Ready/Busy** The R/B_n signal indicates the device status. When low, it indicates that one or more operations are in progress, for example, program or erase operation. This signal is an open drain output and requires an external pull-up.
DQ[7:0]	Input/Output	**Data Inputs/Outputs** These DQs are bidirectional signals which transfer commands, addresses and data to device, and outputs data during read operations. When the device is deselected or when output buffer is disabled, DQ pins float to High-Z.
DQS (DQS_t)	Input/Output	**Data Strobe** The DQS (DQS_t) signal indicates input/output data valid window. It is edge-aligned with data read and center-aligned with data written.
DQS_c	Input/Output	**Data Strobe Complement** The DQS_c signal is the complementary signal to DQS_t, used in differential interface.
ZQ	-	**Reference Pin for ZQ Calibration** The ZQ signal is used on ZQ calibration and shall be connected to Vss through R_{ZQ} resistor.

Signal	Type	Description
V_{CC}	Supply	**Core Power Supply** The V_{CC} signal is the power supply to the device.
V_{CCQ}	Supply	**Input/Output Power Supply** The V_{CCQ} signal is the power supply for input/output signals.
V_{SS}	Supply	**Core Ground** The V_{SS} signal is the power supply ground.
V_{SSQ}	Supply	**Input/Output Ground** The V_{SSQ} signal is the power supply ground for input/output signals.
V_{PP}	Supply	**High Power Supply** The V_{PP} signal is an optional external high voltage power supply to the device. It may be used to enhance program and erase operations.
V_{REFQ}	Supply	**Input/Output Reference Voltage** The V_{REFQ} signal is used as an external voltage reference for input/output signals.
NC	-	**No Connection** It indicates that this pin has no internal connection and can be used as a support for external wiring without disturbing the function of the device.
NU	-	**No Use** It indicates that this pin must be left unconnected.

3. Device Organization

3.1. Memory Organization

Figure 7. Logical Memory Organization



1 Page = (16K + 2048) bytes

1 Block = 1152 pages

1 Plane = 1006 blocks

1 LUN = 2 planes

3.2. Addressing

3.2.1. Memory Access Addressing

Two address types are used: the column address and the row address. The column address is used to access bytes within a page, i.e. the column address is the byte offset into a page. The least significant bit (LSB) of the column address shall always be zero for a DDR interface, i.e. an even number of bytes are always transferred. The row address is used to address pages, blocks and LUNs. When both the column and row addresses are required to be issued, the column address is always issued in the first one or more 8-bit address cycles while the row addresses is issued in the following one or more 8-bit address cycles. There are some functions that may require only row addresses, such as Erase. In this case, the column addresses are not issued. For both column and row addresses, the first address cycle always contains the least significant address bits and the last address cycle always contains the most significant address bits (MSB). If there are bits in the most significant cycles of the column and row addresses that are not used, they should be cleared to zero. The row address structure is shown in the figure below with the least significant row address bit to the right and the most significant row address bit to the left.

Figure 8. Row and Column Address Layout

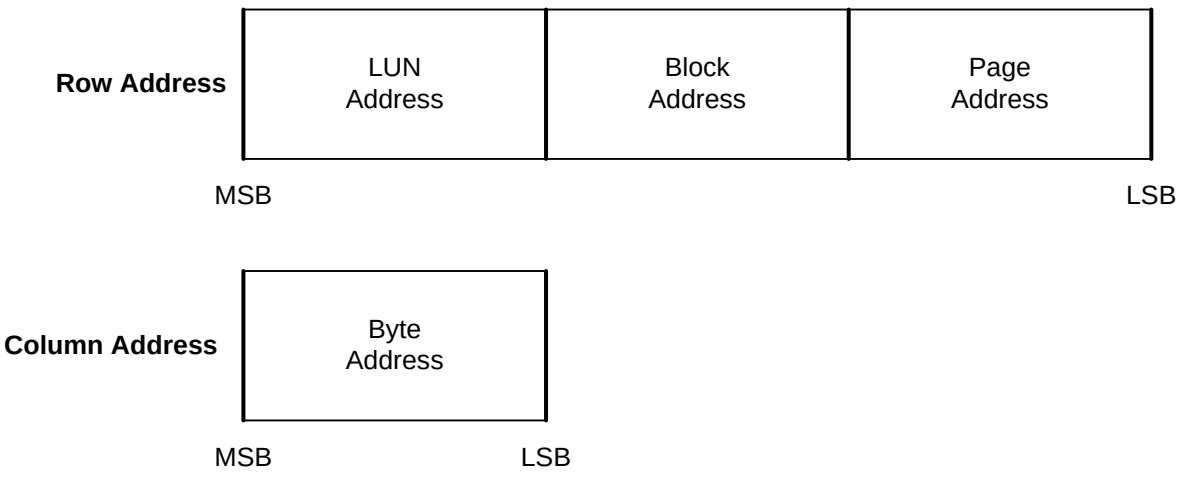


Table 15. TLC Addressing for DDP/QDP/ODP/HDP (6 Address Cycles Required)

Cycles	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	CA14	CA13	CA12	CA11	CA10	CA9	CA8
Third	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA4	BA3	BA2	BA1	BA0	PA10	PA9	PA8
Fifth	LA0	LOW	BA10	BA9	BA8	BA7	BA6	BA5

Cycles	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Sixth	LOW	LOW	LOW	LOW	LOW	LOW	LA2	LA1

Notes:

1. CA[14:0] are column addresses, which refer to byte[0]~byte[18431]. Any column address out of this range is invalid;
2. PA[10:0] are page addresses, which refer to page[0]~page[1151]. Any page address out of this range is invalid;
3. BA[10:1] are block addresses, which refer to block[0]~block[1005]. Any block address out of this range is invalid;
4. BA[0] are plane addresses;
5. LA[2:0] are LUN addresses, which refers to 8 LUNs at most.

Table 16. SLC Addressing for DDP/QDP/ODP/HDP (6 Address Cycles Required)

Cycles	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	CA14	CA13	CA12	CA11	CA10	CA9	CA8
Third	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA4	BA3	BA2	BA1	BA0	LOW	LOW	PA8
Fifth	LA0	LOW	BA10	BA9	BA8	BA7	BA6	BA5
Sixth	LOW	LOW	LOW	LOW	LOW	LOW	LA2	LA1

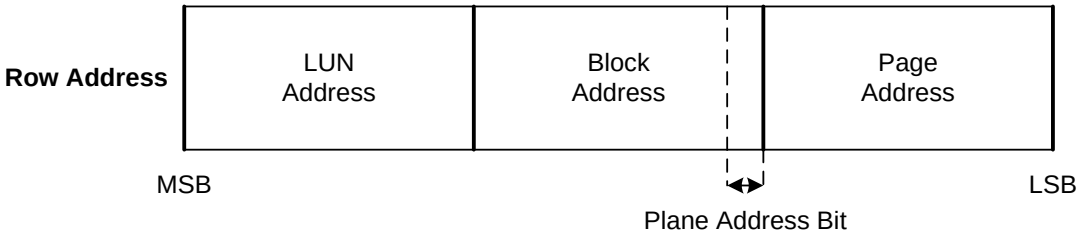
Notes:

1. CA[14:0] are column addresses, which refer to byte[0]~byte[18431]. Any column address out of this range is invalid;
2. PA[8:0] are page addresses, which refer to page[0]~page[383]. Any page address out of this range is invalid;
3. BA[10:1] are block addresses, which refer to block[0]~block[1005]. Any block address out of this range is invalid;
4. BA[0] are plane addresses.
5. LA[2:0] are LUN addresses, which refers to 8 LUNs at most.

3.2.2. Multi-plane Addressing

The plane address comprises the LSB of the block address as shown in the figure below. The plane address is used during a multi-plane operation on a particular LUN. The plane address bit(s) shall be distinct from any other multi-plane operation in the multi-plane command sequence. The page address shall be the same as any other multi-plane operations in the multiplane command sequence.

Figure 9. Location of Plane Address in Row Address



3.2.3. Programming Memory Map

This device supports the one-pass programming method. And it can also be configured into SLC mode to perform SLC programming.

For one-pass programming, Lower Page (LP), Middle Page (MP) and Upper Page (UP) are programmed together. Note that data should be programmed into LP, MP and UP successively. Programming out of this order may cause data loss.

For details on the programming memory map, please refer to application note *YMTC_Gen2_256Gb_TLC_Application_Note_General*.

3.2.4. LUN Selection

LUNs are part of a NAND target and share a single data bus with the host. Ensure that only one LUN is selected for data output to the host at any particular time point to avoid bus contention.

The host selects a LUN for future data output by issuing a Read Status Enhanced command to that LUN. The Read Status Enhanced command shall deselect the output path for all LUNs that are not addressed by the command. The page register selected for output within the LUN is determined by the previous Read commands issued, and is not impacted by Read Status Enhanced.

3.2.5. Restrictions on Multi-LUN Operations

LUNs are independent entities. A multi-LUN operation means that two or more LUNs are simultaneously processing commands. During multi-LUN operations, each LUN involved may be in busy or ready status.

When a Page Program command is issued to any LUN that is not preceded by an 11h command, all idle LUNs may clear their page registers if the program page register clear enhancement is disabled. Thus, the host should not begin a Page Program command on a LUN while a Page Read operation is either ongoing or has completed but the data has not been read from another LUN. A Page Read command can be issued to one LUN while a Page Program command is ongoing within another LUN. If the program page register clear enhancement is enabled, this restriction is not applicable.

When a Page Program command is issued to a LUN, the host should not select another LUN within the same volume until after all data has been input and a 10h or 15h command has been issued. In the case of multi-plane operations, all data input for all multi-plane addresses should be completed prior to selecting another LUN.

When Page Read commands are issued to multiple LUNs, the host shall take steps to avoid issues due to column address corruption. The host shall issue a Change Read Column command before starting to read data from a newly selected LUN.

If a multi-LUN operation has been issued, the next status command issued shall be Read Status Enhanced. The Read Status Enhanced command causes LUNs that are not selected to turn off their output buffers. This ensures that only the LUN selected by the Read Status Enhanced command responds to a subsequent data output cycle. After a Read Status Enhanced command has been completed, the Read Status command may be used until the next multi-LUN operation is issued.

When the host has issued Page Read commands to multiple LUNs at the same time, the host shall issue a Read Status Enhanced command before reading data from each LUN. This ensures that only the LUN selected by the Read Status Enhanced command responds to a data output cycle after being put in data output mode with a 00h command, and thus avoiding bus contention. A Change Read Column (Enhanced) command is required prior to transferring data. An example sequence is shown below:

1. Page Read command issued to LUN 0;
2. Page Read command issued to LUN 1;
3. Read Status Enhanced command issued to LUN 0;
4. Change Read Column (Enhanced) command issued to LUN 0;
5. Data transferred from LUN 0;
6. Read Status Enhanced command issued to LUN 1;
7. Change Read Column (Enhanced) command issued to LUN 1;
8. Data transferred from LUN 1.

When mixed combinations of commands are issued to multiple LUNs (e.g. Page Read commands are issued to one LUN while Page Program commands to another LUN), after the Read Status Enhanced command is issued to the selected LUN, a Change Read Column or Change Read Column Enhanced command shall be issued prior to any data output from the selected LUN.

In all scenarios, the host may substitute a Change Read Column Enhanced sequence for the Read Status Enhanced/Change Read Column sequence if all LUNs are not busy.

3.3. Volume Addressing

3.3.1. Volume Address Appointment

To appoint a volume address, a Set Feature command should be issued with the Volume Configuration feature adderss. The volume address is not retained across power cycles, and thus if a volume is going to be used, this volume address shall be appointed after each target initialization.

3.3.2. Volume Selection

After volume addresses have been appointed, every NAND target (and associated LUN) is selected when the associated CE_n is pulled low. The host issues a Volume Select command to indicate the Volume (i.e. NAND target) that shall execute the next command issued.

3.3.3. Restrictions on Multi-volume Operation

Volumes are independent entities. A multi-volume operation is that two or more volumes are simultaneously processing commands. Before a command is issued to an unselected volume, CE_n shall be pulled high for a minimum of tCEH and a Volume Select command shall then be issued to select the volume. While commands, including multi-LUN operations, are being performed on the selected volume, a Volume Select command is not required.

Issuing the same command to multiple volumes at the same time is not supported.

For a LUN-level command (e.g. a Read or Program command), the host may select a different volume during a data input or data output operation and then resume the data transfer operation at a later time for a LUN-level command. When a volume and its associated LUN(s) are reselected to complete the data input or data output operation, the following actions are required:

- The host shall issue a Change Row Address command prior to resuming data input.
- The host shall issue a Change Read Column Enhanced command prior to resuming data output.

For a target-level command (e.g. a Get Features or Set Features command), the host shall complete all data input or data output operations associated with that command prior to selecting a new volume. A Volume Select command shall not be issued during the following atomic portions of the read, program, erase and copyback operations:

- Read (including Copyback Read)

<CMD: 00h> <ADDR: Column & Row> <CMD: 30h>
<CMD: 00h> <ADDR: Column & Row> <CMD: 31h>
<CMD: 00h> <ADDR: Column & Row> <CMD: 32h>

<CMD: 00h> <ADDR: Column & Row> <CMD: 35h>

- Program (including Copyback Program)

<CMD: 80h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 10h>
<CMD: 80h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 11h>
<CMD: 80h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 15h>
<CMD: 81h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 10h>
<CMD: 81h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 11h>
<CMD: 81h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 15h>
<CMD: 85h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 10h>
<CMD: 85h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 11h>
<CMD: 85h> <ADDR: Column & Row> <DIN: Data Input> <CMD: 15h>

Notes:

The Volume Select command may be issued prior to the 10h, 11h or 15h command if the next command issued to this volume is Change Row Address.

- Erase

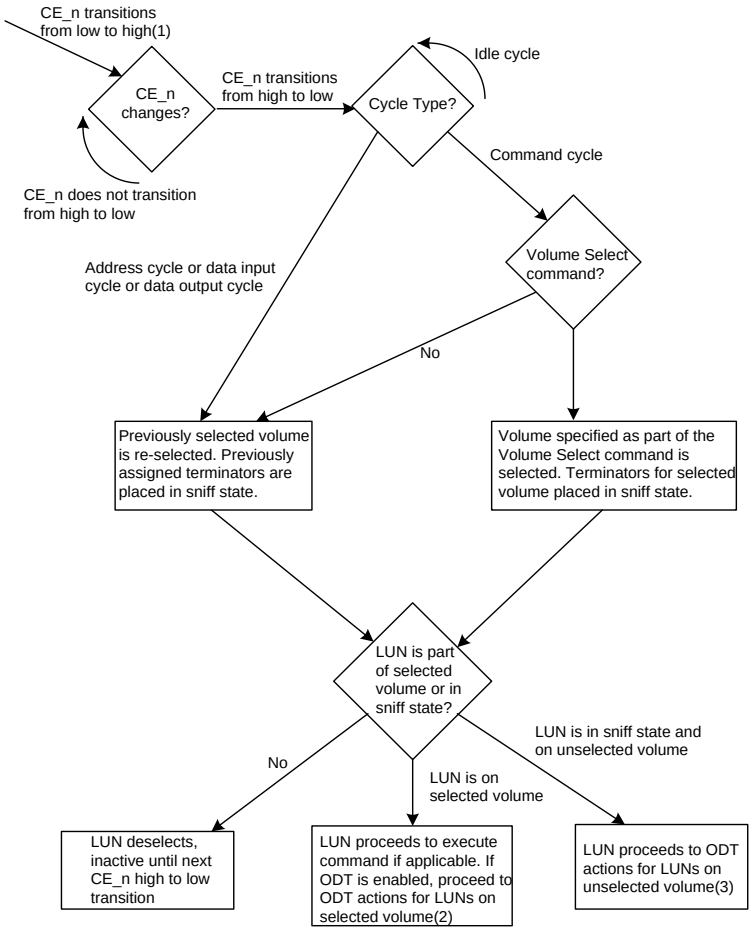
<CMD: 60h> <ADDR: Row> <CMD: D0h>
<CMD: 60h> <ADDR: Row> <CMD: D1h>
<CMD: 60h> <ADDR: Row> <CMD: 60h> <ADDR: Row> <CMD: D1h>

3.3.4. Volume Reversion

If CE_n transitions from high to low and a Volume Select command is not the first command, the LUN shall revert to the previously selected, sniff or deselected state (refer to **Section 5.7.4 "Matrix Termination"**) based on the last specified volume address. If ODT is enabled in the NV-DDR2/NV-DDR3 data interface, there are additional actions described in **Section 5.7 "On-die Termination"**.

The figure below defines the volume reversion requirements when CE_n transitions from high to low.

Figure 10. Volume Reversion Behavior Flow



Notes:

1. This state is entered asynchronously when CE_n transitions from low to high.
2. ODT actions for LUNs on a selected volume are specified in **Figure 24 "ODT Actions for LUNs on Selected Volume"**.
3. ODT actions for LUNs on an unselected volume are specified in **Figure 25 "ODT Actions for LUNs in Sniff on Unselected Volume"**.

3.4. Error Management

NAND Flash may have defective blocks when shipped from factory. And during the endurance life of the product, additional defective blocks may grow with use; however, the total number of valid block per die will not fall below NVB (number of valid blocks).

If a block is defective, the manufacturer shall mark the block as defective by setting the Defective Block Marking. According to ONFI specification, the Defective Block Marking is 00h read out from first byte of the first or last page in the defective block.

Due to the reliability concern, all the blocks might have outgoing patterns at shipping out. In this case, there will be a chance of misread result for bad block scan by reading the 00h data on first and last pages. For other options, please refer to application note *YMTC_Gen2_256Gb_TLC_Application_Note_Bad_Block_Management*.

Figure 11. Area Marked in Factory Defecting Mapping

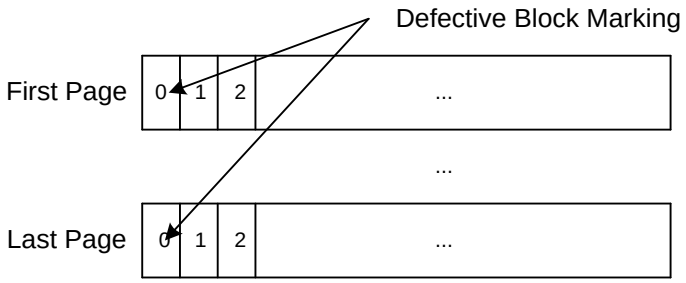


Table 17. Error Management

Parameter	Values
NVB	TBD
ECC Correctibility	TBD

4. Operating Conditions & Electrical Characteristics

4.1. Absolute Maximum Ratings

The stresses greater than those listed in the table below may cause permanent damages to the device. This is a stress rating only.

Table 19. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
V_{CC} Supply Voltage	V_{CC}	-0.6	4.6	V
Reference Voltage	V_{REFQ}	-0.45	2.4	V
V_{PP} Supply Voltage	V_{PP}	-0.6	16	V
Soldering Temperature(1)	T_{SOLDER}	-	260	°C
Storage Temperature	T_{STG}	-65	150	°C
1.8V I/O Signaling				
V_{CCQ} Supply Voltage	V_{CCQ}	-0.45	2.4	V
Input Voltage	V_{IN}	-0.45	2.4	V
Input/Output Voltage	$V_{I/O}$	-0.45	2.4	V
1.2V I/O Signaling				
V_{CCQ} Supply Voltage	V_{CCQ}	-0.4	1.5	V
Input Voltage	V_{IN}	-0.4	1.5	V
Input/Output Voltage	$V_{I/O}$	-0.4	1.5	V

Notes:

1. 260°C/30s/3 times soldering can be done in SLC mode, but cannot be guaranteed in TLC mode.

4.2. Recommended Operating Conditions

Functional operations should be restricted to the conditions listed in the table below. Operations in any other conditions are not guaranteed.

Table 20. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage(1)	V_{CC}	2.35	2.5	3.6	V
Ground Voltage	V_{SS}	0	0	0	V
Supply Voltage for 1.8V I/O Signaling	V_{CCQ}	1.7	1.8	1.95	V
Supply Voltage for 1.2V I/O Signaling	V_{CCQ}	1.14	1.2	1.26	V
Ground Voltage for I/O Signaling	V_{SSQ}	0	0	0	V
Reference Voltage	V_{REFQ}	0.49*V_{CCQ}	0.50*V_{CCQ}	0.51*V_{CCQ}	V
External Voltage	V_{PP}	10.8	12	13.2	V
Operating Temperature(2)	T_{OPER}	0	-	70	°C

Notes:

1. If the voltage supply is out of this range at any time during opertaion, the operation cannot be guaraneteed.
2. Operating temperature (T_{OPER}) is the case surface temperature on the center/top of the NAND.

4.3. AC Overshoot/Undershoot Requirements

The device may have AC overshoot or undershoot from V_{CCQ} and V_{SSQ} levels. The tables below define the maximum values that AC overshoot or undershoot may reach.

Table 21. AC Overshoot/Undershoot Requirements for SDR

Parameter	Maximum Value @ Timing Mode						Unit
	0	1	2	3	4	5	
Maximum Amplitude Allowed for Overshoot Area	1	1	1	1	1	1	V
Maximum Amplitude Allowed for Undershoot Area	1	1	1	1	1	1	V
Maximum Overshoot Area Above V_{CCQ}	3	3	3	3	3	3	V*ns
Maximum Overshoot Area Below V_{SSQ}	3	3	3	3	3	3	V*ns

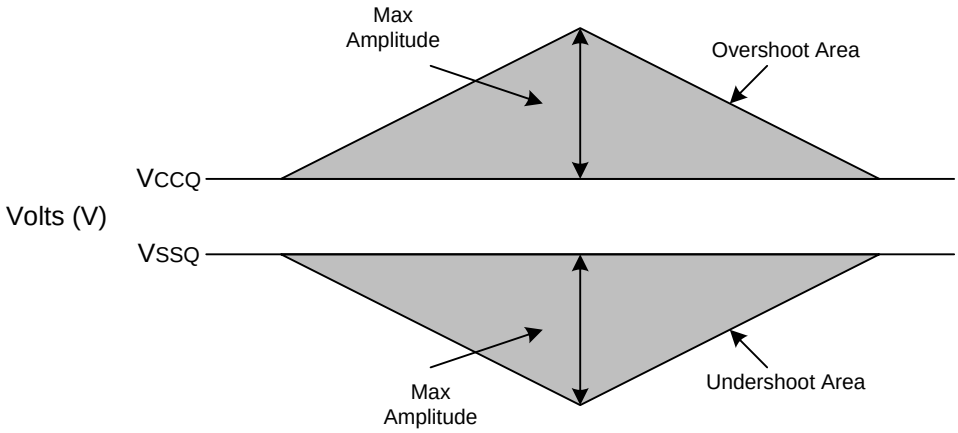
Table 22. AC Overshoot/Undershoot Requirements for NV-DDR2

Parameter	Maximum Value @ Timing Mode									Unit
	0	1	2	3	4	5	6	7	8	
Maximum Amplitude Allowed for Overshoot Area	1	1	1	1	1	1	1	1	1	V
Maximum Amplitude Allowed for Undershoot Area	1	1	1	1	1	1	1	1	1	V
Maximum Overshoot Area Above V_{CCQ} for DQ[7:0], DQS and RE_n	3	3	2.25	1.8	1.5	1.1	0.9	0.75	0.56	V*ns
Maximum Overshoot Area Above V_{CCQ} for Control Signals (exluding DQ[7:0], DQS and RE_n)	3	3	3	3	3	3	3	3	3	V*ns
Maximum Undershoot Area Below V_{SSQ} for DQ[7:0], DQS, RE_n	3	3	2.25	1.8	1.5	1.1	0.9	0.75	0.56	V*ns
Maximum Undershoot Area Below V_{SSQ} for Control Signals (exluding DQ[7:0], DQS and RE_n)	3	3	3	3	3	3	3	3	3	V*ns

Table 23. AC Overshoot/Undershoot Requirements for NV-DDR3

Parameter	Maximum Value @ Timing Mode											Unit
	0	1	2	3	4	5	6	7	8	9	10	
Maximum Amplitude Allowed for Overshoot Area	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	V
Maximum Amplitude Allowed for Undershoot Area	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	V
Maximum Overshoot Area Above V_{CCQ} for DQ[7:0], DQS and RE_n	3	3	2.25	1.8	1.5	1.1	0.9	0.75	0.56	0.45	0.38	V*ns
Maximum Overshoot Area Above V_{CCQ} for Control Signals (exluding DQ[7:0], DQS and RE_n)	3	3	3	3	3	3	3	3	3	3	3	V*ns
Maximum Undershoot Area Below V_{SSQ} for DQ[7:0], DQS, RE_n	3	3	2.25	1.8	1.5	1.1	0.9	0.75	0.56	0.45	0.38	V*ns
Maximum Undershoot Area Below V_{SSQ} for Control Signals (exluding DQ[7:0], DQS and RE_n)	3	3	3	3	3	3	3	3	3	3	3	V*ns

Figure 12. AC Overshoot/Undershoot Definition



4.4. DC and Operating Characteristics

4.4.1. DC and Operating Characteristics

Table 24. DC & Operating Characteristics in SDR(ES only)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Page Read Current On V_{CC} (SLC)	I_{CC1}	Fixed wait time, tR=tR(max)	-	35	TBD	mA
Page Read Current On V_{CC} (TLC)				32	TBD	mA
Page Program Current On V_{CC} (SLC)	I_{CC2}	Fixed wait time, tPROG=tPROG(max)	-	32	TBD	mA
Page Program Current On V_{CC} (TLC)				34	TBD	mA
Erase Current on V_{CC} (SLC)	I_{CC3}	Fixed wait time, tBERS=tBERS(max)	-	25	TBD	mA
Erase Current on V_{CC} (TLC)				25	TBD	mA
Page Read Current on V_{CCQ}	I_{CCQ1}	Fixed wait time, tR=tR(max), without ODT	-	1	TBD	mA
Page Program Current on V_{CCQ}	I_{CCQ2}	Fixed wait time, tPROG=tPROG(max), ODT disabled	-	1	TBD	mA
Erase Current on V_{CCQ}	I_{CCQ3}	Fixed wait time, tBERS=tBERS(max), ODT disabled	-	1	TBD	mA
I/O Burst Read Current for V_{CC} (SDR)	I_{CC4R}	tRC=tRC(min), half of data is switching	-	10	TBD	mA
I/O Burst Read Current for V_{CCQ} (SDR)	I_{CCQ4R}	tRC=tRC(min), half of data is switching, ODT disabled	-	11	TBD	mA
I/O Burst Write Current for V_{CC} (SDR)	I_{CC4W}	tDSC=tDSC(min), half of data is switching	-	12	TBD	mA
I/O Burst Write Current for V_{CCQ} (SDR)	I_{CCQ4W}	tDSC=tDSC(min), half of data is switching, ODT disabled	-	2	TBD	mA
Bus Idle Current on V_{CC}	I_{CC5}	-	-	7	TBD	mA
Bus Idle Current on V_{CCQ}	I_{CCQ5}	-	-	1	TBD	mA
Current During First Reset Command After Power-on	I_{CC6}	-	-	19	TBD	mA
Standby Current on V_{CC}	I_{SB}	CE_n=V_{CCQ}-0.2V, WP_n=0V/V_{CCQ}	-	76	TBD	µA
Standby Current on V_{CCQ}	I_{SBQ}	CE_n=V_{CCQ}-0.2V, WP_n=0V/V_{CCQ} , ODT disabled	-	12	TBD	µA
Input Leakage Current(1)	I_{LI}	V_{IN}=0V to $V_{CCQ(max)}$	-	7	TBD	µA
Output Leakage Current(2)	I_{LO}	V_{OUT}=0V to $V_{CCQ(max)}$	-	7	TBD	µA
V_{REFQ} Leakage Current	I_{VREFQ}	-	-	2	TBD	µA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Staggered Power-Up Current(5)	I_{ST}	CE_n=V_{CCQ}-0.2V, tRISE=1ms, C_{LINE}=0.1µF	-	5	TBD	mA
Output Low Current (R/B Pin)	I_{OL}	V_{OL}=0.2V	-	5	TBD	mA
V_{PP} Active Current	I_{PPA}	V_{PP} is enabled	-	-	TBD	mA
V_{PP} Idle Current	I_{PPI}	V_{PP} is not enabled	-	9	TBD	µA
AC Input High Voltage(3)	$V_{IH(AC)}$	-	0.8*V_{CCQ}	-	-	V
DC Input High Voltage	$V_{IH(DC)}$	-	0.7*V_{CCQ}	-	V_{CCQ}+0.3	V
AC Input Low Voltage(4)	$V_{IL(AC)}$	-	-	-	0.2*V_{CCQ}	V
DC Input Low Voltage	$V_{IL(DC)}$	-	-0.3	-	0.3*V_{CCQ}	V
Output High Voltage	V_{OH}	I_{OH}=-100µA	V_{CCQ}-0.1V	-	-	V
Output Low Voltage	V_{OL}	I_{OL}=100µA	-	-	0.1	V

Notes:

1. The leakage current is measured based on a single die;
2. The leakage current is measured based on a single DQ;
3. Refer to **Section 4.3 "AC Overshoot/Undershoot Requirements"** for the max value;
4. Refer to **Section 4.3"AC Overshoot/Undershoot Requirements"** for the min value.
5. For details, refer to application notes *YMTC_Gen2_256Gb_TLC_Application_Note_General*.

Table 25. DC and Operating Characteristics in NV-DDR2(ES only)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Page Read Current on V_{CC} (SLC)	I_{CC1}	Fixed wait time, tR=tR(max)	-	35	TBD	mA
Page Read Current on V_{CC} (TLC)				32	TBD	mA
Page Program Current on V_{CC} (SLC)	I_{CC2}	Fixed wait time, tPROG=tPROG(max)	-	32	TBD	mA
Page Program Current on V_{CC} (TLC)				34	TBD	mA
Erase Current on V_{CC} (SLC)	I_{CC3}	Fixed wait time, tBERS=tBERS(max)	-	25	TBD	mA
Erase Current on V_{CC} (TLC)				25	TBD	mA
Page Read Current on V_{CCQ}	I_{CCQ1}	Fixed wait time, tR=tR(max), without ODT	-	1	TBD	mA
Page Program Current on V_{CCQ}	I_{CCQ2}	Fixed wait time, tPROG=tPROG(max), ODT disabled	-	1	TBD	mA
Erase Current on V_{CCQ}	I_{CCQ3}	Fixed wait time, tBERS=tBERS(max), ODT disabled	-	1	TBD	mA
I/O Burst Read Current on V_{CC}	I_{CC4R}	tRC=tRC(min), half of data is switching	-	73	TBD	mA
I/O Burst Read Current on V_{CCQ}	I_{CCQ4R}	tRC=tRC(min), half of data is switching, ODT disabled	-	83	TBD	mA
I/O Burst Write Current on V_{CC}	I_{CC4W}	tDSC=tDSC(min), half of data is switching	-	77	TBD	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
I/O Burst Write Current on V_{CCQ}	I_{CCQ4W}	tDSC=tDSC(min), half of data is switching, ODT disabled	-	2	TBD	mA
Bus Idle Current on V_{CC}	I_{CC5}	-	-	7	TBD	mA
Bus Idle Current on V_{CCQ}	I_{CCQ5}	-	-	1	TBD	mA
Standby Current on V_{CC}	I_{SB}	CE_n=V_{CCQ}-0.2V, WP_n=0V/V_{CCQ}	-	74	TBD	µA
Standby Current on V_{CCQ}	I_{SBQ}	CE_n=V_{CCQ}-0.2V, WP_n=0V/V_{CCQ} , ODT disabled	-	9	TBD	µA
Input Leakage Current(1)	I_{LI}	V_{IN}=0V to $V_{CCQ(max)}$	-	7	TBD	µA
Output Leakage Current(2)	I_{LO}	V_{OUT}=0V to $V_{CCQ(max)}$	-	7	TBD	µA
V_{REFQ} Leakage Current	I_{VREFQ}	-	-	2	TBD	µA
Staggered Power-up Current	I_{ST}	CE_n=V_{CCQ}-0.2V, t_{RISE}=1ms, C_{LINE}=0.1uF	-	5	TBD	mA
Output Low Current (R/B Pin)	I_{OL}	V_{OL}=0.2V	-	5	TBD	mA
V_{PP} Active Current	I_{PPA}	V_{PP} is enabled	-	-	TBD	mA
V_{PP} Idle Current	I_{PPI}	V_{PP} is note enabled	-	9	TBD	µA
Single-Ended Signal Without V_{REFQ} (CE_n, WP_n)						
AC Input High Voltage(3)	$V_{IH(AC)}$	-	0.8*V_{CCQ}	-	-	V
DC Input High Voltage	$V_{IH(DC)}$	-	0.7*V_{CCQ}	-	V_{CCQ}+0.3	V
AC Input Low Voltage(4)	$V_{IL(AC)}$	-	-	-	0.2*V_{CCQ}	V
DC Input Low Voltage	$V_{IL(DC)}$	-	-0.3	-	0.3*V_{CCQ}	V
Single-Ended Signal with V_{REFQ}						
AC Input High Voltage(3)	$V_{IH(AC)}$	-	V_{REFQ} +0.25	-	-	V
DC Input High Voltage	$V_{IH(DC)}$	-	V_{REFQ} +0.125	-	V_{CCQ} +0.3	V
AC Input Low Voltage(4)	$V_{IL(AC)}$	-	-	-	V_{REFQ} -0.25	V
DC Input Low Voltage	$V_{IL(DC)}$	-	-0.3	-	V_{REFQ} -0.125	V
Output High Voltage	$V_{OH(AC)}$	-	V_{CCQ}/2 +0.250	-	-	V
Output Low Voltage	$V_{OL(AC)}$	-	-	-	V_{CCQ}/2 –0.250	V
Differential Signal						
AC Input High Voltage	$V_{IHdiff(AC)}$	-	2*[$V_{IH(AC)}$-V_{REFQ}]	-	-	V
DC Input High Voltage	$V_{IHdiff(DC)}$	-	2*[$V_{IH(DC)}$-V_{REFQ}]	-	-	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
AC Input Low Voltage	$V_{ILdiff(AC)}$	-	-	-	$2*[V_{IL(AC)}-V_{REFQ}]$	V
DC Input Low Voltage	$V_{ILdiff(DC)}$	-	-	-	$2*[V_{IL(DC)}-V_{REFQ}]$	V
Output High Voltage	V_{OHdiff}	-	$0.3*V_{CCQ}$	-	-	V
Output Low Voltage	V_{OLdiff}	-	-	-	$-0.3*V_{CCQ}$	V

Notes:

1. The leakage current is measured based on a single die;
2. The leakage current is measured based on a single DQ;
3. Refer to **Section 4.3 "AC Overshoot/Undershoot Requirements"** for the max value;
4. Refer to **Section 4.3 "AC Overshoot/Undershoot Requirements"** for the min value.

Table 26. DC and Operating Characteristics in NV-DDR3(ES only)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Page Read Current on V_{CC} (SLC)	I_{CC1}	Fixed wait time, tR=tR(max)	-	35	TBD	mA
Page Read Current on V_{CC} (TLC)				32	TBD	mA
Page Program Current on V_{CC} (SLC)	I_{CC2}	Fixed wait time, tPROG=tPROG(max)	-	32	TBD	mA
Page Program Current on V_{CC} (TLC)				34	TBD	mA
Erase Current on V_{CC} (SLC)	I_{CC3}	Fixed wait time, tBERS=tBERS(max)	-	25	TBD	mA
Erase Current on V_{CC} (TLC)				25	TBD	mA
Page Read Current on V_{CCQ}	I_{CCQ1}	Fixed wait time, tR=tR(max), without ODT	-	1	TBD	mA
Page Program Current on V_{CCQ}	I_{CCQ2}	Fixed wait time, tPROG=tPROG(max), ODT disabled	-	1	TBD	mA
Erase Current on V_{CCQ}	I_{CCQ3}	Fixed wait time, tBERS=tBERS(max), ODT disabled	-	1	TBD	mA
I/O Burst Read Current on V_{CC}	I_{CC4R}	tRC=tRC(min), half of data is switching	-	73	TBD	mA
I/O Burst Read Current on V_{CCQ}	I_{CCQ4R}	tRC=tRC(min), half of data is switching, ODT disabled	-	58	TBD	mA
I/O Burst Write Current on V_{CC}	I_{CC4W}	tDSC=tDSC(min), half of data is switching	-	77	TBD	mA
I/O Burst Write Current on V_{CCQ}	I_{CCQ4W}	tDSC=tDSC(min), half of data is switching, ODT disabled	-	2	TBD	mA
Bus Idle Current on V_{CC}	I_{CC5}	-	-	7	TBD	mA
Bus Idle Current on V_{CCQ}	I_{CCQ5}	-	-	1	TBD	mA
Standby Current on V_{CC}	I_{SB}	CE_n=V_{CCQ}-0.2V, WP_n=0V/V_{CCQ}	-	74	TBD	µA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Standby Current on V_{CCQ}	I_{SBQ}	CE_n=V_{CCQ}-0.2V, WP_n=0V/V_{CCQ} , ODT disabled	-	12	TBD	µA
Input Leakage Current(1)	I_{LI}	V_{IN}=0V to $V_{CCQ(max)}$	-	7	TBD	µA
Output Leakage Current(2)	I_{LO}	V_{OUT}=0V to $V_{CCQ(max)}$	-	7	TBD	µA
V_{REFQ} Leakage Current	I_{VREFQ}	-	-	1.2	TBD	µA
Staggered Power-up Current	I_{ST}	CE_n=V_{CCQ}-0.2V, t_{RISE}=1ms, C_{LINE}=0.1uF	-	5	TBD	mA
Output Low Current (R/B Pin)	I_{OL}	V_{OL}=0.2V	-	5	TBD	mA
V_{PP} Active Current	I_{PPA}	V_{PP} is enabled	-	-	TBD	mA
V_{PP} Idle Current	I_{PPI}	V_{PP} is note enabled	-	9	TBD	µA
Single-Ended Signal Without V_{REFQ} (CE_n, WP_n)						
AC Input High Voltage(3)	$V_{IH(AC)}$	-	0.8*V_{CCQ}	-	-	V
DC Input High Voltage	$V_{IH(DC)}$	-	0.7*V_{CCQ}	-	V_{CCQ}	V
AC Input Low Voltage(4)	$V_{IL(AC)}$	-	-	-	0.2*V_{CCQ}	V
DC Input Low Voltage	$V_{IL(DC)}$	-	V_{SSQ}	-	0.3*V_{CCQ}	V
Single-Ended Signal with V_{REFQ}						
AC Input High Voltage(3)	$V_{IH(AC)}$	-	V_{REFQ} +0.15	-	-	V
DC Input High Voltage	$V_{IH(DC)}$	-	V_{REFQ} +0.10	-	V_{CCQ}	V
AC Input Low Voltage(4)	$V_{IL(AC)}$	-	-	-	V_{REFQ} -0.15	V
DC Input Low Voltage	$V_{IL(DC)}$	-	V_{SSQ}	-	V_{REFQ} -0.10	V
Output High Voltage	$V_{OH(AC)}$	-	V_{CCQ}/2 +0.250	-	-	V
Output Low Voltage	$V_{OL(AC)}$	-	-	-	V_{CCQ}/2 –0.250	V
Differential Signal						
AC Input High Voltage	$V_{IHdiff(AC)}$	-	2*[$V_{IH(AC)}$-V_{REFQ}]	-	-	V
DC Input High Voltage	$V_{IHdiff(DC)}$	-	2*[$V_{IH(DC)}$-V_{REFQ}]	-	-	V
AC Input Low Voltage	$V_{ILdiff(AC)}$	-	-	-	2*[$V_{IL(AC)}$-V_{REFQ}]	V
DC Input Low Voltage	$V_{ILdiff(DC)}$	-	-	-	2*[$V_{IL(DC)}$-V_{REFQ}]	V
Output High Voltage	V_{OHdiff}	-	0.3*V_{CCQ}	-	-	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Low Voltage	V_{OLdiff}	-	-	-	-0.3*V_{CCQ}	V

Notes:

1. The leakage current is measured based on a single die;
2. The leakage current is measured based on a single DQ;
3. Refer to **Section 4.3 "AC Overshoot/Undershoot Requirements"** for the max value;
4. Refer to **Section 4.3 "AC Overshoot/Undershoot Requirements"** for the min value.

Table 27. AC Differential I/O Voltage in NV-DDR2

Parameter	Symbol	Min	Max	Unit
AC Differential Input Cross-Point Voltage	$V_{IX(AC)}$	0.5*V_{CCQ}–0.175	0.5*V_{CCQ}+0.175	V
AC Differential Output Cross-Point Voltage Without ZQ Calibration	$V_{OX(AC)}$	0.5*V_{CCQ}–0.2	0.5*V_{CCQ}+0.2	V
AC Differential Output Cross-Point Voltage with ZQ Calibration	$V_{OX(AC)}$	0.5*V_{CCQ}–0.15	0.5*V_{CCQ}+0.15	V

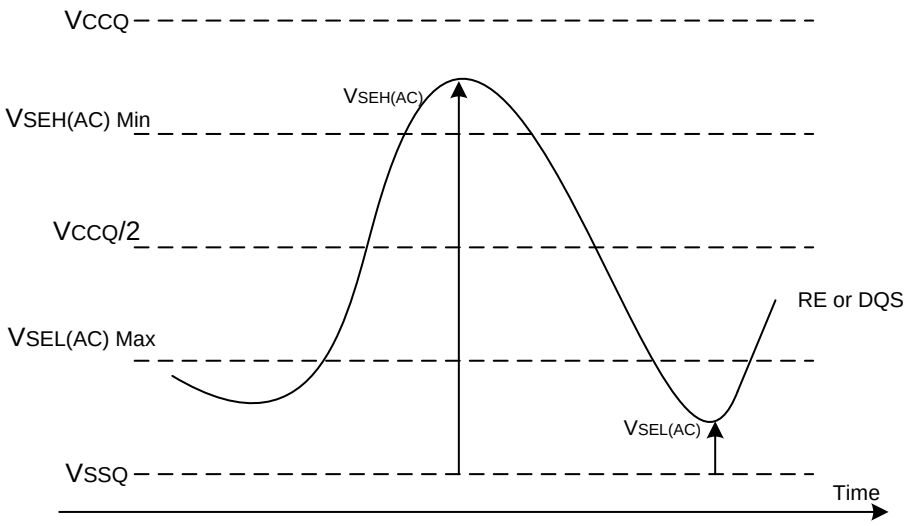
Table 28. AC Differential I/O Voltage in NV-DDR3

Parameter	Symbol	Min	Max	Unit
AC Differential Input Cross-Point Voltage	$V_{IX(AC)}$	0.5*V_{CCQ}–0.12	0.5*V_{CCQ}+0.12	V
AC Differential Output Cross-Point Voltage Without ZQ Calibration	$V_{OX(AC)}$	0.5*V_{CCQ}–0.2	0.5*V_{CCQ}+0.2	V
AC Differential Output Cross-Point Voltage with ZQ Calibration	$V_{OX(AC)}$	0.5*V_{CCQ}–0.15	0.5*V_{CCQ}+0.15	V

4.4.2. Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (RE_t, RE_c, DQS_t or DQS_c) shall comply with requirements for single-ended signals, RE_t and RE_c shall meet $V_{SEH(AC)\ Min}/V_{SEL(AC)\ Max}$ in every half-cycle. DQS_t and DQS_c shall meet $V_{SEH(AC)\ Min}/V_{SEL(AC)\ Max}$ in every half-cycle preceding and following a valid transition.

Figure 13. Single-Ended Requirements for Differential Signals



While control (e.g. ALE, CLE) and DQ signal requirements are with respect to V_{REFQ}, the single-ended components of differential signals have a requirement with respect to $V_{CCQ}/2$. V_{REFQ} and $V_{CCQ}/2$ are nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential signals, the requirement to reach $V_{SEL(AC)\ Max}$, $V_{SEH(AC)\ Min}$ has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 29. Single-Ended Levels for Differential Signals

Parameter	Symbol	Minimum	Maximum	Unit
NV-DDR2 Single-Ended High Level	$V_{SEH(AC)}$	$V_{CCQ}/2+0.250$	See note 1.	V
NV-DDR2 Single-Ended Low Level	$V_{SEL(AC)}$	Note 1	$V_{CCQ}/2–0.250$	V
NV-DDR3 Single-Ended High Level	$V_{SEH(AC)}$	$V_{CCQ}/2+0.150$	See note 1.	V
NV-DDR3 Single-Ended Low Level	$V_{SEL(AC)}$	See note 1.	$V_{CCQ}/2–0.150$	V

Notes:

1. These values are not defined. However, the single-ended signal (RE_t, RE_c, DQS_t or DQS_c) shall be within [$V_{IH(DC)\ Max}$, $V_{IL(DC)\ Min}$] for each single-ended signal as well as the overshoot and undershoot limits.

4.4.3. V_{REFQ} Tolerance

The figure below shows the DC tolerance and AC noise limits for V_{REFQ}. A valid reference voltage $V_{REFQ(t)}$ is shown as a function of time. $V_{REFQ(DC)}$ is the linear average of $V_{REFQ(t)}$ over a very long period of time (e.g. 1 second). This average shall meet the Min/Max requirements defined in the table below. $V_{REFQ(t)}$ may temporarily deviate from $V_{REFQ(DC)}$ by no more than +/-1% V_{CCQ}. $V_{REFQ(t)}$ shall not track noise on V_{CCQ} if this would result in V_{REFQ} deviating out of these specifications.

The location of the V_{REFQ} tolerance measurement is across the pins of the V_{REFQ} de-cap that is closest to the V_{REFQ} pin of the NAND package.

Figure 14. V_{REFQ} DC Tolerance and AC Noise Limits

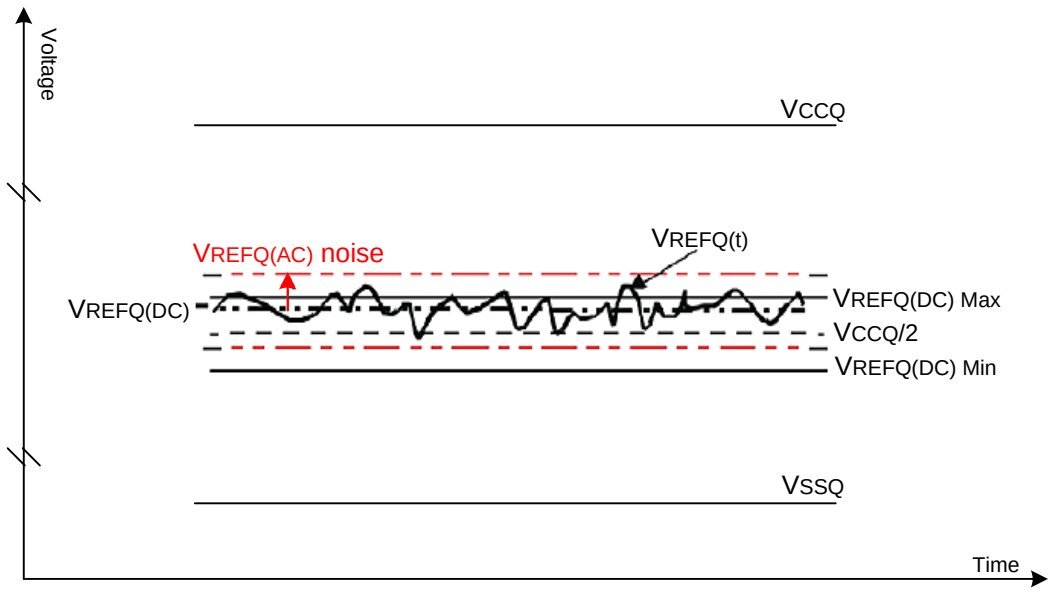


Table 30. V_{REFQ} Specifications

Parameter	Symbol	Minimum	Maximum	Unit
Reference Voltage	$V_{REFQ(DC)}$	0.49*V_{CCQ}	0.51*V_{CCQ}	V

The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $V_{IH(DC)}$, $V_{IL(AC)}$ and $V_{IL(DC)}$ are dependent on V_{REFQ}.

This clarifies that the setup/hold specifications and derating values need to include time and voltage associated with $V_{REFQ(AC)}$ noise. Timing and voltage effects due to $V_{REFQ(AC)}$ noise up to the specified limit (+/-1% of V_{CCQ}) are included in timings and their associated deratings. During any transaction, if the device induces V_{REFQ} noise that is greater than 20MHz and causes a V_{REFQ} violation, the device shall still meet specifications.

External V_{REFQ} may be turned off when all CE_n (NAND targets) that use the external V_{REFQ} are high. Before CE_n is pulled low to enable operation, external V_{REFQ} shall be stable and within the V_{REFQ} tolerance.

4.4.4. I/O Capacitance

Table 31. I/O Capacitance

Parameter	Symbol	Test Condition	Typ	Max	Unit
Input Capacitance (ALE, CE_n, CLE, WE_n, WP_n)	C_{IN}	V_{IN}=0V	1.8	TBD	pF
Input/Output Capacitance (DQ[7:0], DQS)	C_{IO}	V_{IN}=0V/V_{OUT}=0V	1.83	TBD	pF

4.4.5. I/O Slew Rate

When slew rates slower than the minimum values are used, the host must derate timing.

Table 32. Input Slew Rate (NV-DDR2/NV-DDR3)

Parameter	Single-ended	Differential	Unit
Input slew rate (min)	1.0	2.0	V/ns
Input slew rate (max)	4.5	9.0	V/ns

Table 33. Test Conditions for Input Slew Rate

Parameter	Value
Positive input transition (single-ended)	VIL(DC) to VIH(AC)
Negative input transition (single-ended)	VIH(DC) to VIL(AC)
Positive input transition (differential)	VILdiff(AC) to VREFQ
Negative input transition (differential)	VREFQ to VILdiff(DC)

Table 34. Input Slew Rate Derating (NV-DDR2 Single-Ended)

DQ V/ns	DQS Slew Rate Derating VIH(AC)=250mV, VIL(AC)=250mV, VIH(DC)=125mV, VIL(DC)=125mV														
	6		5		3		2		1.5		1		0.9		Unit
	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	
6	0	0	0	0	-	-	-	-	-	-	-	-	-	-	ps
5	0	0	0	0	0	0	-	-	-	-	-	-	-	-	ps
4	-	-	0	0	0	0	0	0	-	-	-	-	-	-	ps
3	-	-	0	0	0	0	0	0	0	0	-	-	-	-	ps
2	-	-	-	-	0	0	0	0	0	0	0	0	-	-	ps
1.5	-	-	-	-	0	0	0	0	0	0	0	0	14	14	ps
1	-	-	-	-	-	-	0	0	0	0	0	0	14	14	ps
0.9	-	-	-	-	-	-	-	-	14	14	14	14	28	28	ps
0.8	-	-	-	-	-	-	-	-	-	-	31	31	45	45	ps

0.7	-	-	-	-	-	-	-	-	-	-	-	-	67	67	ps
0.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ps
0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ps
0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ps
0.3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ps

DQ V/ns	DQS Slew Rate Derating VIH(AC)=250mV, VIL(AC)=250mV, VIH(DC)=125mV, VIL(DC)=125mV												Unit
	0.8		0.7		0.6		0.5		0.4		0.3		
	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	
6	-	-	-	-	-	-	-	-	-	-	-	-	ps
5	-	-	-	-	-	-	-	-	-	-	-	-	ps
4	-	-	-	-	-	-	-	-	-	-	-	-	ps
3	-	-	-	-	-	-	-	-	-	-	-	-	ps
2	-	-	-	-	-	-	-	-	-	-	-	-	ps
1.5	-	-	-	-	-	-	-	-	-	-	-	-	ps
1	31	31	-	-	-	-	-	-	-	-	-	-	ps
0.9	45	45	67	67	-	-	-	-	-	-	-	-	ps
0.8	63	63	85	85	115	115	-	-	-	-	-	-	ps
0.7	85	85	107	107	137	137	179	179	-	-	-	-	ps
0.6	115	115	137	137	167	167	208	208	271	271	-	-	ps
0.5	-	-	179	179	208	208	250	250	313	313	418	418	ps
0.4	-	-	-	-	271	271	313	313	375	375	480	480	ps
0.3	-	-	-	-	-	-	418	418	480	480	594	594	ps

Notes: "-" area indicates that input slew rate combination is not supported.

Table 35. Input Slew Rate Derating (NV-DDR2 Differential)

DQ V/ns	DQS_t/DQS_c Slew Rate Derating VIH(AC)=250mV, VIL(AC)=250mV, VIH(DC)=125mV, VIL(DC)=125mV												Unit
	12		6		4		3		2		1.8		
	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	
6	-26	-26	-21	-21	-16	-16	-	-	-	-	-	-	ps
3	-26	-26	-21	-21	-16	-16	-10	-10	-	-	-	-	ps
2	-	-	-21	-21	-16	-16	-10	-10	0	0	-	-	ps
1.5	-	-	-	-	-16	-16	-10	-10	0	0	7	7	ps
1	-	-	-	-	-16	-16	-10	-10	0	0	7	7	ps
0.9	-	-	-	-	-	-	3	3	14	14	21	21	ps
0.8	-	-	-	-	-	-	-	-	31	31	38	38	ps
0.7	-	-	-	-	-	-	-	-	-	-	61	61	ps
0.6	-	-	-	-	-	-	-	-	-	-	-	-	ps
0.5	-	-	-	-	-	-	-	-	-	-	-	-	ps

0.4	-	-	-	-	-	-	-	-	-	-	-	-	ps
0.3	-	-	-	-	-	-	-	-	-	-	-	-	ps

DQ V/ns	DQS_t/DQS_c Slew Rate Derating VIH(AC)=250mV, VIL(AC)=250mV, VIH(DC)=125mV, VIL(DC)=125mV												
	1.6		1.4		1.2		1		0.8		0.6		Unit
	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	
6	-	-	-	-	-	-	-	-	-	-	-	-	ps
3	-	-	-	-	-	-	-	-	-	-	-	-	ps
2	-	-	-	-	-	-	-	-	-	-	-	-	ps
1.5	-	-	-	-	-	-	-	-	-	-	-	-	ps
1	16	16	-	-	-	-	-	-	-	-	-	-	ps
0.9	30	30	41	41	-	-	-	-	-	-	-	-	ps
0.8	47	47	58	58	73	73	-	-	-	-	-	-	ps
0.7	69	69	80	80	95	95	116	116	-	-	-	-	ps
0.6	99	99	110	110	125	125	146	146	176	176	-	-	ps
0.5	-	-	152	152	167	167	188	188	218	218	269	269	ps
0.4	-	-	-	-	229	229	250	250	282	282	333	333	ps
0.3	-	-	-	-	-	-	355	355	385	385	436	436	ps

Notes: "-" area indicates that input slew rate combination is not supported.

Table 36. Input Slew Rate Derating (NV-DDR3 Single-Ended)

DQ V/ns	DQS Slew Rate Derating VIH(AC)=150mV, VIL(AC)=150mV, VIH(DC)=100mV, VIL(DC)=100mV														
	6		5		3		2		1.5		1		0.9		Unit
	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	
6	0	0	0	0	-	-	-	-	-	-	-	-	-	-	ps
5	0	0	0	0	0	0	-	-	-	-	-	-	-	-	ps
4	-	-	0	0	0	0	0	0	-	-	-	-	-	-	ps
3	-	-	0	0	0	0	0	0	0	0	-	-	-	-	ps
2	-	-	-	-	0	0	0	0	0	0	0	0	-	-	ps
1.5	-	-	-	-	0	0	0	0	0	0	0	0	11	11	ps
1	-	-	-	-	-	-	0	0	0	0	0	0	11	11	ps
0.9	-	-	-	-	-	-	-	-	11	11	11	11	22	22	ps
0.8	-	-	-	-	-	-	-	-	-	-	25	25	36	36	ps
0.7	-	-	-	-	-	-	-	-	-	-	-	-	54	54	ps
0.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ps
0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ps
0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ps
0.3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ps

DQ V/ns	DQS Slew Rate Derating VIH(AC)=150mV, VIL(AC)=150mV, VIH(DC)=100mV, VIL(DC)=100mV												
	0.8		0.7		0.6		0.5		0.4		0.3		Unit
	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	
6	-	-	-	-	-	-	-	-	-	-	-	-	ps
5	-	-	-	-	-	-	-	-	-	-	-	-	ps
4	-	-	-	-	-	-	-	-	-	-	-	-	ps
3	-	-	-	-	-	-	-	-	-	-	-	-	ps
2	-	-	-	-	-	-	-	-	-	-	-	-	ps
1.5	-	-	-	-	-	-	-	-	-	-	-	-	ps
1	25	25	-	-	-	-	-	-	-	-	-	-	ps
0.9	36	36	54	54	-	-	-	-	-	-	-	-	ps
0.8	50	50	68	68	92	92	-	-	-	-	-	-	ps
0.7	68	68	86	86	110	110	143	143	-	-	-	-	ps
0.6	92	92	110	110	133	133	167	167	217	217	-	-	ps
0.5	-	-	143	143	167	167	200	200	250	250	333	333	ps
0.4	-	-	-	-	217	217	250	250	300	300	383	383	ps
0.3	-	-	-	-	-	-	333	333	383	383	467	467	ps

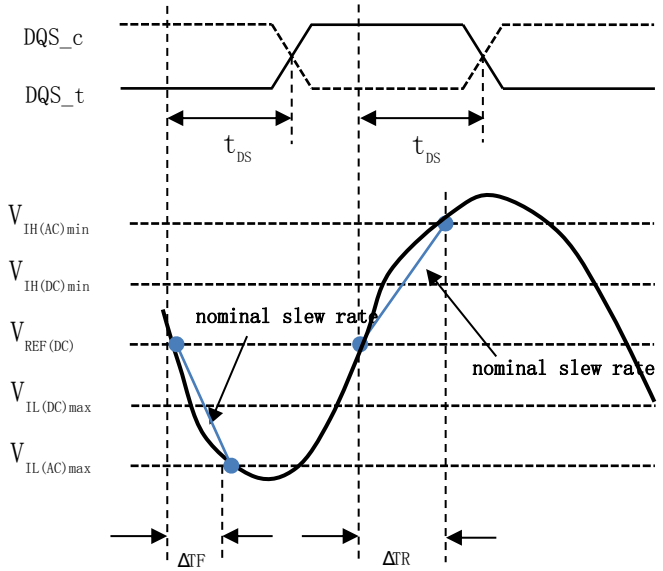
Notes: "-" area indicates that input slew rate combination is not supported.

Table 37. Input Slew Rate Derating (NV-DDR3 Differential)

DQ V/ns	DQS_t/DQS_c Slew Rate Derating VIH(AC)=150mV, VIL(AC)=150mV, VIH(DC)=100mV, VIL(DC)=100mV												
	12		6		4		3		2		1.8		Unit
	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	
6	-63	-31	-33	-17	-25	-13	-	-	-	-	-	-	ps
3	-63	-31	-33	-17	-25	-13	-17	-8	-	-	-	-	ps
2	-	-	-33	-17	-25	-13	-17	-8	0	0	-	-	ps
1.5	-	-	-	-	-25	-13	-17	-8	0	0	6	6	ps
1	-	-	-	-	-25	-13	-17	-8	0	0	6	6	ps
0.9	-	-	-	-	-	-	-6	3	11	11	17	17	ps
0.8	-	-	-	-	-	-	-	-	25	25	31	31	ps
0.7	-	-	-	-	-	-	-	-	-	-	48	48	ps
0.6	-	-	-	-	-	-	-	-	-	-	-	-	ps
0.5	-	-	-	-	-	-	-	-	-	-	-	-	ps
0.4	-	-	-	-	-	-	-	-	-	-	-	-	ps
0.3	-	-	-	-	-	-	-	-	-	-	-	-	ps
DQ V/ns	DQS_t/DQS_c Slew Rate Derating VIH(AC)=150mV, VIL(AC)=150mV, VIH(DC)=100mV, VIL(DC)=100mV												
	1.6		1.4		1.2		1		0.8		0.6		Unit

	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	Δset	Δhold	
6	-	-	-	-	-	-	-	-	-	-	-	-	ps
3	-	-	-	-	-	-	-	-	-	-	-	-	ps
2	-	-	-	-	-	-	-	-	-	-	-	-	ps
1.5	-	-	-	-	-	-	-	-	-	-	-	-	ps
1	13	13	-	-	-	-	-	-	-	-	-	-	ps
0.9	24	24	33	33	-	-	-	-	-	-	-	-	ps
0.8	38	38	46	46	58	58	-	-	-	-	-	-	ps
0.7	55	55	64	64	76	76	93	93	-	-	-	-	ps
0.6	79	79	88	88	100	100	117	117	142	142	-	-	ps
0.5	-	-	121	121	133	133	150	150	175	175	217	217	ps
0.4	-	-	-	-	183	183	200	200	225	225	267	267	ps
0.3	-	-	-	-	-	-	283	283	308	308	350	350	ps

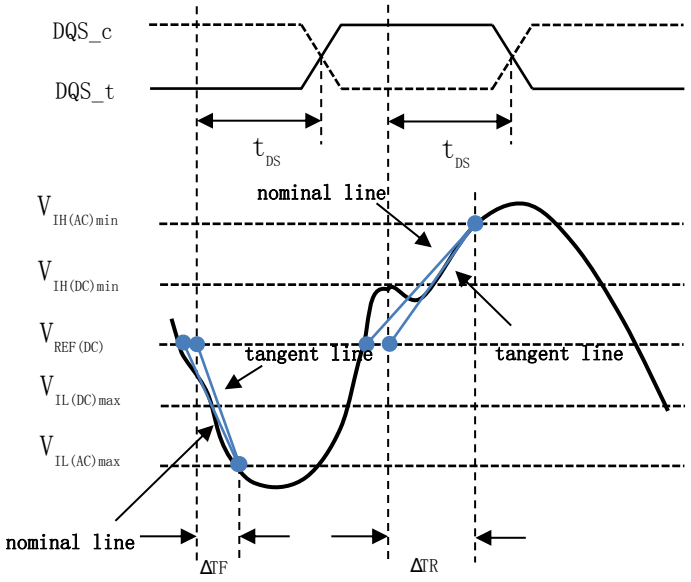
Figure 15. Nominal Slew Rate for Data Setup Time



$$\text{Setup Slew Rate Falling signal} = \frac{VREF(DC) - VIL(AC)max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising signal} = \frac{VIH(AC)min - VREF(DC)}{\Delta TR}$$

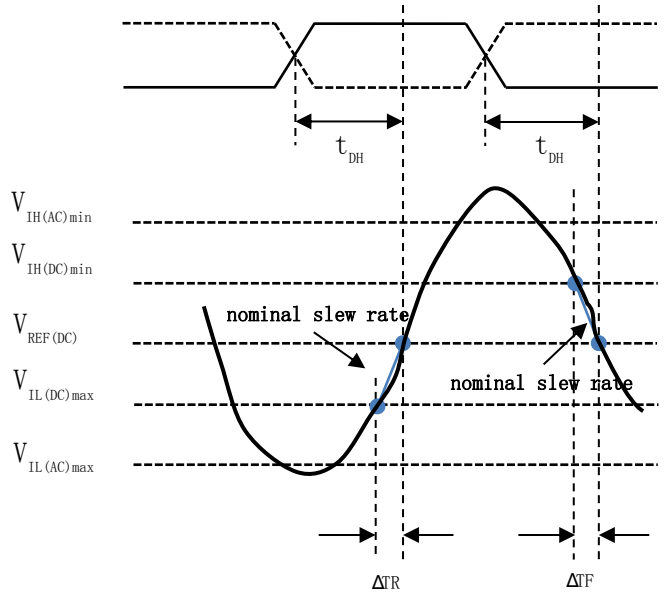
Figure 16. Tangent Line for Data Setup Time



$$\text{Setup Slew Rate Falling signal} = \frac{tangent\ line[VREF(DC) - VIL(AC)max]}{\Delta TF}$$

$$\text{Setup Slew Rate Rising signal} = \frac{tangent\ line[VIH(AC)min - VREF(DC)]}{\Delta TR}$$

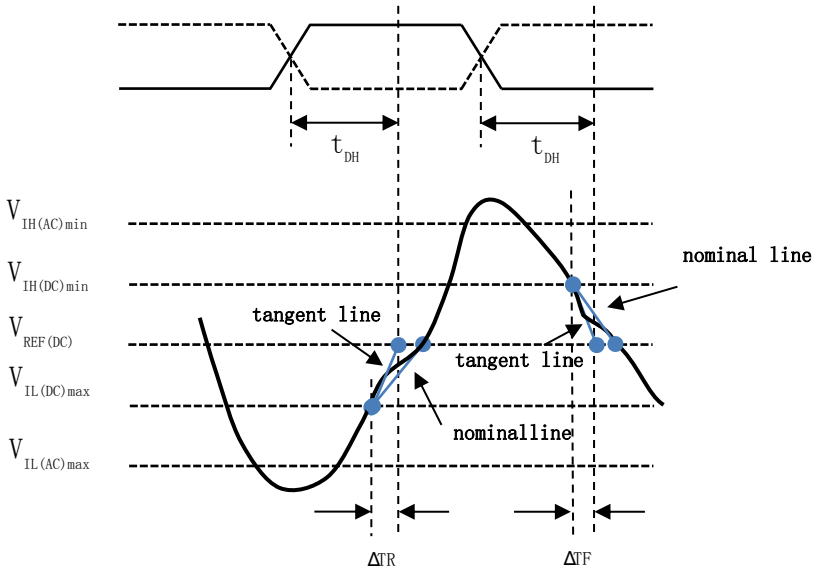
Figure 17. Nominal Slew Rate for Data Hold Time



$$\text{Hold Slew Rate Falling signal} = \frac{VIH(DC)min - VREF(DC)}{\Delta TF}$$

$$\text{Setup Slew Rate Rising signal} = \frac{VREF(DC) - VIL(DC)max}{\Delta TR}$$

Figure 18. Tangent Line for Data Hold Time



$$\text{Hold Slew Rate Falling signal} = \frac{tangent\ line[VIH(DC)min - VREF(DC)]}{\Delta TF}$$

$$\text{Hold Slew Rate Rising signal} = \frac{tangent\ line[VREF(DC) - VIL(DC)max]}{\Delta TR}$$

Table 38. Output Slew Rate (SDR)

Output Drive Strength	Min	Max	Unit
25 Ohms	0.85	5	V/ns
35 Ohms	0.75	4	V/ns
50 Ohms	0.6	4	V/ns

Table 39. Output Slew Rate (NV-DDR2, w/o ZQ Calibration, Single-Ended)

Output Drive Strength	Min	Max	Unit
25 Ohms	0.85	5	V/ns
35 Ohms	0.75	4	V/ns
50 Ohms	0.6	4	V/ns

Table 40. Output Slew Rate (NV-DDR2, w/o ZQ Calibration, Differential)

Output Drive Strength	Min	Max	Unit
25 Ohms	1.7	10.0	V/ns
35 Ohms	1.5	8.0	V/ns
50 Ohms	1.2	8.0	V/ns

Table 41. Output Slew Rate (NV-DDR2, with ZQ Calibration, Single-Ended)

Output Drive Strength	Min	Max	Unit
35 Ohms	1.08	4	V/ns
50 Ohms	0.9	3.5	V/ns

Table 42. Output Slew Rate (NV-DDR2, with ZQ Calibration, Differential)

Output Drive Strength	Min	Max	Unit
35 Ohms	2.16	8.0	V/ns
50 Ohms	1.8	7.0	V/ns

Table 43. Output Slew Rate (NV-DDR3, with ZQ Calibration, Single-Ended)

Output Drive Strength	Min	Max	Unit
35 Ohms	0.72	4	V/ns
50 Ohms	0.6	3.5	V/ns

Table 44. Output Slew Rate (NV-DDR3, with ZQ Calibration, Differential)

Output Drive Strength	Min	Max	Unit
35 Ohms	1.44	8.0	V/ns
50 Ohms	1.2	7.0	V/ns

Table 45. Test Conditions for Output Slew Rate

Parameter	Value (SDR)	Value (NV-DDR2, Single-Ended)	Value (NV-DDR2, Differential)	Value (NV-DDR3, Single-Ended)	Value (NV-DDR3, Differential)
VOL(DC)	$0.4*V_{CCQ}$	-	-		
VOH(DC)	$0.6*V_{CCQ}$	-	-		
VOL(AC)	$0.3*V_{CCQ}$	V_{TT} - $0.15*V_{CCQ}$	-	V_{TT} - $0.1*V_{CCQ}$	-
VOH(AC)	$0.7*V_{CCQ}$	V_{TT} + $0.15*V_{CCQ}$	-	V_{TT} + $0.1*V_{CCQ}$	-
VOLdiff(AC)	-	-	$-0.3*V_{CCQ}$	-	$-0.2*V_{CCQ}$
VOHdiff(AC)	-	-	$0.3*V_{CCQ}$	-	$0.2*V_{CCQ}$
tRISE	Time during rising edge from $V_{OL(DC)}$ to $V_{OH(AC)}$	Time during rising edge from $V_{OL(AC)}$ to $V_{OH(AC)}$	-	Time during rising edge from $V_{OL(AC)}$ to $V_{OH(AC)}$	-
tFALL	Time during falling edge from $V_{OH(DC)}$ to $V_{OL(AC)}$	Time during falling edge from $V_{OH(AC)}$ to $V_{OL(AC)}$	-	Time during falling edge from $V_{OH(AC)}$ to $V_{OL(AC)}$	-
tRISEdiff	-	-	Time during rising edge from $V_{OLdiff(AC)}$ to $V_{OHdiff(AC)}$	-	Time during rising edge from $V_{OLdiff(AC)}$ to $V_{OHdiff(AC)}$
tFALLdiff	-	-	Time during rising edge from $V_{OHdiff(AC)}$ to $V_{OLdiff(AC)}$	-	Time during rising edge from $V_{OHdiff(AC)}$ to $V_{OLdiff(AC)}$
Output slew rate, rising edge	$[V_{OH(AC)}-V_{OL(DC)}]/t_{RISE}$	$[V_{OH(AC)}-V_{OL(AC)}]/t_{RISE}$	$[V_{OHdiff(AC)}-V_{OLdiff(AC)}]/t_{RISE}$	$[V_{OH(AC)}-V_{OL(AC)}]/t_{RISE}$	$[V_{OHdiff(AC)}-V_{OLdiff(AC)}]/t_{RISE}$
Output slew rate, falling edge	$[V_{OH(DC)}-V_{OL(AC)}]/t_{FALL}$	$[V_{OH(AC)}-V_{OL(AC)}]/t_{FALL}$	$[V_{OHdiff(AC)}-V_{OLdiff(AC)}]/t_{FALL}$	$[V_{OH(AC)}-V_{OL(AC)}]/t_{FALL}$	$[V_{OHdiff(AC)}-V_{OLdiff(AC)}]/t_{FALL}$
Output reference load	50 Ohms to V_{TT}	50 Ohms to V_{TT}	50 Ohms to V_{TT}	50 Ohms to V_{TT}	50 Ohms to V_{TT}
Temperature range	T_A	T_A	T_A	T_A	T_A

Notes: $V_{TT}=0.5*V_{CCQ}$

4.5. I/O Driver Strength

4.5.1. Output Driver Strength

Because NAND Flash is designed for use in systems that are typically point-to-point connections, an option to control the drive strength of the output buffers is provided. Drive strength should be selected based on the expected loading of the memory bus. The 35 Ohms output drive strength is the power-on default value in the SDR, NV-DDR2 and NV-DDR3 interfaces. This host can select a different drive strength using Set Feature command. It supports thesettings in the table below.

Table 46. Output Drive Strength Settings

Setting	Drive Strength
Overdrive	1.4x = 25 Ohms (SDR and NV-DDR2 only)
Nominal	1.0x = 35 Ohms
Underdrive	0.7x = 50 Ohms

The output impedance range from minimum to maximum covers process, voltage, and temperature variations.

Table 47. Test Conditions for Impedance Values for NV-DDR2

Impedance Range	Process Condition	V_{CCQ}	Temperature
Minimum	Slow-Slow	1.7V	TA (max)
Nominal	Typical-Typical	1.8V	+25°C
Maximum	Fast-Fast	1.95V	TA (min)

Table 48. Test Conditions for Impedance Values for NV-DDR3

Impedance Range	Process Condition	V_{CCQ}	Temperature
Minimum	Slow-Slow	1.14V	TA (max)
Nominal	Typical-Typical	1.2V	+25°C
Maximum	Fast-Fast	1.26V	TA (min)

Table 49. Output Drive Strength Impedance Values w/o ZQ Calibration (1.8V V_{CCQ}, NV-DDR2)

Output Strength	RPD/RPU	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit

25 Ohms	RPD	V_{CCQ} x 0.2	11.4	25.0	44.0	Ohms
		V_{CCQ} x 0.5	15.0	25.0	44.0	Ohms
		V_{CCQ} x 0.8	15.0	25.0	61.0	Ohms
	RPU	V_{CCQ} x 0.2	15.0	25.0	61.0	Ohms
		V_{CCQ} x 0.5	15.0	25.0	44.0	Ohms
		V_{CCQ} x 0.8	11.4	25.0	44.0	Ohms
35 Ohms	RPD	V_{CCQ} x 0.2	16.0	35.0	61.0	Ohms
		V_{CCQ} x 0.5	21.0	35.0	61.0	Ohms
		V_{CCQ} x 0.8	21.0	35.0	85.3	Ohms
	RPU	V_{CCQ} x 0.2	21.0	35.0	85.3	Ohms
		V_{CCQ} x 0.5	21.0	35.0	61.0	Ohms
		V_{CCQ} x 0.8	16.0	35.0	61.0	Ohms
50 Ohms	RPD	V_{CCQ} x 0.2	24.0	50.0	87.0	Ohms
		V_{CCQ} x 0.5	30.0	50.0	87.0	Ohms
		V_{CCQ} x 0.8	30.0	50.0	122.0	Ohms
	RPU	V_{CCQ} x 0.2	30.0	50.0	122.0	Ohms
		V_{CCQ} x 0.5	30.0	50.0	87.0	Ohms
		V_{CCQ} x 0.8	24.0	50.0	87.0	Ohms

Table 50. Output Drive Strength Impedance Values with ZQ Calibration (1.8V V_{CCQ}, NV-DDR2)

Output Strength	RPD/RPU	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
35 Ohms	RPD	V_{CCQ} x 0.2	0.57	1	1.15	RZQ/8.5
		V_{CCQ} x 0.5	0.85	1	1.15	RZQ/8.5
		V_{CCQ} x 0.8	0.85	1	1.47	RZQ/8.5
	RPU	V_{CCQ} x 0.2	0.85	1	1.47	RZQ/8.5
		V_{CCQ} x 0.5	0.85	1	1.15	RZQ/8.5
		V_{CCQ} x 0.8	0.57	1	1.15	RZQ/8.5
50 Ohms	RPD	V_{CCQ} x 0.2	0.57	1	1.15	RZQ/6
		V_{CCQ} x 0.5	0.85	1	1.15	RZQ/6
		V_{CCQ} x 0.8	0.85	1	1.47	RZQ/6
	RPU	V_{CCQ} x 0.2	0.85	1	1.47	RZQ/6
		V_{CCQ} x 0.5	0.85	1	1.15	RZQ/6
		V_{CCQ} x 0.8	0.57	1	1.15	RZQ/6

Notes:

1. Tolerance limits assume RZQ of 300Ω ±1% and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage.
2. Refer to **Section 4.5.2 "Output Driver Sensitivity"** if either the temperature or the voltage changes after calibration.
3. The minimum values are derated by 6% when the device operates between –40°C and 0°C (TC).

Table 51. Output Drive Strength Impedance Values w/o ZQ Calibration (1.2V V_{CCQ}, NV-DDR3)

Output Strength	RPD/RPU	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
35 Ohms	RPD	V_{CCQ} x 0.2	16.0	35.0	61.0	Ohms
		V_{CCQ} x 0.5	21.0	35.0	61.0	Ohms
		V_{CCQ} x 0.8	21.0	35.0	85.3	Ohms
	RPU	V_{CCQ} x 0.2	21.0	35.0	85.3	Ohms
		V_{CCQ} x 0.5	21.0	35.0	61.0	Ohms
		V_{CCQ} x 0.8	16.0	35.0	61.0	Ohms
50 Ohms	RPD	V_{CCQ} x 0.2	24.0	50.0	87.0	Ohms
		V_{CCQ} x 0.5	30.0	50.0	87.0	Ohms
		V_{CCQ} x 0.8	30.0	50.0	122.0	Ohms
	RPU	V_{CCQ} x 0.2	30.0	50.0	122.0	Ohms
		V_{CCQ} x 0.5	30.0	50.0	87.0	Ohms
		V_{CCQ} x 0.8	24.0	50.0	87.0	Ohms

Table 52. Output Drive Strength Impedance Values with ZQ Calibration (1.2V V_{CCQ}, NV-DDR3)

Output Strength	RPD/RPU	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
35 Ohms	RPD	V_{CCQ} x 0.2	0.57	1	1.15	RZQ/8.5
		V_{CCQ} x 0.5	0.85	1	1.15	RZQ/8.5
		V_{CCQ} x 0.8	0.85	1	1.47	RZQ/8.5
	RPU	V_{CCQ} x 0.2	0.85	1	1.47	RZQ/8.5
		V_{CCQ} x 0.5	0.85	1	1.15	RZQ/8.5
		V_{CCQ} x 0.8	0.57	1	1.15	RZQ/8.5
50 Ohms	RPD	V_{CCQ} x 0.2	0.57	1	1.15	RZQ/6
		V_{CCQ} x 0.5	0.85	1	1.15	RZQ/6
		V_{CCQ} x 0.8	0.85	1	1.47	RZQ/6
	RPU	V_{CCQ} x 0.2	0.85	1	1.47	RZQ/6
		V_{CCQ} x 0.5	0.85	1	1.15	RZQ/6
		V_{CCQ} x 0.8	0.57	1	1.15	RZQ/6

Notes:

1. Tolerance limits assume RZQ of 300Ω ±1% and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage.
2. Refer to **Section 4.5.2 "Output Driver Sensitivity"** if either the temperature or the voltage changes after calibration.
3. The minimum values are derated by 6% when the device operates between –40°C and 0°C (TC).

4.5.2. Output Driver Sensitivity

If either the temperature or the voltage changes after ZQ calibration, then the tolerance limits listed in **Table 50 "Output Drive Strength Impedance Values with ZQ Calibration (1.8V VCCQ, NV-DDR2)"** and **Table 52 "Output Drive Strength Impedance Values with ZQ Calibration (1.2V VCCQ, NV-DDR3)"** can be expected to widen according to below tables.

Table 53. Output Driver Sensitivity Definition

Output Strength	RPD/RPU	V_{OUT} to V_{SSQ}	Minimum	Maximum	Unit
35 Ohms	RPD	V_{CCQ} x 0.2	0.57 - dRONdT x ΔT - dRONdV x ΔV	1.15 + dRONdT x ΔT + dRONdV x ΔV	RZQ/8.5
		V_{CCQ} x 0.5	0.85 - dRONdT x ΔT - dRONdV x ΔV	1.15 + dRONdT x ΔT + dRONdV x ΔV	RZQ/8.5
		V_{CCQ} x 0.8	0.85 - dRONdT x ΔT - dRONdV x ΔV	1.47 + dRONdT x ΔT + dRONdV x ΔV	RZQ/8.5
	RPU	V_{CCQ} x 0.2	0.85 - dRONdT x ΔT - dRONdV x ΔV	1.47 + dRONdT x ΔT + dRONdV x ΔV	RZQ/8.5
		V_{CCQ} x 0.5	0.85 - dRONdT x ΔT - dRONdV x ΔV	1.15 + dRONdT x ΔT + dRONdV x ΔV	RZQ/8.5
		V_{CCQ} x 0.8	0.57 - dRONdT x ΔT - dRONdV x ΔV	1.15 + dRONdT x ΔT + dRONdV x ΔV	RZQ/8.5
50 Ohms	RPD	V_{CCQ} x 0.2	0.57 - dRONdT x ΔT - dRONdV x ΔV	1.15 + dRONdT x ΔT + dRONdV x ΔV	RZQ/6
		V_{CCQ} x 0.5	0.85 - dRONdT x ΔT - dRONdV x ΔV	1.15 + dRONdT x ΔT + dRONdV x ΔV	RZQ/6
		V_{CCQ} x 0.8	0.85 - dRONdT x ΔT - dRONdV x ΔV	1.47 + dRONdT x ΔT + dRONdV x ΔV	RZQ/6
	RPU	V_{CCQ} x 0.2	0.85 - dRONdT x ΔT - dRONdV x ΔV	1.47 + dRONdT x ΔT + dRONdV x ΔV	RZQ/6
		V_{CCQ} x 0.5	0.85 - dRONdT x ΔT - dRONdV x ΔV	1.15 + dRONdT x ΔT + dRONdV x ΔV	RZQ/6
		V_{CCQ} x 0.8	0.57 - dRONdT x ΔT - dRONdV x ΔV	1.15 + dRONdT x ΔT + dRONdV x ΔV	RZQ/6

Table 54. Output Driver Voltage and Temperature Sensitivity

Change	Minimum	Maximum	Unit
dRONdT	0	0.5	%/°C
dRONdV	0	0.2	%/mV

4.6. Performance Characteristics

Table 55. Performance Specifications(ES only)

Parameter	Symbol	Typ	Max	Unit
Change Column Setup Time	tCCS	-	400	ns
Interface and Timing Mode Change Time	tITC	-	1	µs
Busy Time for Set Features and Get Features	tFEAT	-	1	µs
Single-Plane Page Read Operation Time (SLC)(1)	tR	34	TBD	µs
Single-Plane Page Read Operation Time (TLC)(1)	tR	57/74/57	TBD	µs
Multi-Plane Page Read Operation Time (SLC)(1)	tR_MP	34	TBD	µs
Multi-Plane Page Read Operation Time (TLC)(1)	tR_MP	57/74/57	TBD	µs
Partial Read 4KB Operation Time (SLC)(1)	tRP	32	TBD	µs
Partial Read 4KB Operation Time (TLC)(1)	tRP	48/60/48	TBD	µs
Number of Partial Page Programs (SLC)	NOP	-	4	-
Number of Partial Page Programs (TLC)	NOP	-	1	-
Program Operation Time (SLC)	tPROG	200	TBD	µs
Program Operation Time (TLC)	tPROG	760	TBD	µs
Program Suspend Operation Time	tPSPD	56	TBD	µs
Program Resume Operation Time	tPRES	-	2	µs
Block Erase Operation Time (SLC)	tBERS	3.3	TBD	ms
Block Erase Operation Time (TLC)	tBERS	9	TBD	ms
Erase Suspend Operation Time	tESPD	46	TBD	µs
Erase Resume Operation Time	tERES	-	2	µs
Read Cache Busy Time	tRCBSY	8	TBD	µs
Program Cache Busy Time	tPCBSY	12.8	TBD	µs
Busy Time for Multi-Plane Program Operation	tPLPBSY	300	TBD	ns
Busy Time for Multi-Plane Erase Operation	tPLEBSY	515	TBD	ns
Busy Time for Multi-Plane Read Operation	tPLRBSY	305	TBD	ns
Power-on Reset Time	tPOR	2	TBD	ms
Normal Operation Long Calibration Time	tZQCL	485	TBD	ns
Normal Operation Short Calibration Time	tZQCS	410	TBD	ns

Notes:

1. This is measured while the randomizer is off.

5. Device Operation

5.1. Power Cycle Requirements

As part of a power cycle, the host shall hold both the V_{CC} and V_{CCQ} voltage levels below 100mV for a minimum time of 100ns. If these requirements are not met as part of a power cycle operation, the device may enter an indeterminate state. During V_{CC} and V_{CCQ} ramping, both power supplies can ramp at the same time or one after another. When V_{CCQ}=0 V, DQS_t/DQS_c and RE_t/RE_c shall be low. V_{CC} and V_{CCQ} shall be monotonically ramped up from 0V to operating voltage.

The device shall not be powered down during busy period.

5.2. R/B_n Signal Requirements

Ready/Busy is implemented as an open drain circuit, thus a pull-up resistor shall be used for termination. The combination of the pull-up resistor and the capacitive loading of the R/B_n circuit determines the rise time of R/B_n.

5.2.1. Power-on Requirements

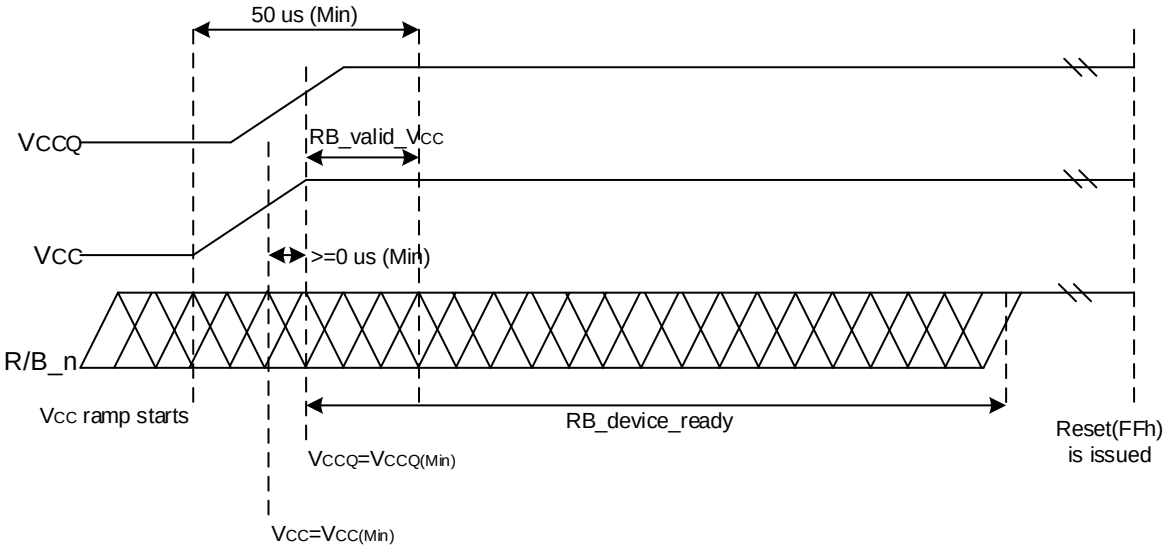
Once V_{CC} and V_{CCQ} reach their minimum values in recommended DC operating conditions and power is stable, the R/B_n signal shall be valid after RB_valid_V_{CC} and shall be set to one (i.e. the state of ready) within RB_device_ready, as listed in the table below. R/B_n is undefined until 50µs has elapsed after V_{CC} has started to ramp. The R/B_n signal is not valid until both of these conditions are met.

Table 56. R/B_n Power-on Requirements

Parameter	Values
RB_valid_V_{CC}	10µs
RB_device_ready	100µs

During V_{CC} and V_{CCQ} ramping, both power supplies can ramp at the same time or one after another. The figure below shows how does V_{CCQ} ramp after V_{CC}, however, they may also ramp at the same time or V_{CCQ} ramp before V_{CC}.

Figure 19. R/B_n Power-on Behavior



5.2.2. Relationship Between R/B_n and SR[6]

R/B_n shall reflect the logical AND of the SR[6] (Status Register Bit6) values for all LUNs on the corresponding NAND target or volume. For example, R/B3_n is the logical AND of the SR[6] values for all LUNs on CE3_n. Thus R/B_n reflects whether any LUN is busy on a particular NAND target.

5.3. Discovery and Initialization

5.3.1. Device Initialization

The procedure below shows how to initialize a device.

1. Power is applied to the device by ramping up V_{CC} and V_{CCQ};
2. R/B_n is pulled low for the device stabilization;
3. The host should not issue any command before R/B_n is pulled high;
4. If the host cannot monitor R/B_n, it should wait for 100µs until the device enters ready;
5. To reset all LUNs in parallel, the host shall issue a Reset (FFh) command. This command is accepted by all LUNs on the same CE_n (i.e. host target);
6. To reset each LUN sequentially for peak power management, then:
   The host shall issue LUN addresses and then Hard Reset (FDh) commands to LUNs one by one;
7. For both parallel and sequential initialization sequences, the host shall issue a Read Status (70h) command and wait until SR[6] is set to one;
8. Read ID, Read Parameter Page and other commands are issued as needed to configure the LUN;
9. For each NAND target connected to the host target, steps 6~8 are repeated for the sequential initialization, while steps 5 and 7~8 are repeated for the parallel initialization;
10. If no more LUNs are discovered on the same CE_n, steps 2~9 shall be repeated for the next CE_n (i.e. host target).

5.3.2. Target Initialization

To initialize a discovered target, the following steps shall be taken. The initialization process should be followed for each connected CE_n signal, including performing the Read Parameter Page command for each target. Each chip enable corresponds to a unique target with its own independent properties that the host shall observe and subsequently use.

The host should issue the Read Parameter Page command. This command returns information that includes the capabilities, features and operating parameters of the device. When the information is read from the device, the host shall check the CRC to ensure that the data was received correctly and without errors prior to taking action on that data.

If the CRC of the first parameter page read is invalid, the host should read redundant parameter page copies. The host can determine whether a redundant parameter page is present by checking if the first four bytes contain at least two bytes of the parameter page signature. If the parameter page signature is present, the host should read the entirety of that redundant parameter page. The host should then check the CRC of that redundant parameter page. If the CRC is correct, the host may take action based on the contents of that redundant parameter page. If the CRC is incorrect, the host should attempt to read the next redundant parameter page through the same procedure.

The host should continue reading redundant parameter pages until the host is able to accurately reconstruct the parameter page contents. All parameter pages returned by the target may have invalid CRC values; however, bit-wise majority or other ECC techniques may be used to recover the contents of the parameter page. The host may use bit-wise majority or other ECC techniques to recover the contents of the parameter page from the parameter page copies present. If the host determines that a parameter page signature is not present, all parameter pages have been read.

After successfully retrieving the parameter page, the host has all information necessary to successfully communicate with that target. If the host has not previously mapped defective block information for this target, the host should then map out all defective blocks in the target. The host may proceed to utilize the target, including during erase and program operations.

5.4. CE_n Signal Requirements

If one or more LUNs are active and the host sets CE_n to one, operations continue running to completion at which point the NAND target enters standby. After the CE_n signal transitions to one, the host may pull a different CE_n signal to zero and begin operations on another NAND target.

When SR[6] for a particular LUN is cleared to zero and the CE_n signal for the corresponding NAND target is pulled low, the host may only issue the Reset, Synchronous Reset, Reset LUN, Read Status, Read Status Enhanced or Volume Select commands to that LUN.

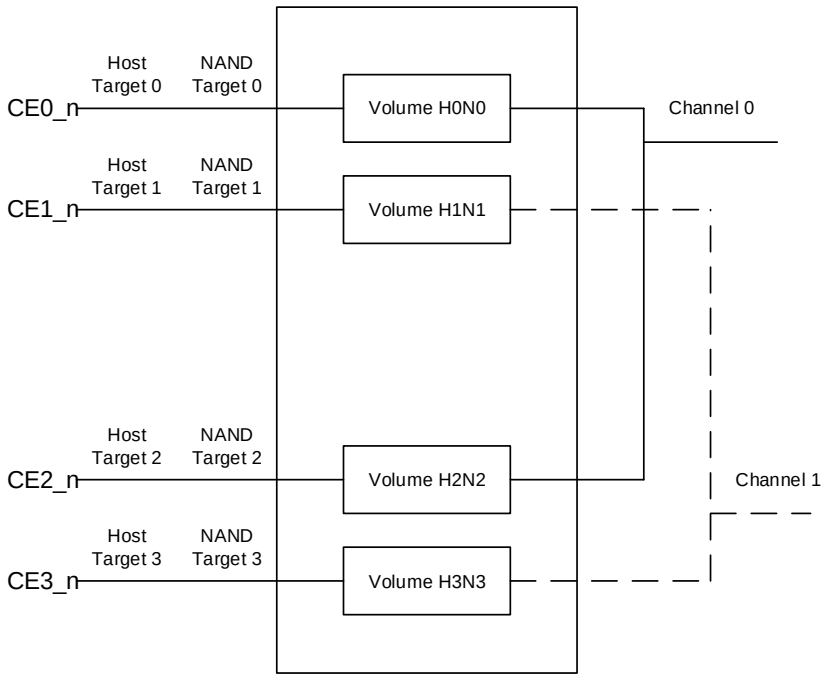
5.4.1. Volume Appointment

The figure below shows an example of how to appoint a volume. If the host wants to have a terminator on a package that does not share a CE_n signal with the selected NAND target, the NAND target that may act as a terminator shall have a volume appointed at initialization by issuing a Set Feature command with the Volume Configuration feature address.

Every CE_n signal shall be individually pulled low and has a unique volume address appointed. Once all NAND targets have their volume addresses appointed, the appointed ones may be used for termination selection.

During operations, the CE_n signals for the selected volume and for the NAND targets acting as terminators shall be pulled low. When CE_n is pulled low for an unselected volume, all LUNs that do not act as terminators for the selected volume are deselected. A Volume Select command should be issued when volume addresses are appointed.

Figure 20. Discrete CE_n per Package Topology



5.5. I/O Interface Requirements

5.5.1. Data Interface Types

The NAND Flash supports three data interface types: SDR, NV-DDR2 and NV-DDR3. The SDR data interface is the traditional NAND interface that uses RE_n to latch data read, WE_n to latch data written, and does not include a clock. The NV-DDR2 and NV-DDR3 data interfaces are double data rate (DDR) and include additional capabilities for scaling speed like ODT and differential signaling. The NV-DDR3 data interface includes all NV-DDR2 features, but operates at V_{CCQ}=1.2V.

If V_{CCQ}=1.8V on power up, the device shall operate in SDR data interface timing mode 0. After the host determines that the NV-DDR2 data interface is supported in the parameter page, the host may select the NV-DDR2 data interface and supported timing mode by using Set Features with a Feature Address of 01h.

If V_{CCQ}=1.2V on power up, the device shall operate in NV-DDR3 interface timing mode 0. After the host determines that the NV-DDR3 timing mode is supported in the parameter page, the host may enable the supported timing mode by transitioning CE_n high and changing the interface speed to the desired timing mode. The new timing mode is active when the host pulls CE_n low.

The NV-DDR2 and NV-DDR3 data interfaces use a DDR protocol. Thus, an even number of bytes is always transferred. The least significant bit of the column address shall always be zero when using the DDR protocol. If the least significant bit of the column address is set to one when using the DDR protocol, then the results are indeterminate.

The following transitions between data interface are supported:

- SDR to NV-DDR2
- NV-DDR2 to SDR

Within any data interface, transitioning between timing modes is supported.

To change the data interface to NV-DDR2, or to change any timing mode, the Set Features command is used with the Timing Mode feature. The Set Features command, Feature Address, and the four parameters are entered using the previously selected timing mode in the previously selected data interface. When issuing the Set Features command, the host shall drive the DQS signal high (if supported by the interface the Set Features command is issued) during the entirety of the command (including parameter entry). After the fourth parameter, P4, is entered until the tITC time has passed, the host shall not issue any commands to the device. After issuing the Set Features command and prior to transitioning CE_n high, the host shall hold signals in an idle cycle state and DQS shall be set to one.

A transition from NV-DDR3 to the other interfaces (SDR or NV-DDR2) is not supported. If VccQ = 1.2V then only the NV-DDR3 interface is supported. To change the Timing Mode for NV-DDR3, the host should transition CE_n high and change the interface speed to the desired timing mode. The new timing mode is

active when the host pulls CE_n low. When changing the NV-DDR3 timing mode, prior to transitioning CE_n high, the host shall hold signals in an Idle bus state and DQS shall be set to one.

Prior to issuing any new commands to the device, the host shall transition CE_n high. The new data interface or timing mode is active when the host pulls CE_n low.

5.5.1.1. SDR Transition from NV-DDR2

To transition from NV-DDR2 to the SDR data interface, the host shall use the Reset command using SDR timing mode 0. A device in any timing mode is required to recognize a Reset command issued in SDR timing mode 0. After the Reset is issued, the host shall not issue any commands to the device until after the tITC time has passed. Note that after the tITC time has passed, only status commands may be issued by the host until the Reset completes. After issuing the Reset and prior to transitioning CE_n high, the host shall hold signals in an idle cycle state and DQS shall be set to one.

After CE_n has been pulled high and then transitioned low again, the host should issue a Set Features to select the appropriate SDR timing mode.

5.5.1.2. NV-DDR2 Recommendations

Prior to selecting the NV-DDR2 data interface, it is recommended that settings for the NV-DDR2 data interface be configured. Specifically:

- Set Features should be used to configure the NV-DDR2 Configuration feature.
- If ODT is used with a more advanced topology, the appropriate ODT Configure commands should be issued.

These actions should be completed prior to selecting the NV-DDR2 data interface. If these settings are modified when the NV-DDR2 data interface is already selected, the host should take care to ensure that appropriate settings are applied in a manner that avoids signal integrity issues.

5.5.1.3. NV-DDR3 Recommendations

Prior to enabling the intended timing mode for the NV-DDR3 data interface, it is recommended that settings for the NV-DDR3 data interface be configured in Timing Mode 0. Specifically:

- Set Features should be used to configure the NV-DDR3 Configuration feature.
- If ODT is used with a more advanced topology, the appropriate ODT Configure commands should be issued.

These actions should be completed prior to enabling a NV-DDR3 Timing Mode other than Timing Mode 0.

5.5.2. Bus States

The table below defines the bus states in the SDR data interface.

Table 57. Bus States in SDR

CE_n	ALE	CLE	WE_n	RE_n	Bus State
1	X	X	X	X	Standby
0	0	0	1	1	Idle
0	0	1	↑	1	Command Cycle
0	1	0	↑	1	Address Cycle
0	0	0	↑	1	Data Input Cycle
0	0	0	1	↓	Data Output Cycle
0	1	1	X	X	Undefined

The table below defines the bus states in the NV-DDR2 and NV-DDR3 data interfaces.

Table 58. Bus States in NV-DDR2/NV-DDR3

CE_n	ALE	CLE	RE_n	DQS	WE_n	Data I/O	Measurement Point	Bus State
1	X	X	X	X	X	X	X	Standby
0	0	0	1	1	1	None	X	Idle
0	0	1	1	-	↑	None	WE_n rising edge to rising edge	Command Cycle
0	1	0	1	-	↑	None	WE_n rising edge to rising edge	Address Cycle
0	0	0	1	↕	1	Input	DQS rising edge to rising edge	Data Input Cycle
0	0	0	↕	↕	1	Output	RE_n rising edge to rising edge	Data Output Cycle

Notes:

1. The current state of the device is data input, data output or neither based on the commands issued;
2. There are two data input/output cycles from the rising edge of DQS/RE_n to the next rising edge of DQS/RE_n;
3. ODT may be enabled as part of the data input and output cycles;
4. At the beginning of a data output burst, DQS shall be held high for tDQSRH after RE_n transitions low to begin data output.

5.5.3. Data I/O Pausing

The host may pause data input or output by entering the state of idle in any data interface.

In the SDR data interface, to pause data input or data output, the value of WE_n or RE_n shall be maintained at one.

In the NV-DDR2 and NV-DDR3 data interfaces, to pause data input or data output, the bus shall be placed in the state of idle. To pause data output only, RE_n (RE_t/RE_c) shall be stopped and held static high or low until the data burst resumes. To pause data input only, DQS (DQS_t/DQS_c) shall be stopped and held static high or low until the data burst resumes. WE_n shall be held high when data input and output bursts pause. Besides, ODT (if enabled) shall be kept enabled during this period, and warmup cycles (if enabled) shall not be reissued when a data bust restarts from stop. If warmup cycles are required, refer to **Section 5.6 "Warmup Cycles"** for details on how to reissue warmup cycles at the time points of exiting and restarting data bursts. To end a data burst after exiting it, the host shall issue a new command.

5.5.4. NV-DDR2/NV-DDR3 and Repeat Bytes

The NV-DDR2 and NV-DDR3 data interfaces adopt the DDR data transfer technique to achieve a high data transfer rate. However, certain commands associated with configuration and settings are seldom used and do not require a high data transfer rate. Besides, these commands typically are not serviced by the pipeline for data transfers.

To avoid unnecessary complexity to implementations of these commands, the data is transferred in the single data rate. Specifically, the same data byte is repeated twice and shall conform to the timings required for the NV-DDR2 or NV-DDR3 data interfaces. The data pattern in these cases is [D0 D0 D1 D1 D2 D2…]. The receiver (host or device) shall only latch one copy of each data byte. Data input or data output shall not be stopped during the execution of these commands. The receiver is not required to wait for the repeated data byte before starting internal actions.

The commands that repeat each data byte twice in the NV-DDR2 and NV-DDR3 data interfaces include Set Features, Read ID, Get Features, Read Status, Read Status Enhanced and ODT Configure. SDR commands may use the highest data transfer rate supported by the device.

5.6. Warmup Cycles

To support higher-speed operations, warmup cycles for data output and data input are provided in the NV-DDR2 and NV-DDR3 data interfaces.

Warmup cycles for data output provide extra RE_n and corresponding DQS transitions at the beginning of a data output burst. These extra RE_n and DQS transitions do not have any data associated with them. The number of extra cycles is configured via the feature address of NV-DDR2/NV-DDR3 Configuration. The number of cycles specified includes a full data output cycle (both rising and falling edges for RE_n and DQS).

Warmup cycles for data input provide extra DQS transitions at the beginning of a data input burst. These extra DQS transitions do not have any data associated with them. The number of extra cycles is configured via the feature address of NV-DDR2/NV-DDR3 Configuration. The number of cycles specified includes a full data input cycle (both rising and falling edges for DQS).

Warmup cycles are optional for both data output and data input, and if used, do not need to be configured to the same value. Warmup cycles apply to all commands, including SDR commands. The warmup cycles shall be initiated at the start of each data burst when warmup cycles are enabled for that data transfer type. If the host stops and then resumes a data transfer without exiting and re-entering the data burst, the host shall not issue additional warmup cycles. Exiting and re-entering the data burst shall be performed by pulling ALE, CLE or CE_n high without latching with WE_n. In the case of not re-issuing warmup cycles, the host should take care to avoid signal integrity issues due to stopping the data transfer and resuming without warmup cycles.

Warmup cycles are active when the selected data interface is NV-DDR2 or NV-DDR3 and warmup cycles are enabled in the NV-DDR2/NV-DDR3 Configuration feature. For NV-DDR2, it is recommended that the NV-DDR2/NV-DDR3 Configuration feature be configured in the SDR data interface. If warmup cycles are enabled while the NV-DDR2 or NV-DDR3 interface is active, warmup cycles shall be used for all subsequent commands after the Set Features command is executed.

Figure 21. Warmup Cycles for Data Output

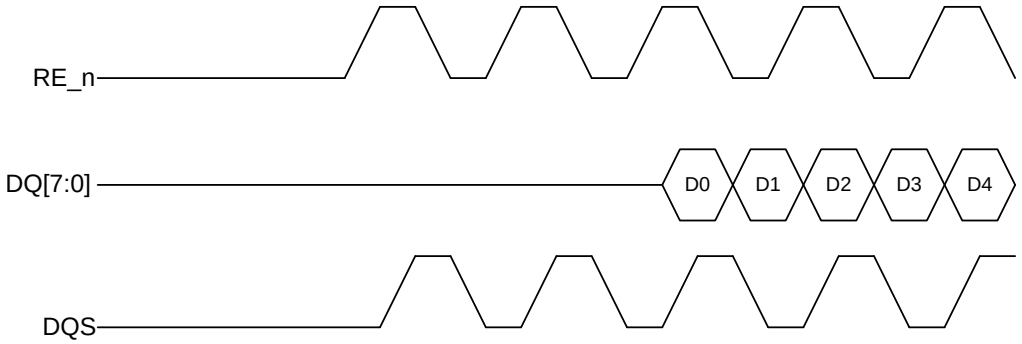
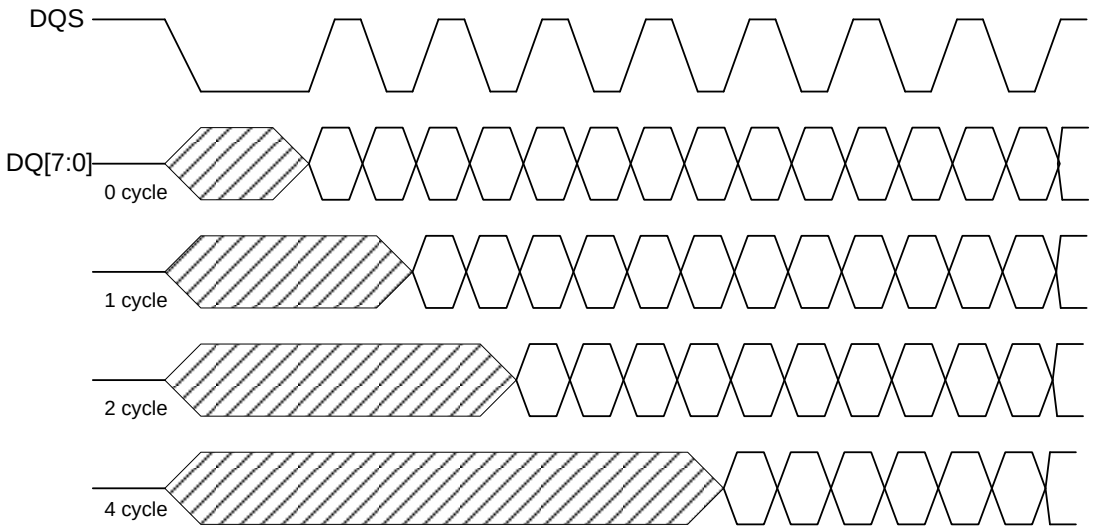


Figure 22. Warmup Cycles for Data Input



5.7. On-die Termination (ODT)

5.7.1. ODT Settings

ODT may be required at higher speeds depending on system topology. This section describes the mechanism for ODT on the DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c signals.

ODT is an optional capability that may be employed to meet higher speeds in particular topologies. If power needs to be optimized in a particular condition, then ODT may be disabled and the topology may potentially need to be run at a slower speed. ODT is supported for the NV-DDR2 and NV-DDR3 data interfaces only.

ODT settings are configured during initialization. The host may configure ODT in a self-termination only configuration, or it may configure a more flexible ODT scheme utilizing matrix termination, which enables a mixture of target and non-target termination to be specified.

For the more flexible ODT configuration, referred to as matrix termination, the host configures a matrix that defines the LUN(s) that terminate for a particular volume. This matrix is configured using the ODT Configure command. For the simple configuration of self-termination only ODT, no ODT matrix configuration is required.

ODT is enabled and disabled based on the type of cycle (on for data input and output cycles, off for command and address cycles). ODT applies for data input and output cycles for all commands.

When ODT is enabled via the NV-DDR2/NV-DDR3 Configuration feature address, the default is self-termination only. To use matrix termination for non-target termination or termination topologies that use multiple terminators, the volume address mechanism shall be used and the ODT configuration matrix shall be specified using the ODT Configure command. If using matrix termination, the ODT Configure command shall be issued to at least one LUN on all NAND Targets. As part of the ODT Configure command, R_{TT} settings may be specified on a per LUN basis with individual values for:

- RE_n R_{TT},
- DQ[7:0] and DQS for data output R_{TT}, and
- DQ[7:0] and DQS for data input R_{TT}.

ODT is disabled when ALE, CLE or CE_n transitions from low to high.

RttEff1, RttEff2, RttEff3, RttEff4, and RttEff5 are determined by separately applying VIH(AC) and VIL(AC) to the ball being tested, and then measuring current I(VIH[AC]) and I(VIL[AC]), respectively. The equation is:

$$RttEff = (VIH[AC] - VIL[AC]) / \{I(VIH[AC]) - I(VIL[AC]\}$$

The measurement voltage (VM) is at the tested ball with no load. The deviation of VM with respect to V_{CCQ} / 2 is defined as:

$$\Delta VM = \{(2 \times VM)/V_{CCQ} - 1\} \times 100$$

Table 59. ODT DC Electrical Characteristics, NV-DDR2/NV-DDR3 Without ZQ Calibration

Parameter	Symbol	Min	Nom	Max	Unit	Optional or Mandatory
Rtt effective Impedance value for 50 Ohms setting	RttEff2	32.5	50	67.5	Ohms	Mandatory
Rtt effective Impedance value for 75 Ohms setting	RttEff3	48.7	75	101.3	Ohms	Mandatory
Rtt effective Impedance value for 100 Ohms setting	RttEff4	65	100	135	Ohms	Mandatory
Rtt effective Impedance value for 150 Ohms setting	RttEff5	97.5	150	202.5	Ohms	Mandatory
Deviation of VM with respect to $V_{CCQ}/2$	ΔVM	-7		7	%	Mandatory

Table 60. ODT DC Electrical Characteristics, NV-DDR2/NV-DDR3 with ZQ Calibration

Parameter	Symbol	Min	Nom	Max	Unit
Rtt effective Impedance value	RttEff	See **Table 61 "Rtt Effective Impedance, NV-DDR2/NV-DRR3 with ZQ Calibration"**			Ohms
Deviation of VM with respect to $V_{CCQ}/2$	ΔVM	-7		7	%

Table 61. Rtt Effective Impedance, NV-DDR2/NV-DRR3 with ZQ Calibration

Rtt	Resistor	V_{OUT} to V_{SSQ}	Maximum	Nominal	Minimum	Unit
Rtt = 50 Ohms						
50 Ohms	R_pulldown	0.2 x V_{CCQ}	1.15	1.0	0.57	RZQ/3
		0.5 x V_{CCQ}	1.15	1.0	0.85	RZQ/3
		0.8 x V_{CCQ}	1.47	1.0	0.85	RZQ/3
	R_pullup	0.2 x V_{CCQ}	1.47	1.0	0.85	RZQ/3
		0.5 x V_{CCQ}	1.15	1.0	0.85	RZQ/3
		0.8 x V_{CCQ}	1.15	1.0	0.57	RZQ/3
50 Ohms		VIL(AC) to VIH(AC)	1.67	1.0	0.85	RZQ/6
Rtt = 75 Ohms						
75 Ohms	R_pulldown	0.2 x V_{CCQ}	1.15	1.0	0.57	RZQ/2
		0.5 x V_{CCQ}	1.15	1.0	0.85	RZQ/2
		0.8 x V_{CCQ}	1.47	1.0	0.85	RZQ/2
	R_pullup	0.2 x V_{CCQ}	1.47	1.0	0.85	RZQ/2
		0.5 x V_{CCQ}	1.15	1.0	0.85	RZQ/2
		0.8 x V_{CCQ}	1.15	1.15	1.0	0.57
75 Ohms		VIL(AC) to VIH(AC)	1.67	1.0	0.85	RZQ/4
Rtt = 100 Ohms						
100 Ohms	R_pulldown	0.2 x V_{CCQ}	1.15	1.0	0.57	RZQ/1.5
		0.5 x V_{CCQ}	1.15	1.0	0.85	RZQ/1.5

Rtt	Resistor	V_{OUT} to V_{SSQ}	Maximum	Nominal	Minimum	Unit
		0.8 x V_{CCQ}	1.47	1.0	0.85	RZQ/1.5
	R_pullup	0.2 x V_{CCQ}	1.47	1.0	0.85	RZQ/1.5
		0.5 x V_{CCQ}	1.15	1.0	0.85	RZQ/1.5
		0.8 x V_{CCQ}	1.15	1.0	0.57	RZQ/1.5
100 Ohms		VIL(AC) to VIH(AC)	1.67	1.0	0.85	RZQ/3
Rtt = 150 Ohms						
150 Ohms	R_pulldown	0.2 x V_{CCQ}	1.15	1.0	0.57	RZQ/1
		0.5 x V_{CCQ}	1.15	1.0	0.85	RZQ/1
		0.8 x V_{CCQ}	1.47	1.0	0.85	RZQ/1
	R_pullup	0.2 x V_{CCQ}	1.47	1.0	0.85	RZQ/1
		0.5 x V_{CCQ}	1.15	1.0	0.85	RZQ/1
		0.8 x V_{CCQ}	1.15	1.0	0.57	RZQ/1
150 Ohms		VIL(AC) to VIH(AC)	1.67	1.0	0.85	RZQ/2

Notes:

1. Tolerance limits assume RZQ of 300Ω +/- 1% and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage
2. Refer to **Section 5.7.2 "ODT Sensitivity"** if either the temperature or the voltage changes after calibration.

5.7.2. ODT Sensitivity

If either the temperature or the voltage changes after ZQ calibration, then the ODT tolerance limits listed in **Table 61 "Rtt Effective Impedance, NV-DDR2/NV-DRR3 with ZQ Calibration"** can be expected to widen according to below two tables.

Table 62. ODT Sensitivity Definition

Description	Minimum	Maximum	Unit
Rtt	0.85 - dRttdT x ΔT - dRttdV x ΔV	1.67 + dRttdT x ΔT + dRttdV x ΔV	RZQ/(2,3,4,6)

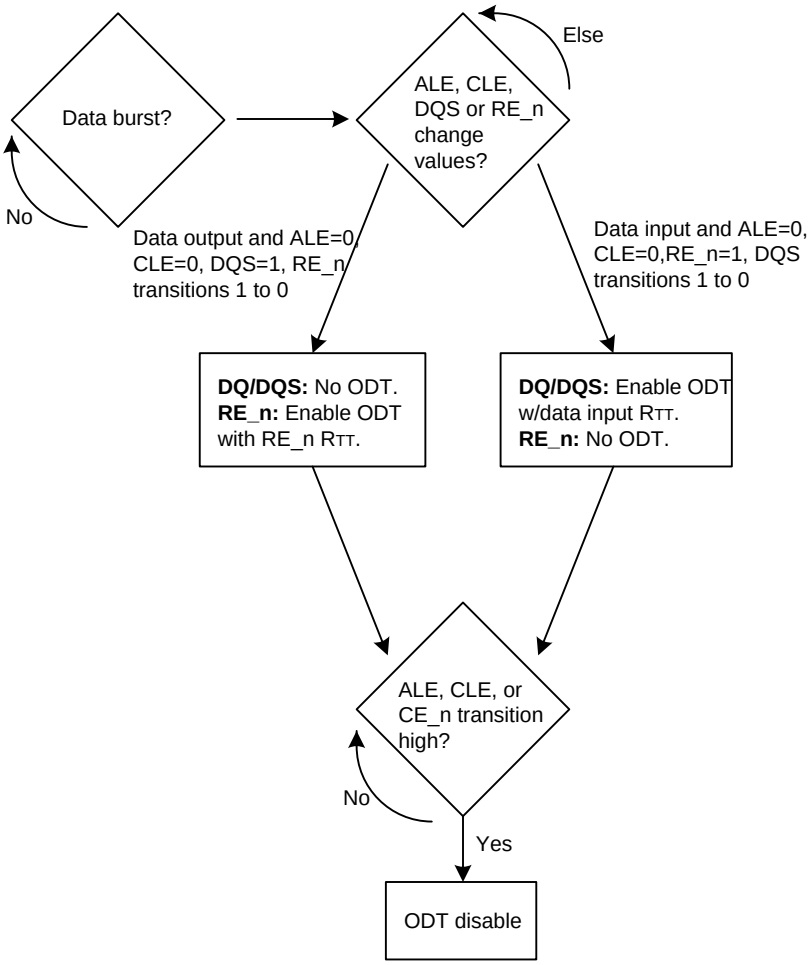
Table 63. ODT Voltage and Temperature Sensitivity

Change	Minimum	Maximum	Unit
dRttdT	0	0.5	%/°C
dRttdV	0	0.2	%/mV

5.7.3. Self-termination ODT

When self-termination is enabled, the LUN that is executing the command provides ODT. The following figure defines self-termination only ODT enable and disable requirements for the LUN that is executing the command when self-termination ODT is enabled. Self-termination ODT is enabled using Set Features with the NV-DDR2/NV-DDR3 Configuration feature. If the ODT Configure command is issued to a LUN on a target, then the ODT mechanism used for that target changes to matrix termination.

Figure 23. Self-termination Only ODT Behavior Flow



5.7.4. Matrix Termination

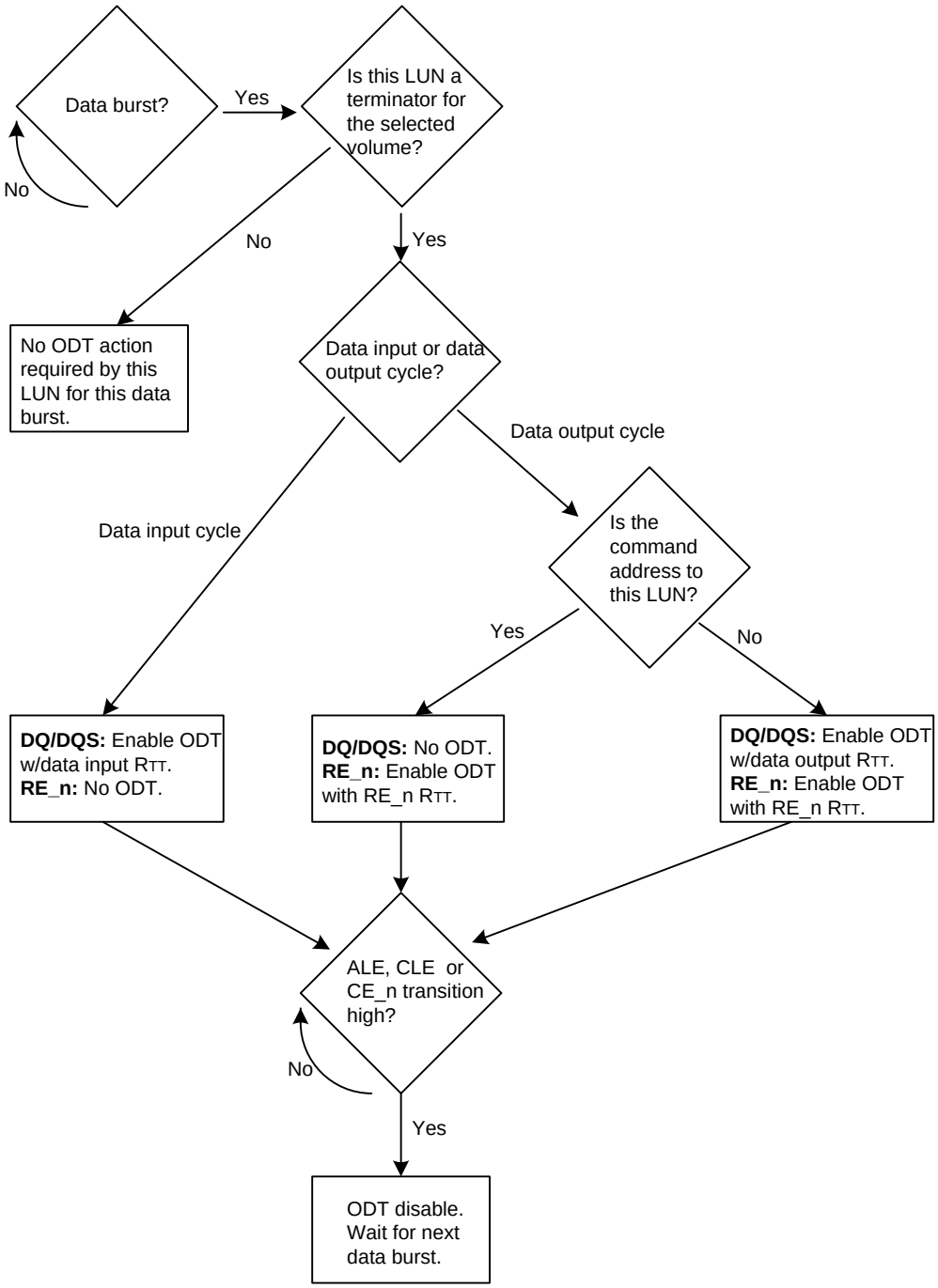
A LUN that is configured to act as a terminator with the configuration matrix that is specified with the ODT Configure command may be located on the same volume as the volume it is terminating for target termination or a separate volume (i.e. non-target termination). Based on the ODT configuration and the volume a command is addressed to, LUNs enter different states listed in the table below. These states determine their ODT behaviors.

Table 64. LUN States for Matrix Termination

LUN is on selected volume?	Terminator for selected volume?	LUN State	ODT Actions Defined
Yes	NA	Selected	Refer to **Figure 24 "ODT Actions for LUNs on Selected Volume"**
No	Yes	Sniff	Refer to **Figure 25 "ODT Actions for LUNs in Sniff on Unselected Volume"**
No	No	Deselected	No ODT action

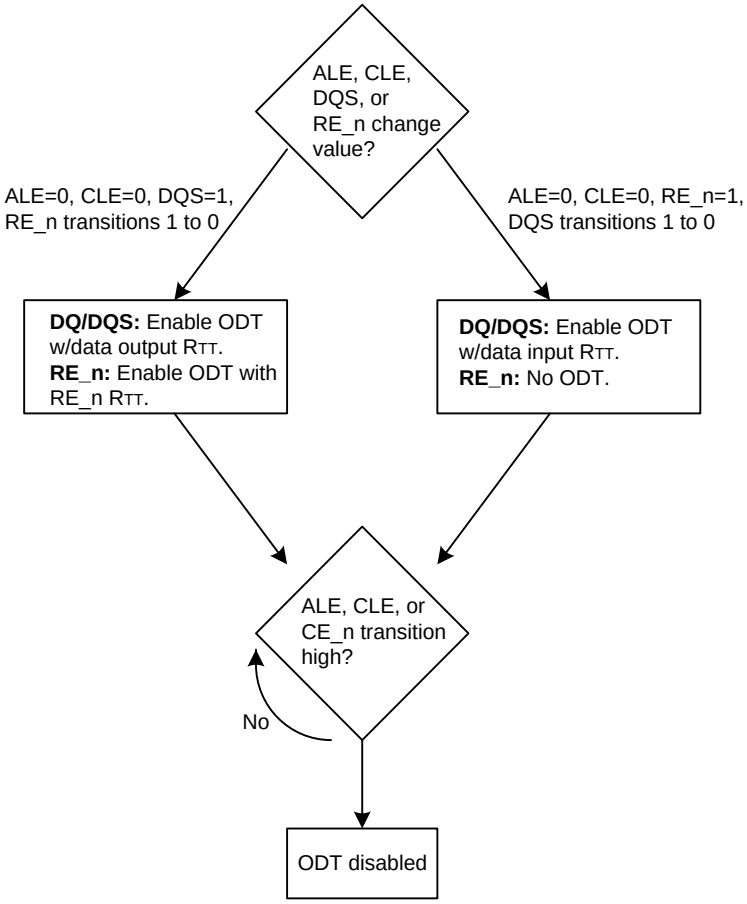
The LUN that a command is addressed to for execution may provide termination. Other LUNs on the selected volume that is not responsible for execution of the command may also provide termination. The figure below defines the ODT actions required for LUNs of each of these types on the selected volume. LUNs on the selected volume remain in an active state, and thus are aware of state information like whether there is a data burst currently and the type of cycle; these LUNs do not rely only on ALE, CLE, DQS and RE_n signals.

Figure 24. ODT Actions for LUNs on Selected Volume



The ODT configuration matrix also offers the flexibility of having LUNs on an unselected volume provide termination for the selected volume. When a LUN is placed in the sniff state, it checks the ALE, CLE, DQS and RE_n signals to determine when to enable or disable ODT. The figure below defines the ODT actions for LUNs in the sniff state on an unselected volume.

Figure 25. ODT Actions for LUNs in Sniff on Unselected Volume

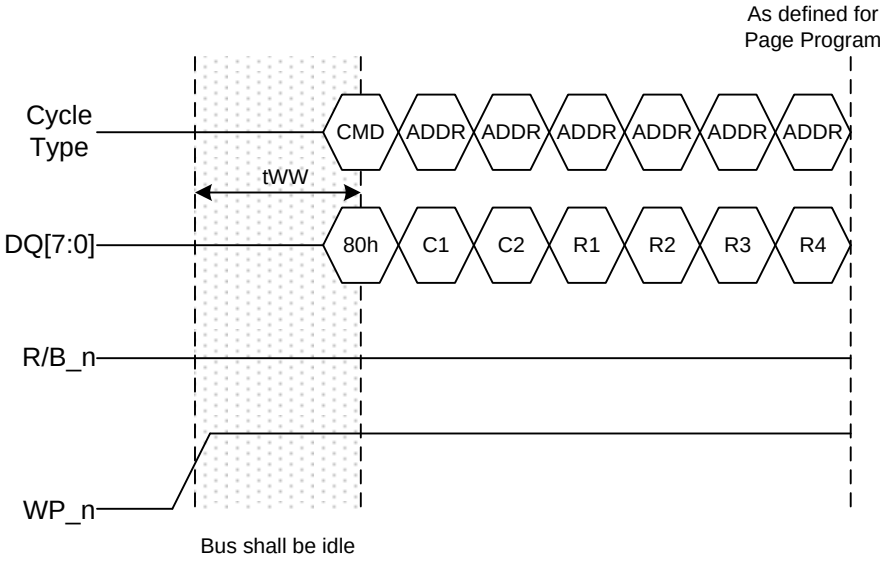


5.8. Write Protection

When cleared to zero, the WP_n signal disables flash array program and erase operations. This signal shall only be transitioned while there are no commands executing on the device. After modifying the value of WP_n, the host shall not issue a new command to the device for at least tWW delay time. If WP_n transitions to low and keeps low during RB_n=0, the ongoing program and erase operations would be aborted and the data in the flash array would not be guaranteed. Read operation would not be affected by WP_n transition.

The figure below describes the tWW timing requirement, shown with the start of a Program command. Before a new command is issued by the host, the bus shall be idle for tWW after WP_n transitions from zero to one or from one to zero.

Figure 26. Write Protect Sequence



5.9. External V_{PP}

This NAND device supports external V_{PP} signal to enhance array operation for the host system by improving power efficiency. V_{PP} shall be maintained within the valid range between 10.8V and 13.2V (typical 12V) while this feature is enabled via Set Features command.

To initialize V_{PP}, follow the procedure:

1. Before starting to ramp V_{PP}, V_{CC} must be successfully ramped.
2. Before issuing the Set Features command to enable V_{PP} feature, V_{PP} shall be ramped to meet its valid range.
3. To disable V_{PP} feature, the Set Features command shall be issued while V_{PP} is within its valid range.
4. Once V_{PP} feature is enabled, V_{PP} shall be maintained to keep the valid range.
5. V_{PP} must go down to 0V before V_{CC} ramping down.

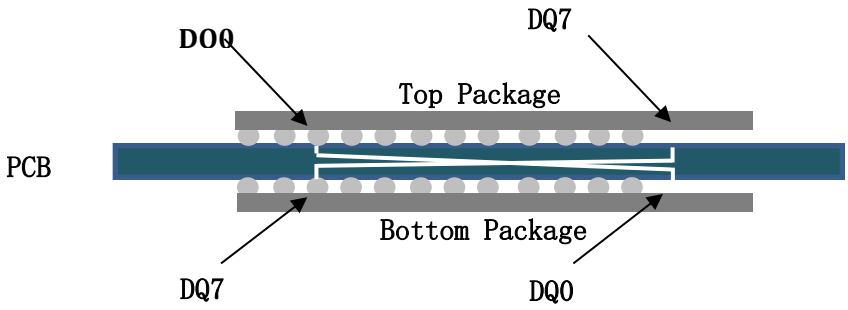
5.10. Electronic Mirroring

This feature supports electronically mirrored DQ[7:0] to optimize two-sided PCB layout. This ability for electronic mirrored DQ[7:0] also assists to reduce the vertical profile of a two-sided system. Only the DQ[7:0] signals can be changed by the electronical mirroring feature. All other signals of NAND remain unchanged.

The devices can be configured to be mirrored or non-mirrored depending on how first Read Status command is decoded after device initialization. The Read Status (70h) command must be issued only once per target after device initialization, to make NAND target correctly do DQ[7:0] mirrored or non-mirrored configuration. If the Read Status command appears as 70h on DQ[7:0], the NAND target should set itself to non-mirrored mode. If the Read Status command appears as 0Eh on DQ[7:0], the NAND target should set itself to mirrored mode. For details on device initialization and electronic mirroring configuration flow chart, refer to **Figure 27 "Example PCB Layout of a Two-Sided System Without Electronic Mirroring of DQ[7:0]"** and **Figure 28 "Example PCB Layout of a Two-Sided System with Electronic Mirroring of DQ[7:0]"**.

The device remains in mirrored mode until power-down. All Reset commands will not change a device from mirrored mode to non-mirrored mode.

Figure 27. Example PCB Layout of a Two-Sided System Without Electronic Mirroring of DQ[7:0]



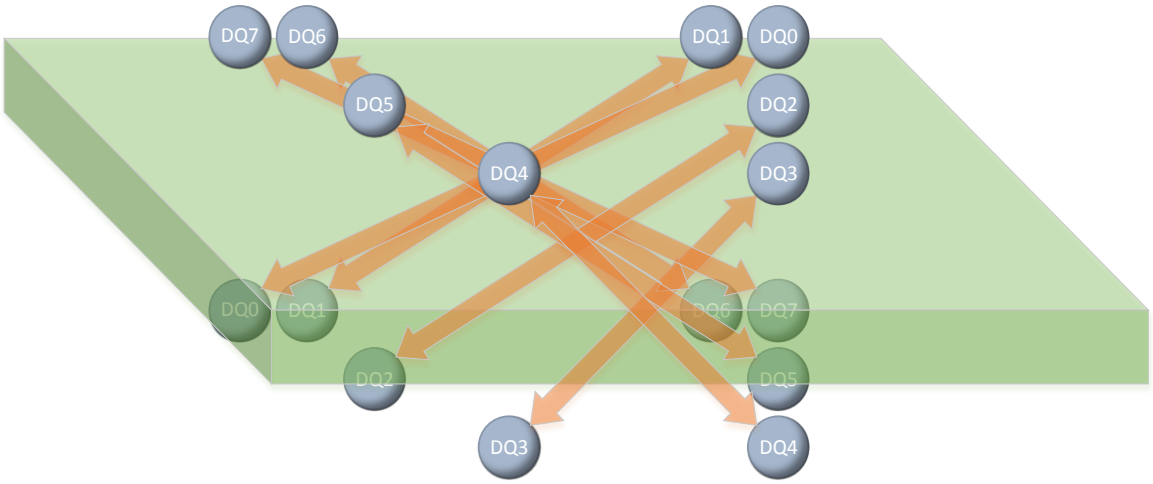
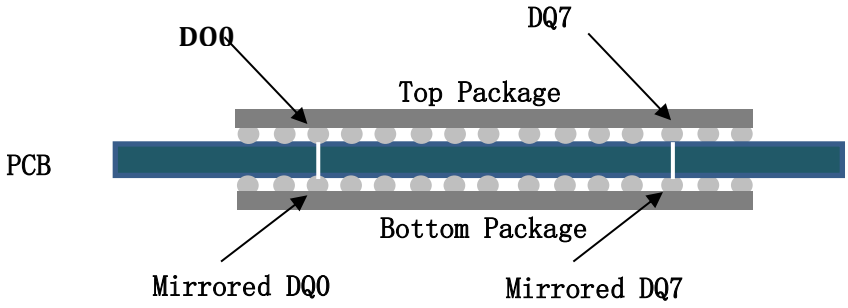
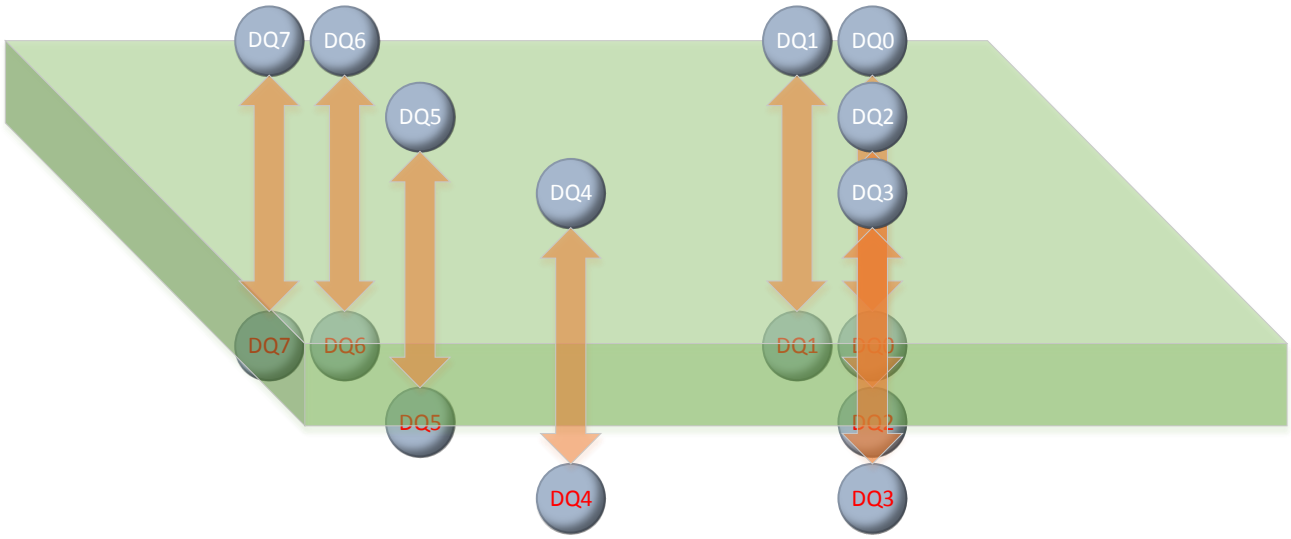


Figure 28. Example PCB Layout of a Two-Sided System with Electronic Mirroring of DQ[7:0]





5.11. Timing Parameters

Table 65. Test Conditions for AC Timing Parameters

Parameter	Value (SDR)	Value (NV-DDR2, Single-Ended)	Value (NV-DDR2, Differential)	Value (NV-DDR3, Single-Ended)	Value (NV-DDR3, Differential)
Positive input transition	$V_{IL(DC)}$ to $V_{IH(AC)}$	$V_{IL(DC)}$ to $V_{IH(AC)}$	$V_{ILdiff(DC)}$ to $V_{IHdiff(AC)}$	$V_{IL(DC)}$ to $V_{IH(AC)}$	$V_{ILdiff(DC)}$ to $V_{IHdiff(AC)}$
Negative input transition	$V_{IH(DC)}$ to $V_{IL(AC)}$	$V_{IH(DC)}$ to $V_{IL(AC)}$	$V_{IHdiff(DC)}$ to $V_{ILdiff(AC)}$	$V_{IH(DC)}$ to $V_{IL(AC)}$	$V_{IHdiff(DC)}$ to $V_{ILdiff(AC)}$
Input rise and fall slew rate	1 V/ns	1 V/ns	2 V/ns	1 V/ns	2 V/ns
Input timing level	$V_{CCQ}/2$	V_{REFQ}	$V_{IX(AC)}$	V_{REFQ}	$V_{IX(AC)}$
Output timing level	$V_{CCQ}/2$	V_{TT}	$V_{OX(AC)}$	V_{TT}	$V_{OX(AC)}$
Output capacitance load	5pF	5pF	5pF	5pF	5pF

Table 66. AC Characteristics (SDR)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Clock period	-	100		50		35		30		25		20		ns
Frequency	-	10		20		28		33		40		50		MHz
Address cycle to data loading time	tADL	300	-	300	-	300	-	300	-	300	-	300	-	ns
ALE hold time	tALH	20	-	10	-	10	-	5	-	5	-	5	-	ns
ALE setup time	tALS	50	-	25	-	15	-	10	-	10	-	10	-	ns
ALE to RE_n delay	tAR	25	-	10	-	10	-	10	-	10	-	10	-	ns
CE_n access time	tCEA	-	100	-	45	-	30	-	25	-	25	-	25	ns
CE_n HIGH hold time	tCEH	20	-	20	-	20	-	20	-	20	-	20	-	ns
CE_n hold time	tCH	20	-	10	-	10	-	5	-	5	-	5	-	ns

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Delay prior to bringing CE_n high after a new Volume is selected using the Volume Select command	tCEVDLY	50	-	50	-	50	-	50	-	50	-	50	-	ns
CE_n HIGH to output High-Z	tCHZ	-	100	-	50	-	50		50	-	30	-	30	ns
CE_n setup time	tCS	70	-	35	-	25	-	25	-	20	-	15	-	ns
CE_n HIGH to output hold	tCOH	0	-	15	-	15	-	15	-	15	-	15	-	ns
CE_n to RE_n LOW	tCR	10	-	10	-	10	-	10	-	10	-	10	-	ns
CE_n to RE_n low after CE_n has been high for greater than 1us	tCR2	100	-	100	-	100	-	100	-	100	-	100	-	ns
CE_n to RE_n low after CE_n has been high for greater than 1us during read ID	tCR2	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	ns
CLE hold time	tCLH	20	-	10	-	10	-	5	-	5	-	5	-	ns
CLE to RE_n delay	tCLR	20	-	10	-	10	-	10	-	10	-	10	-	ns
CLE setup time	tCLS	50	-	25	-	15	-	10	-	10	-	10	-	ns
Data hold time	tDH	20	-	10	-	5	-	5	-	5	-	5	-	ns
Data setup time	tDS	40	-	20	-	15	-	10	-	10	-	7	-	ns
Output High-Z to RE_n LOW	tIR	10	-	0	-	0	-	0	-	0	-	0	-	ns
RE_n cycle time	tRC	100	-	50	-	35	-	30	-	25	-	20	-	ns
RE_n access time	tREA	-	40	-	30	-	25	-	20	-	20	-	16	ns
RE_n HIGH hold time	tREH	30	-	15	-	15	-	10	-	10	-	7	-	ns
RE_n HIGH to output hold	tRHOH	0	-	15	-	15	-	15	-	15	-	15	-	ns
RE_n HIGH to WE_n LOW	tRHW	200	-	100	-	100	-	100	-	100	-	100	-	ns
RE_n LOW to output hold	tRLOH	0	-	0	-	0	-	0	-	5	-	5	-	ns

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
RE_n HIGH to output High-Z	tRHZ	-	200	-	100	-	100	-	100	-	100	-	100	ns
RE_n pulse width	tRP	50	-	25	-	17	-	15	-	12	-	10	-	ns
Ready to data output cycle (data only)	tRR	40	-	20	-	20	-	20	-	20	-	20	-	ns
WE_n HIGH to R/B_n LOW	tWB	-	200	-	100	-	100	-	100	-	100	-	100	ns
WE_n cycle time	tWC	100	-	45	-	35	-	30	-	25	-	20	-	ns
WE_n HIGH hold time	tWH	30	-	15	-	15	-	10	-	10	-	7	-	ns
Command, address, or data input cycle to data output cycle (RE_n low)	tWHR	120	-	80	-	80	-	80	-	80	-	80	-	ns
WE_n pulse width	tWP	50	-	25	-	17	-	15	-	12	-	10	-	ns
WP_n transition to command cycle (WE_n low)	tWW	100	-	100	-	100	-	100	-	100	-	100	-	ns
Delay prior to issuing the next command after a new Volume is selected using the Volume Select command	tVDLY	50	-	50	-	50	-	50	-	50	-	50	-	ns
Device RESET time (READ/PROGRAM/ ERASE)	tRST	-	5000	-	15/30/500	-	15/30/500	-	15/30/500	-	15/30/500	-	15/30/500	µs

Table 67. AC Characteristics (NV-DDR2/NV-DDR3) for Modes 0-4

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Clock period	-	30		25		15		12		10		ns
Frequency	-	33		40		66		83		100		Mhz
Command and Address												
Address cycle to data loading time	tADL	300	-	300	-	300	-	300	-	300	-	ns
ALE to (RE_n low or RE_t/RE_c crosspoint)	tAR	10	-	10	-	10	-	10	-	10	-	ns
Command/address DQ hold time	tCAH	5	-	5	-	5	-	5	-	5	-	ns
Command/address DQ setup time	tCAS	5	-	5	-	5		5	-	5	-	ns
CLE and ALE hold time	tCALH	5	-	5	-	5	-	5	-	5	-	ns
CLE and ALE setup time	tCALS	15	-	15	-	15	-	15	-	15	-	ns
CLE and ALE setup time when ODT is enabled	tCALS2	25	-	25	-	25	-	25	-	25	-	ns
CE_n HIGH hold time	tCEH	20	-	20	-	20	-	20	-	20	-	ns
CE_n hold time	tCH	5	-	5	-	5	-	5	-	5	-	ns
CE_n setup time	tCS	20	-	20	-	20	-	20	-	20	-	ns
CE_n setup time for data burst with ODT disabled	tCS1	30	-	30	-	30	-	30	-	30	-	ns
CE_n setup time with DQS/DQ[7:0] ODT enabled	tCS2	40	-	40	-	40	-	40	-	40	-	ns
ALE, CLE, WE_n hold time for CE_n HIGH	tCSD	10	-	10	-	10	-	10	-	10	-	ns
CE_n HIGH to output High-Z	tCHZ	-	30	-	30	-	03	-	30	-	30	ns
CE_n HIGH to output hold	tCOH	15	-	15	-	15	-	15	-	15	-	ns
CLE HIGH to output High-Z	tCLHZ	-	30	-	30	-	30	-	30	-	30	ns

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
CLE to (RE_n low or RE_t/RE_c crosspoint)	tCLR	10	-	10	-	10	-	10	-	10	-	ns
CE_n to (RE_n low or RE_t/RE_c crosspoint)	tCR	10	-	10	-	10	-	10	-	10	-	ns
CE_n to (RE_n low or RE_t/RE_c crosspoint) after CE_n has been high for greater than 1us	tCR2	100	-	100	-	100	-	100	-	100	-	ns
DQS (DQS_t) HIGH and RE_n (RE_t) HIGH setup to ALE, CLE and CE_n LOW during data burst	tDBS	5	-	5	-	5	-	5	-	5	-	ns
RE_n (RE_t) HIGH to WE_n LOW	tRHW	100	-	100	-	100	-	100	-	100	-	ns
WE_n HIGH to R/B_n LOW	tWB	-	100	-	100	-	100	-	100	-	100	ns
Write cycle time	tWC	25	-	25	-	25	-	25	-	25	-	ns
WE_n HIGH pulse width	tWH	11	-	11	-	11	-	11	-	11	-	ns
Command, address, or data input cycle to data output cycle (RE_n low)	tWHR	80	-	80	-	80	-	80	-	80	-	ns
WE_n LOW pulse width	tWP	11	-	11	-	11	-	11	-	11	-	ns
WP_n transition to command cycle (WE_n low)	tWW	100	-	100	-	100	-	100	-	100	-	ns
Ready to data output cycle (data only)	tRR	20	-	20	-	20	-	20	-	20	-	ns
Device RESET time (READ/PROGRAM/ERASE)	tRST	-	15/30/500	-	15/30/500	-	15/30/500	-	15/30/500	-	15/30/500	µs
Data Input												

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
DQS setup time for data input start	tCDQSS	30	-	30	-	30	-	30	-	30	-	ns
DQS hold time for data input end	tCDQSH	100	-	100	-	100	-	100	-	100	-	ns
DQ input pulse width	tDIPW	0.31	-	0.31	-	0.31	-	0.31	-	0.31	-	tDSC(avg)
DQS HIGH level width	tDQSH	0.43	-	0.43	-	0.43	-	0.43	-	0.43	-	tDSC(avg)
DQS LOW level width	tDQSL	0.43	-	0.43	-	0.43	-	0.43	-	0.43	-	tDSC(avg)
Average DQS cycle time	tDSC(avg)	30	-	25	-	15	-	12	-	10	-	ns
Absolute write cycle period	tDSC(abs)	Min: tDSC(AVG) + tJITper(DQS) (min) Max: tDSC(AVG) + tJITper(DQS) (max)										ns
DQS write preamble	tWPRE	15	-	15	-	15	-	15	-	15	-	ns
DQS write preamble when ODT enabled	tWPRE2	25	-	25	-	25	-	25	-	25	-	ns
DQS write postamble	tWPST	6.5	-	6.5	-	6.5	-	6.5	-	6.5	-	ns
DQS write postamble hold time	tWPSTH	15	-	15	-	15	-	15	-	15	-	ns
Data hold time	tDH	4	-	3.3	-	2.0	-	1.1	-	-	-	ns
Data hold time tight timing	tDH_tight	-	-	-	-	-	-	-	-	0.7	-	ns
Data hold time relaxed timing	tDH_relaxed	-	-	-	-	-	-	-	-	0.9	-	ns
Data setup time	tDS	4	-	3.3	-	2.0	-	1.1	-	-	-	ns
Data DQ setup time tight timing	tDS_tight	-	-	-	-	-	-	-	-	0.7	-	ns
Data DQ setup time relaxed timing	tDS_relaxed	-	-	-	-	-	-	-	-	0.9	-	ns
Data Output												
Access window of DQ[7:0] from RE_n (RE_t/RE_c cross-point)	tAC	3	25	3	25	3	25	3	25	3	25	ns
(RE_n low or RE_t/RE_c crosspoint) to	tDQSD	5	18	5	18	5	18	5	18	5	18	ns

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
DQS/DQ driven by device												
DQS-DQ skew (DQS to last DQ valid, per access)	tDQSQ	-	2.5	-	2.0	-	1.4	-	1.0	-	0.8	ns
Access window of DQS from RE_n (RE_t/RE_c)	tDQSRE	3	25	3	25	3	25	3	25	3	25	ns
DQS hold time after (RE_n low or RE_t/RE_c crosspoint)	tDQSRH	5	-	5	-	5	-	5	-	5	-	ns
Output data valid window	tDVW	Min: tQH - tDQSQ Max: tQH – tDQSQ										ns
DQ-DQS hold (DQS to first DQ to go invalid, per access)	tQH	0.37	-	0.37	-	0.37	-	0.37	-	0.37	-	tRC(avg)
DQS output HIGH time (if differential, DQS_t is high)	tQSH	0.37	-	0.37	-	0.37	-	0.37	-	0.37	-	tRC(avg)
DQS output LOW time (if differential, DQS_t is low)	tQSL	0.37	-	0.37	-	0.37	-	0.37	-	0.37	-	tRC(avg)
Average read cycle time	tRC(avg)	30	-	25	-	15	-	12	-	10	-	ns
Absolute read cycle period	tRC(abs)	Min: tRC(AVG) + tJITper(RE_n) (min) Max: tRC(AVG) + tJITper(RE_n) (max)										ns
Average RE_n (RE_t) HIGH width	tREH(avg)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
Absolute RE_n (RE_t) HIGH width	tREH(abs)	0.43	-	0.43	-	0.43	-	0.43	-	0.43	-	tRC(avg)
Average RE_n (RE_t) LOW width	tRP(avg)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
Absolute RE_n (RE_t) LOW width	tRP(abs)	0.43	-	0.43	-	0.43	-	0.43	-	0.43	-	tRC(avg)
Read preamble	tRPRE	15	-	15	-	15	-	15	-	15	-	ns
Read preamble with ODT enabled	tRPRE2	25	-	25	-	25	-	25	-	25	-	ns

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read postamble	tRPST	Min: tDQSRE + 0.5*tRC						Max: -				ns
Read postamble hold time	tRPSTH	15	-	15	-	15	-	15	-	15	-	ns
Jitter												
The deviation of a given tDQS(abs)/tDSC(abs) from a tDQS(avg)/tDSC(avg)	tJITper(DQS)	-2.4	2.4	-2.0	2.0	-1.2	1.2	-1.0	1.0	-0.8	0.8	ns
The deviation of a given tRC(abs)/tDSC(abs) from a tRC(avg)/tDSC(avg)	tJITper(RE_n)	-1.8	1.8	-1.5	1.5	-0.9	0.9	-0.75	0.75	-0.6	0.6	ns
Cycle to cycle jitter for DQS	tJITcc(DQS)	4.8	-	4.0	-	2.4	-	2.0	-	1.6	-	ns
Cycle to cycle jitter for RE_n	tJITcc(RE_n)	3.6	-	3.0	-	1.8	-	1.5	-	1.2	-	ns
Volume Addressing												
Delay prior to bringing CE_n high after a new Volume is selected using the Volume Select command	tCEVDLY	50	-	50	-	50	-	50	-	50	-	ns
Delay prior to issuing the next command after a new Volume is selected using the Volume Select command	tVDLY	50	-	50	-	50	-	50	-	50	-	ns

Table 68. AC Characteristics (NV-DDR2/NV-DDR3) for Modes 5-8

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Mode 8		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock period	-	7.5		6		5		3.75		ns
Frequency	-	133		166		200		267		Mhz
Command and Address										
Address cycle to data loading time	tADL	300	-	300	-	300	-	300	-	ns
ALE to (RE_n low or RE_t/RE_c crosspoint)	tAR	10	-	10	-	10	-	10	-	ns
Command/address DQ hold time	tCAH	5	-	5	-	5	-	5	-	ns
Command/address DQ setup time	tCAS	5	-	5	-	5		5	-	ns
CLE and ALE hold time	tCALH	5	-	5	-	5	-	5	-	ns
CLE and ALE setup time	tCALS	15	-	15	-	15	-	15	-	ns
CLE and ALE setup time when ODT is enabled	tCALS2	25	-	25	-	25	-	25	-	ns
CE_n HIGH hold time	tCEH	20	-	20	-	20	-	20	-	ns
CE_n hold time	tCH	5	-	5	-	5	-	5	-	ns
CE_n setup time	tCS	20	-	20	-	20	-	20	-	ns
CE_n setup time for data burst with ODT disabled	tCS1	30	-	30	-	30	-	30	-	ns
CE_n setup time with DQS/DQ[7:0] ODT enabled	tCS2	40	-	40	-	40	-	40	-	ns
ALE, CLE, WE_n hold time for CE_n HIGH	tCSD	10	-	10	-	10	-	10	-	ns
CE_n HIGH to output High-Z	tCHZ	-	30	-	30	-	30	-	30	ns
CE_n HIGH to output hold	tCOH	15	-	15	-	15	-	15	-	ns
CLE HIGH to output High-Z	tCLHZ	-	30	-	30	-	30	-	30	ns
CLE to (RE_n low or RE_t/RE_c crosspoint)	tCLR	10	-	10	-	10	-	10	-	ns

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Mode 8		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
CE_n to (RE_n low or RE_t/RE_c crosspoint)	tCR	10	-	10	-	10	-	10	-	ns
CE_n to (RE_n low or RE_t/RE_c crosspoint) after CE_n has been high for greater than 1us	tCR2	100	-	100	-	100	-	100	-	ns
DQS (DQS_t) HIGH and RE_n (RE_t) HIGH setup to ALE, CLE and CE_n LOW during data burst	tDBS	5	-	5	-	5	-	5	-	ns
RE_n (RE_t) HIGH to WE_n LOW	tRHW	100	-	100	-	100	-	100	-	ns
WE_n HIGH to R/B_n LOW	tWB	-	100	-	100	-	100	-	100	ns
Write cycle time	tWC	25	-	25	-	25	-	25	-	ns
WE_n HIGH pulse width	tWH	11	-	11	-	11	-	11	-	ns
Command, address, or data input cycle to data output cycle (RE_n low)	tWHR	80	-	80	-	80	-	80	-	ns
WE_n LOW pulse width	tWP	11	-	11	-	11	-	11	-	ns
WP_n transition to command cycle (WE_n low)	tWW	100	-	100	-	100	-	100	-	ns
Ready to data output cycle (data only)	tRR	20	-	20	-	20	-	20	-	ns
Device RESET time (READ/PROGRAM/ERASE)	tRST	-	15/30/500	-	15/30/500	-	15/30/500	-	15/30/500	µs
Data Input										
DQS setup time for data input start	tCDQSS	30	-	30	-	30	-	30	-	ns
DQS hold time for data input end	tCDQSH	100	-	100	-	100	-	100	-	ns

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Mode 8		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
DQ input pulse width	tDIPW	0.31	-	0.31	-	0.31	-	0.31	-	tDSC(avg)
DQS HIGH level width	tDQSH	0.43	-	0.43	-	0.43	-	0.43	-	tDSC(avg)
DQS LOW level width	tDQSL	0.43	-	0.43	-	0.43	-	0.43	-	tDSC(avg)
Average DQS cycle time	tDSC(avg)	7.5	-	6	-	5	-	3.75	-	ns
Absolute write cycle period	tDSC(abs)	Min: tDSC(AVG) + tJITper(DQS) (min) Max: tDSC(AVG) + tJITper(DQS) (max)								ns
DQS write preamble	tWPRE	15	-	15	-	15	-	15	-	ns
DQS write preamble when ODT enabled	tWPRE2	25	-	25	-	25	-	25	-	ns
DQS write postamble	tWPST	6.5	-	6.5	-	6.5	-	6.5	-	ns
DQS write postamble hold time	tWPSTH	15	-	15	-	15	-	15	-	ns
Data hold time	tDH	-	-	-	-	-	-	-	-	ns
Data hold time tight timing	tDH_tight	0.5	-	0.4	-	0.35	-	0.3	-	ns
Data hold time relaxed timing	tDH_relaxed	0.75	-	0.55	-	0.4	-	0.35	-	ns
Data setup time	tDS	-	-	-	-	-	-	-	-	ns
Data DQ setup time tight timing	tDS_tight	0.5	-	0.4	-	0.35	-	0.3	-	ns
Data DQ setup time relaxed timing	tDS_relaxed	0.75	-	0.55	-	0.4	-	0.35	-	ns
Data Output										
Access window of DQ[7:0] from RE_n (RE_t/RE_c cross-point)	tAC	3	25	3	25	3	25	3	25	ns
(RE_n low or RE_t/RE_c crosspoint) to DQS/DQ driven by device	tDQSD	5	18	5	18	5	18	5	18	ns
DQS-DQ skew (DQS to last DQ valid, per access)	tDQSQ	-	0.6	-	0.5	-	0.4	-	0.35	ns

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Mode 8		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Access window of DQS from RE_n (RE_t/RE_c)	tDQSRE	3	25	3	25	3	25	3	25	ns
DQS hold time after (RE_n low or RE_t/RE_c crosspoint)	tDQSRH	5	-	5	-	5	-	5	-	ns
Output data valid window	tDVW	Min: tQH - tDQSQ Max: tQH – tDQSQ								ns
DQ-DQS hold (DQS to first DQ to go invalid, per access)	tQH	0.37	-	0.37	-	0.37	-	0.37	-	tRC(avg)
DQS output HIGH time (if differential, DQS_t is high)	tQSH	0.37	-	0.37	-	0.37	-	0.37	-	tRC(avg)
DQS output LOW time (if differential, DQS_t is low)	tQSL	0.37	-	0.37	-	0.37	-	0.37	-	tRC(avg)
Average read cycle time	tRC(avg)	7.5	-	6	-	5	-	3.75	-	ns
Absolute read cycle period	tRC(abs)	Min: tRC(AVG) + tJITper(RE_n) (min) Max: tRC(AVG) + tJITper(RE_n) (max)								ns
Average RE_n (RE_t) HIGH width	tREH(avg)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
Absolute RE_n (RE_t) HIGH width	tREH(abs)	0.43	-	0.43	-	0.43	-	0.43	-	tRC(avg)
Average RE_n (RE_t) LOW width	tRP(avg)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC(avg)
Absolute RE_n (RE_t) LOW width	tRP(abs)	0.43	-	0.43	-	0.43	-	0.43	-	tRC(avg)
Read preamble	tRPRE	15	-	15	-	15	-	15	-	ns
Read preamble with ODT enabled	tRPRE2	25	-	25	-	25	-	25	-	ns
Read postamble	tRPST	Min: tDQSRE + 0.5*tRC				Max: -				ns
Read postamble hold time	tRPSTH	15	-	15	-	15	-	15	-	ns
Jitter										
The deviation of a given tDQS(abs)/tDSC(abs)	tJITper(DQS)	-0.6	0.6	-0.48	0.48	-0.4	0.4	-0.3	0.3	ns

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Mode 8		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
from a tDQS(avg)/tDSC(avg)										
The deviation of a given tRC(abs)/tDSC(abs) from a tRC(avg)/tDSC(avg)	tJITper(RE_n)	-0.45	0.45	-0.36	0.36	-0.3	0.3	-0.225	0.225	ns
Cycle to cycle jitter for DQS	tJITcc(DQS)	1.2	-	0.96	-	0.8	-	0.6	-	ns
Cycle to cycle jitter for RE_n	tJITcc(RE_n)	0.9	-	0.72	-	0.6	-	0.45	-	ns
Volume Addressing										
Delay prior to bringing CE_n high after a new Volume is selected using the Volume Select command	tCEVDLY	50	-	50	-	50	-	50	-	ns
Delay prior to issuing the next command after a new Volume is selected using the Volume Select command	tVDLY	50	-	50	-	50	-	50	-	ns

Table 69. AC Characteristics (NV-DDR3) for Modes9- 10

Parameter	Symbol	Mode 9		Mode 10		Unit
		Min	Max	Min	Max	
Clock period	-	3		2.5		ns
Frequency	-	333		400		MHz
Command and Address						
Address cycle to data loading time	tADL	300	-	300	-	ns
ALE to (RE_n low or RE_t/RE_c crosspoint)	tAR	10	-	10	-	ns
Command/address DQ hold time	tCAH	5	-	5	-	ns

Command/address DQ setup time	tCAS	5	-	5	-	ns
CLE and ALE hold time	tCALH	5	-	5	-	ns
CLE and ALE setup time	tCALS	15	-	15	-	ns
CLE and ALE setup time when ODT is enabled	tCALS2	25	-	25	-	ns
CE_n HIGH hold time	tCEH	20	-	20	-	ns
CE_n hold time	tCH	5	-	5	-	ns
CE_n setup time	tCS	20	-	20	-	ns
CE_n setup time for data burst with ODT disabled	tCS1	30	-	30	-	ns
CE_n setup time with DQS/DQ[7:0] ODT enabled	tCS2	40	-	40	-	ns
ALE, CLE, WE_n hold time for CE_n HIGH	tCSD	10	-	10	-	ns
CE_n HIGH to output High-Z	tCHZ	-	30	-	30	ns
CE_n HIGH to output hold	tCOH	15	-	15	-	ns
CLE HIGH to output High-Z	tCLHZ	-	30	-	30	ns
CLE to (RE_n low or RE_t/RE_c crosspoint)	tCLR	10	-	10	-	ns
CE_n to (RE_n low or RE_t/RE_c crosspoint)	tCR	10	-	10	-	ns
CE_n to (RE_n low or RE_t/RE_c crosspoint) after CE_n has been high for greater than 1us	tCR2	100	-	100	-	ns
DQS (DQS_t) HIGH and RE_n (RE_t) HIGH setup to ALE, CLE and CE_n LOW during data burst	tDBS	5	-	5	-	ns
RE_n (RE_t) HIGH to WE_n LOW	tRHW	100	-	100	-	ns
WE_n HIGH to R/B_n LOW	tWB	-	100	-	100	ns
Write cycle time	tWC	25	-	25	-	ns
WE_n HIGH pulse width	tWH	11	-	11	-	ns
Command, address, or data input cycle to data output cycle (RE_n low)	tWHR	80	-	80	-	ns
WE_n LOW pulse width	tWP	11	-	11	-	ns
WP_n transition to command cycle (WE_n low)	tWW	100	-	100	-	ns

Ready to data output cycle (data only)	tRR	20	-	20	-	ns
Device RESET time (READ/PROGRAM/ERASE)	tRST	-	15/30/500	-	15/30/500	µs
Data Input						
DQS setup time for data input start	tCDQSS	30	-	30	-	ns
DQS hold time for data input end	tCDQSH	100	-	100	-	ns
DQ input pulse width	tDIPW	0.31	-	0.31	-	tDSC(avg)
DQS HIGH level width	tDQSH	0.43	-	0.43	-	tDSC(avg)
DQS LOW level width	tDQSL	0.43	-	0.43	-	tDSC(avg)
Average DQS cycle time	tDSC(avg)	3	-	2.5	-	ns
Absolute write cycle period	tDSC(abs)	Min: tDSC(AVG) + tJITper(DQS) (min) Max: tDSC(AVG) + tJITper(DQS) (max)				ns
DQS write preamble	tWPRE	15	-	15	-	ns
DQS write preamble when ODT enabled	tWPRE2	25	-	25	-	ns
DQS write postamble	tWPST	6.5	-	6.5	-	ns
DQS write postamble hold time	tWPSTH	15	-	15	-	ns
Data hold time	tDH	-	-	-	-	ns
Data hold time tight timing	tDH_tight	0.24	-	0.2	-	ns
Data hold time relaxed timing	tDH_relaxed	0.31	-	0.26	-	ns
Data setup time	tDS	-	-	-	-	ns
Data DQ setup time tight timing	tDS_tight	0.24	-	0.2	-	ns
Data DQ setup time relaxed timing	tDS_relaxed	0.31	-	0.26	-	ns
Data Output						
Access window of DQ[7:0] from RE_n (RE_t/RE_c cross-point)	tAC	3	25	3	25	ns
(RE_n low or RE_t/RE_c crosspoint) to DQS/DQ driven by device	tDQSD	5	18	5	18	ns
DQS-DQ skew (DQS to last DQ valid, per access)	tDQSQ	-	0.3	-	0.25	ns
Access window of DQS from RE_n (RE_t/RE_c)	tDQSRE	3	25	3	25	ns
DQS hold time after (RE_n low or RE_t/RE_c crosspoint)	tDQSRH	5	-	5	-	ns

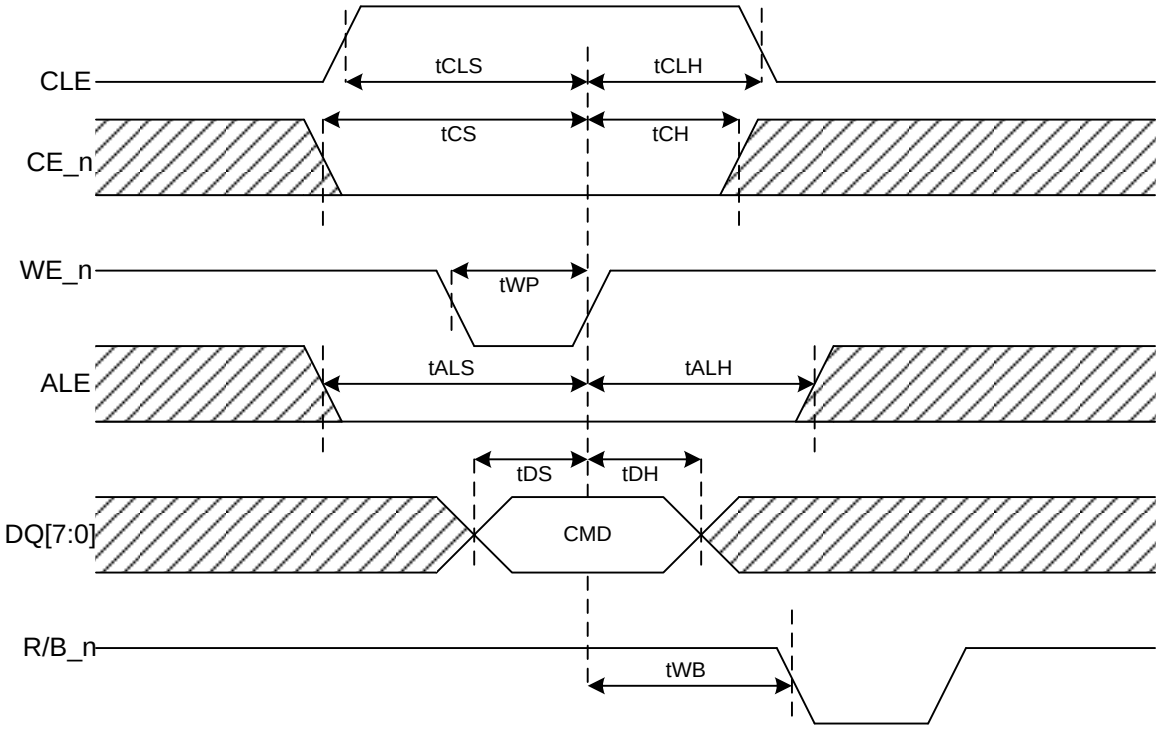
Output data valid window	tDVW	Min: tQH - tDQSQ Max: tQH - tDQSQ				ns
DQ-DQS hold (DQS to first DQ to go invalid, per access)	tQH	0.37	-	0.37	-	tRC(avg)
DQS output HIGH time (if differential, DQS_t is high)	tQSH	0.37	-	0.37	-	tRC(avg)
DQS output LOW time (if differential, DQS_t is low)	tQSL	0.37	-	0.37	-	tRC(avg)
Average read cycle time	tRC(avg)	3	-	2.5	-	ns
Absolute read cycle period	tRC(abs)	Min: tRC(AVG) + tJITper(RE_n) (min) Max: tRC(AVG) + tJITper(RE_n) (max)				ns
Average RE_n (RE_t) HIGH width	tREH(avg)	0.45	0.55	0.45	0.55	tRC(avg)
Absolute RE_n (RE_t) HIGH width	tREH(abs)	0.43	-	0.43	-	tRC(avg)
Average RE_n (RE_t) LOW width	tRP(avg)	0.45	0.55	0.45	0.55	tRC(avg)
Absolute RE_n (RE_t) LOW width	tRP(abs)	0.43	-	0.43	-	tRC(avg)
Read preamble	tRPRE	15	-	15	-	ns
Read preamble with ODT enabled	tRPRE2	25	-	25	-	ns
Read postamble	tRPST	Min: tDQSRE + 0.5*tRC		Max: -		ns
Read postamble hold time	tRPSTH	15	-	15	-	ns
Jitter						
The deviation of a given tDQS(abs)/tDSC(abs) from a tDQS(avg)/tDSC(avg)	tJITper(DQS)	-0.24	0.24	-0.2	0.2	ns
The deviation of a given tRC(abs)/tDSC(abs) from a tRC(avg)/tDSC(avg)	tJITper(RE_n)	-0.18	0.18	-0.15	0.15	ns
Cycle to cycle jitter for DQS	tJITcc(DQS)	0.48	-	0.4	-	ns
Cycle to cycle jitter for RE_n	tJITcc(RE_n)	0.36	-	0.3	-	ns
Volume Addressing						
Delay prior to bringing CE_n high after a new Volume is selected using the Volume Select command	tCEVDLY	50	-	50	-	ns
Delay prior to issuing the next command after a new Volume	tVDLY	50	-	50	-	ns

is selected using the Volume Select command						

5.12. Timing Diagrams

5.12.1. Timing Diagrams in SDR

Figure 29. Command Latch Timings in SDR



Notes:

The requirement for the R/B_n signal only apply to commands where R/B_n is cleared to zero after the command is issued, as specified in the command definitions.

Figure 30. Address Latch Timings in SDR

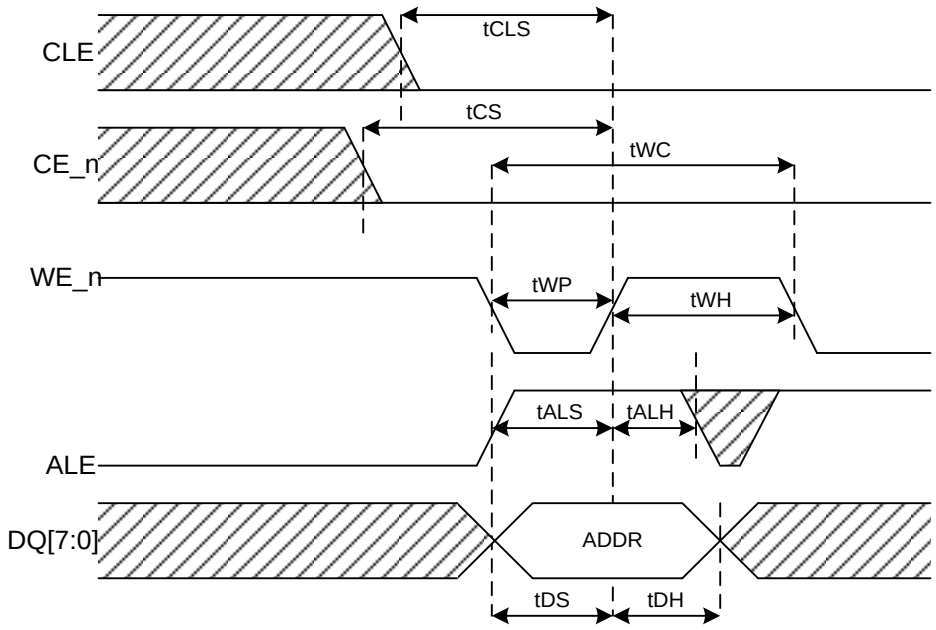
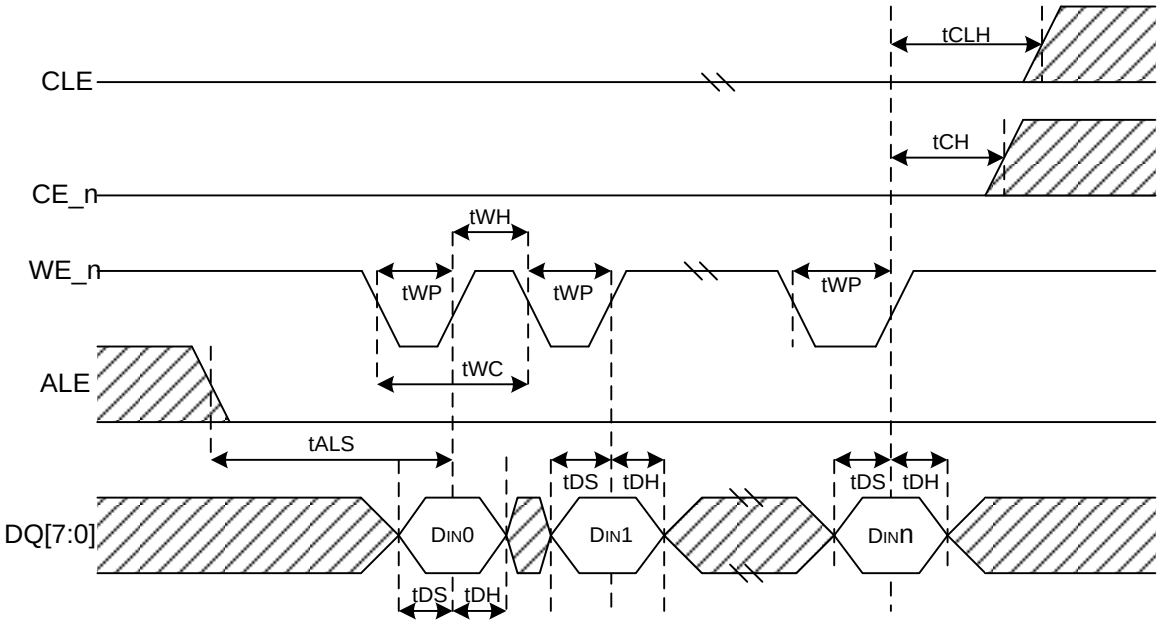


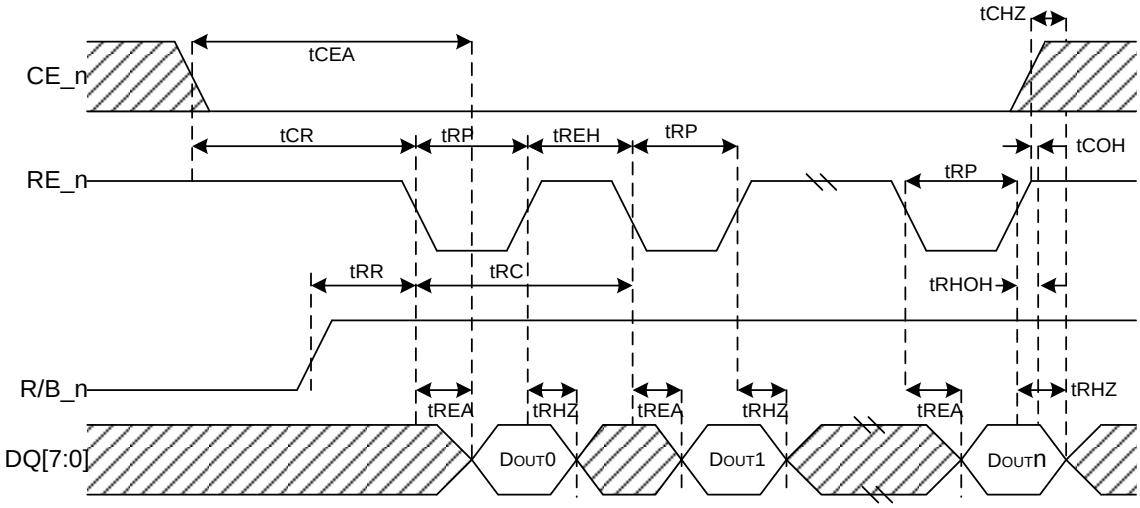
Figure 31. Data Input Cycle Timings in SDR



Notes:

Data input may be accompanied with CE_n Don't Care. However, if CE_n Don't Care is performed, tCS and tCH requirements shall be met by the host, and the WE_n falling edge shall always occur after the CE_n falling edge (i.e. tCS>tWP).

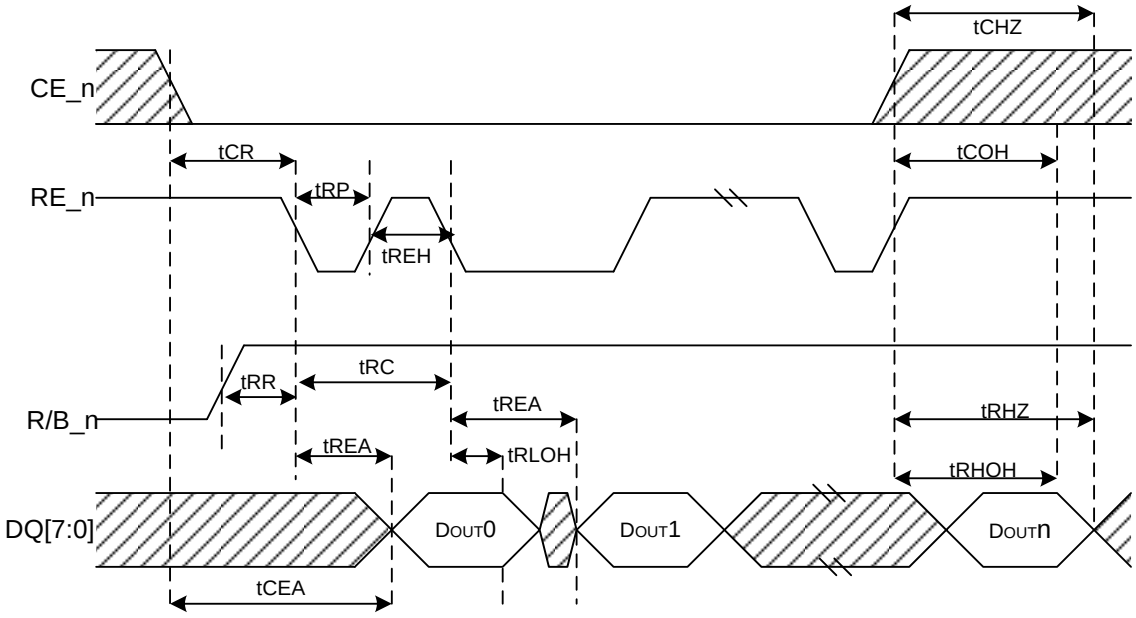
Figure 32. Data Output Cycle Timings in SDR



Notes:

Data output may be accompanied with CE_n Don't Care. However, if CE_n don't care is performed, tCEA and tCOH requirements shall be met by the host, and either RE_n shall remain low or the RE_n falling edge shall occur after the CE_n falling edge.

Figure 33. Data Output Cycle Timings (EDO) in SDR



Notes:

EDO data output cycle timings shall be used if the host drives tRC less than 30 ns. Data output may be accompanied with CE_n Don't Care. However, if CE_n Don't Care is performed, tCEA and tCOH requirements shall be met by the host.

Figure 34. Read Status Timings in SDR

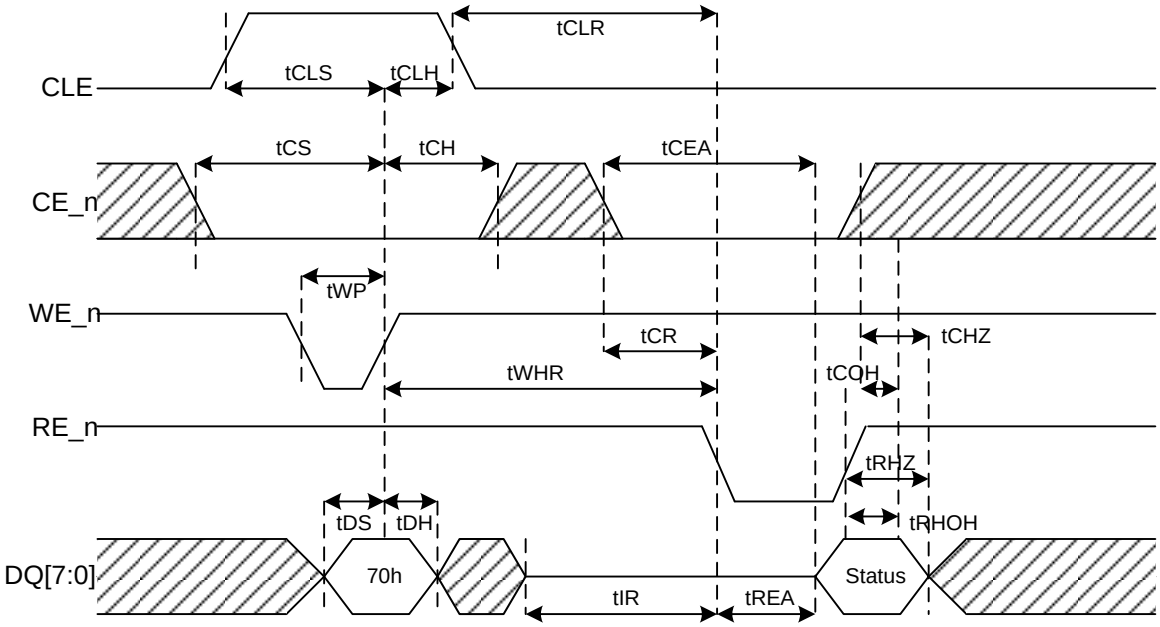
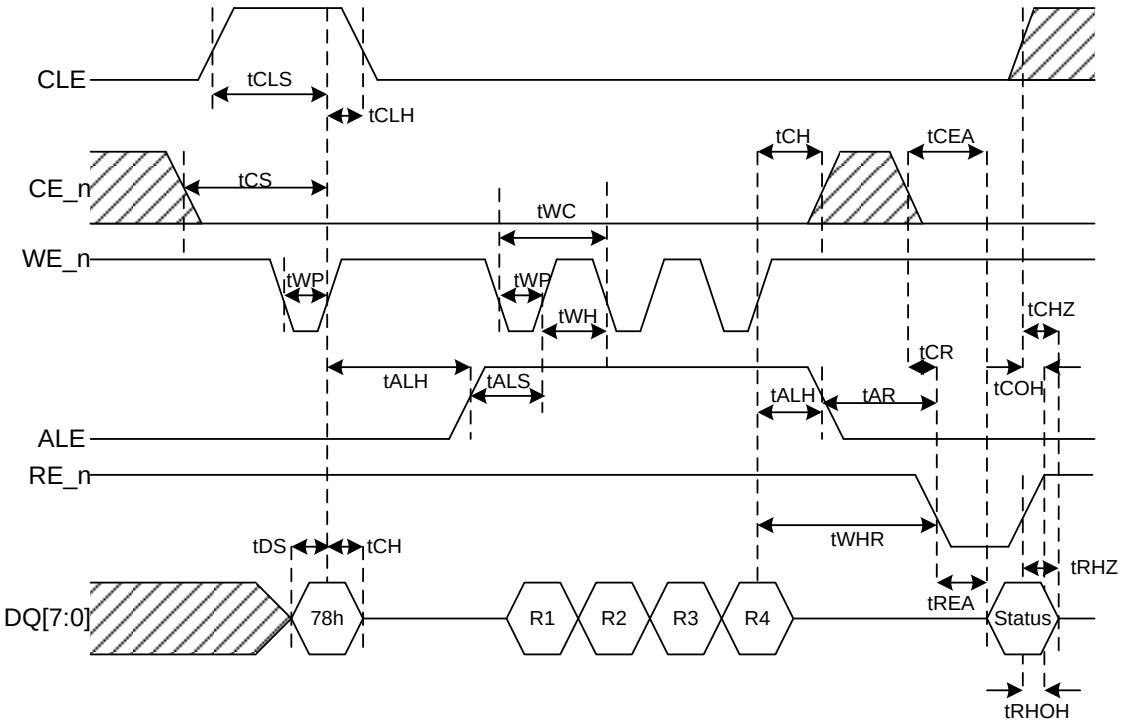
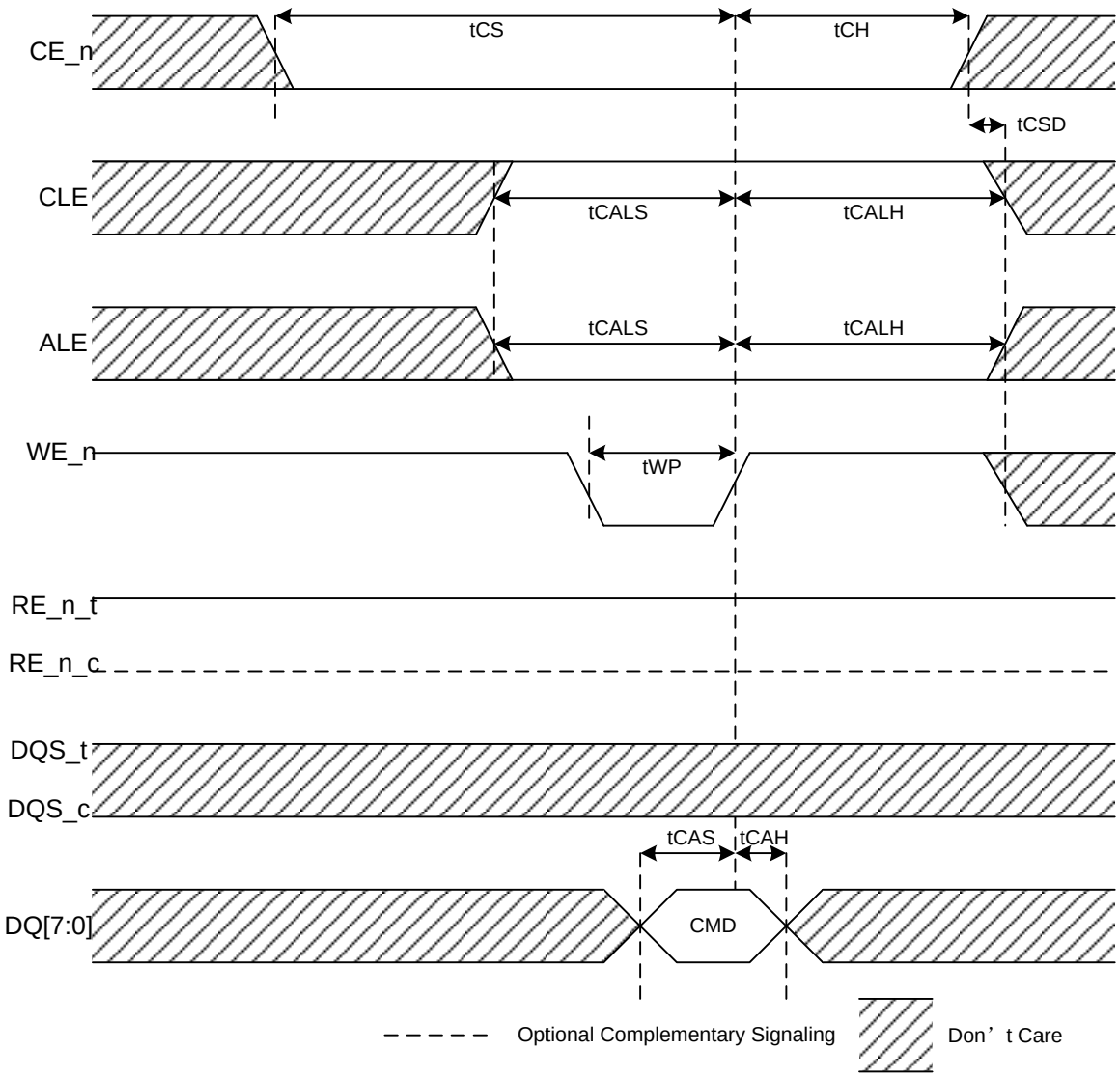


Figure 35. Read Status Enhanced Timings in SDR



5.12.2. Timing Diagrams in NV-DDR2/NV-DDR3

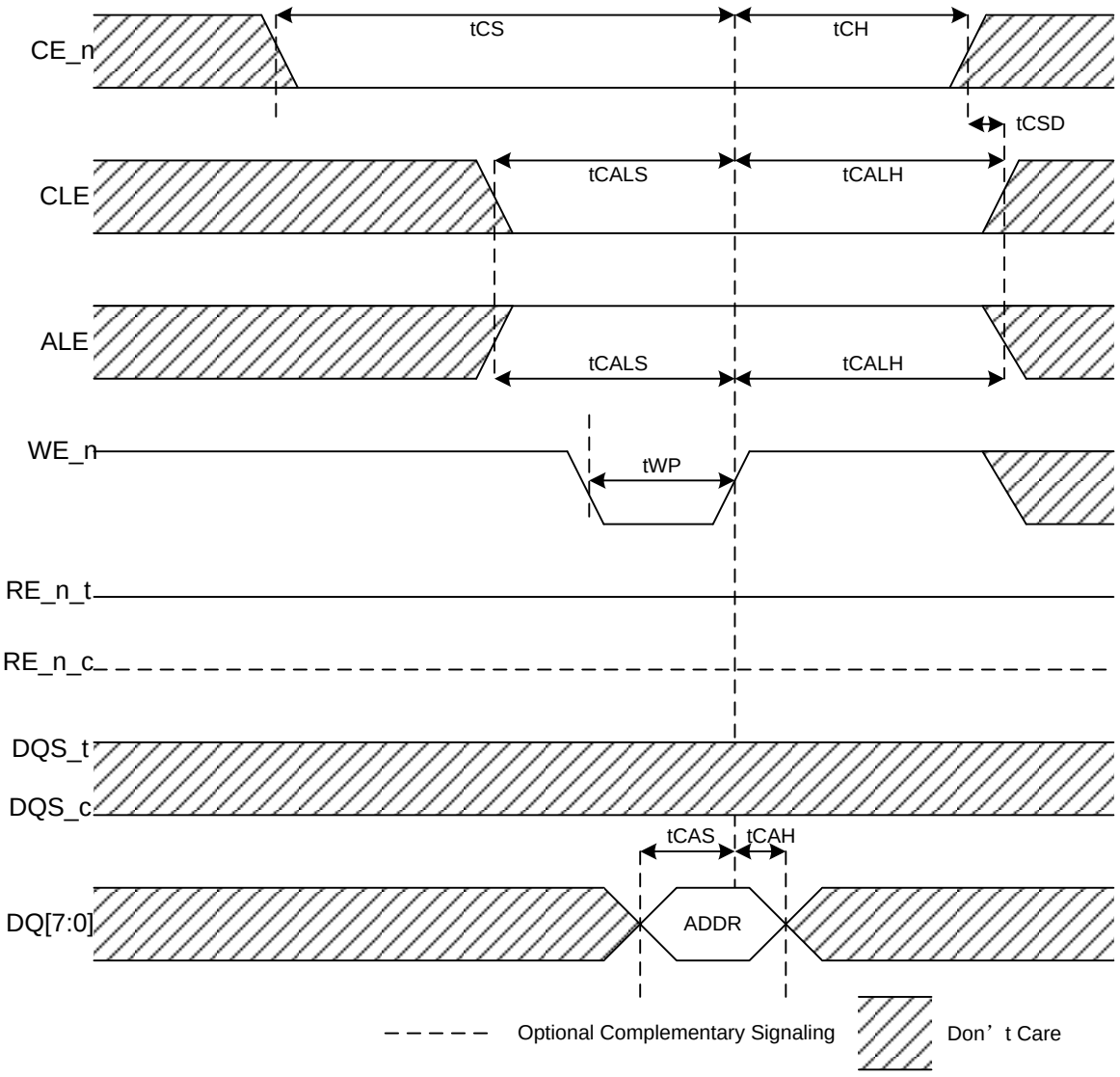
Figure 36. Command Cycle Timings in NV-DDR2/NV-DDR3



Notes:

When the bus state is not a data input or data output cycle and the ALE, CLE and CE_n signals are all low (i.e. idle state), DQS (DQS_t) shall be held high by the host to prevent the device from enabling ODT. If ODT is disabled, DQS is a Don’t Care during idle states.

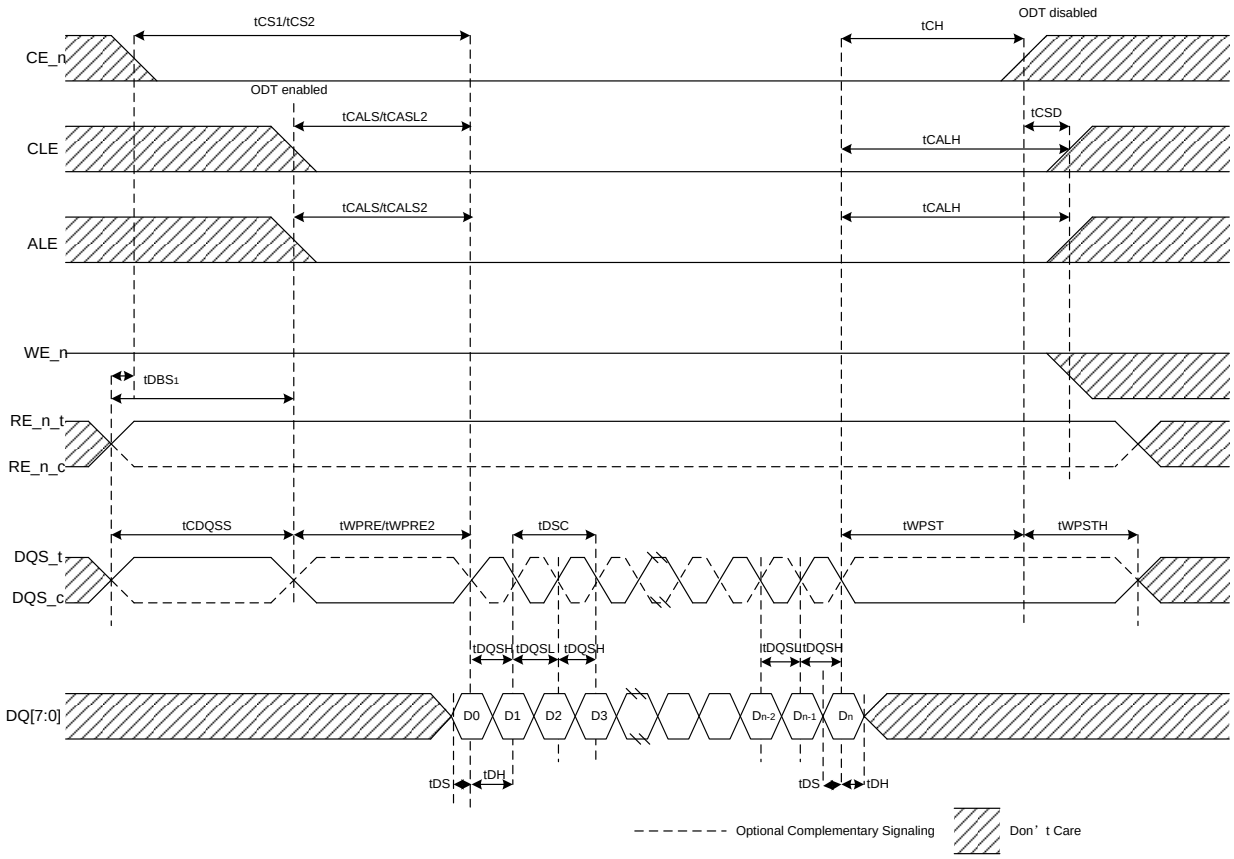
Figure 37. Address Cycle Timings in NV-DDR2/NV-DDR3



Notes:

When the bus state is not a data input or data output cycle, and the ALE, CLE and CE_n signals are all low (i.e. idle state), DQS (DQS_t) shall be held high by the host to prevent the device from enabling ODT. If ODT is disabled, DQS is a Don't Care during idle states.

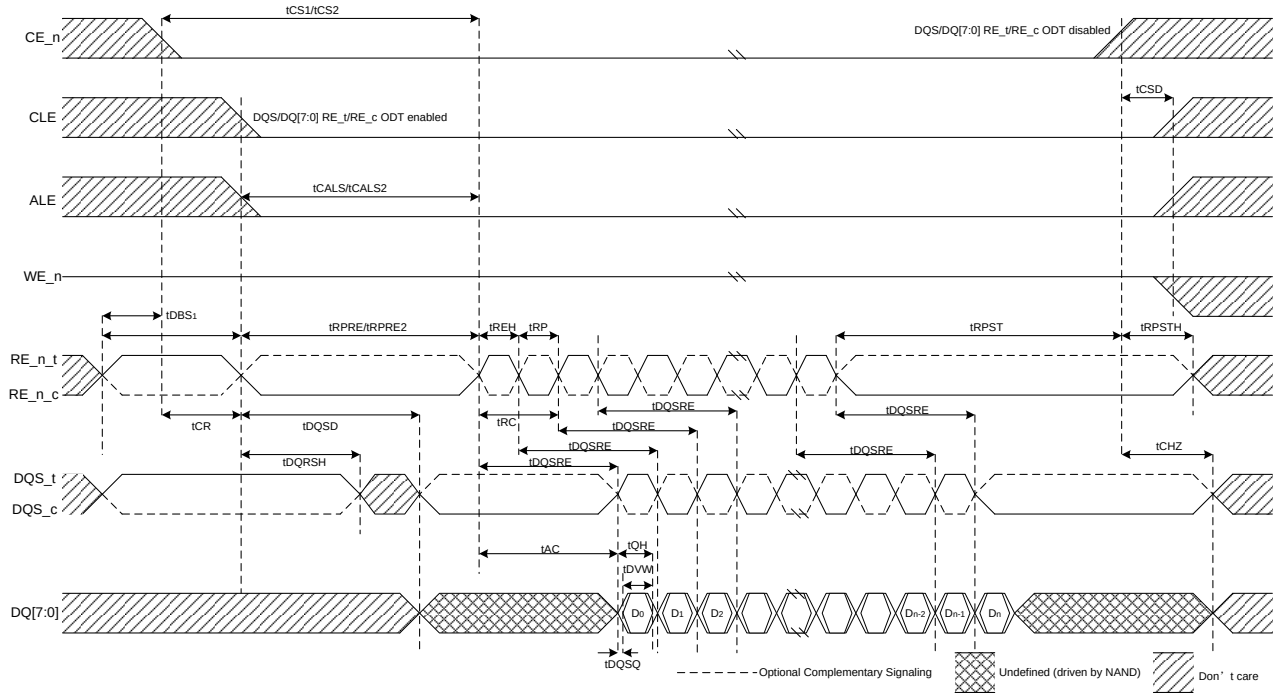
Figure 38. Data Input Cycle Timings in NV-DDR2/NV-DDR3



Notes:

1. Data input may pause by stopping the transitioning of DQS (DQS_t/DQS_c).
2. For the Set Features and ODT Configure commands, the same data byte is repeated twice. The data pattern in this case is [D0 D0 D1 D1 D2 D2 …]. The device shall only latch one copy of each data byte.
3. ODT may not be used for data input. If ODT is selected for use with Set Features, ODT is enabled and disabled during the points indicated in this figure.
4. tDBS refers to the last falling edge of either CLE, ALE or CE_n.
5. To exit the data burst, CE_n, ALE or CLE is set to one by the host.

Figure 39. Data Output Cycle Timings in NV-DDR2/NV-DDR3



Notes:

1. Data output may pause by stopping the transitioning of RE_n (RE_t/RE_c).
2. For the Read ID, Get Features, Read Status and Read Status Enhanced commands, the same data byte is repeated twice. The data pattern in this case is [D0 D0 D1 D1 D2 D2 …]. The host shall only latch one copy of each data byte.
3. ODT may not be used for data output. If ODT is selected for use with Set Features, ODT is enabled and disabled during the points indicated in this figure.
4. tDBS refers to the last falling edge of either CLE, ALE or CE_n.
5. To exit the data burst, CE_n, ALE or CLE is set to one by the host. tCHZ only applies when CE_n is used to end the data burst.

6. Command and Feature Description

6.1. Command Sets

6.1.1. Command Format

Figure 40. Agnostic Command Description

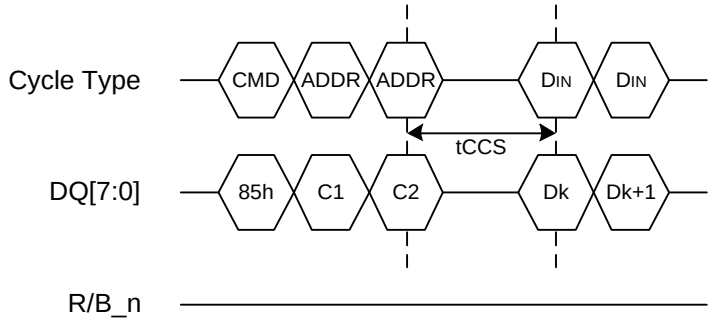


Figure 41. SDR Data Interface Command Description

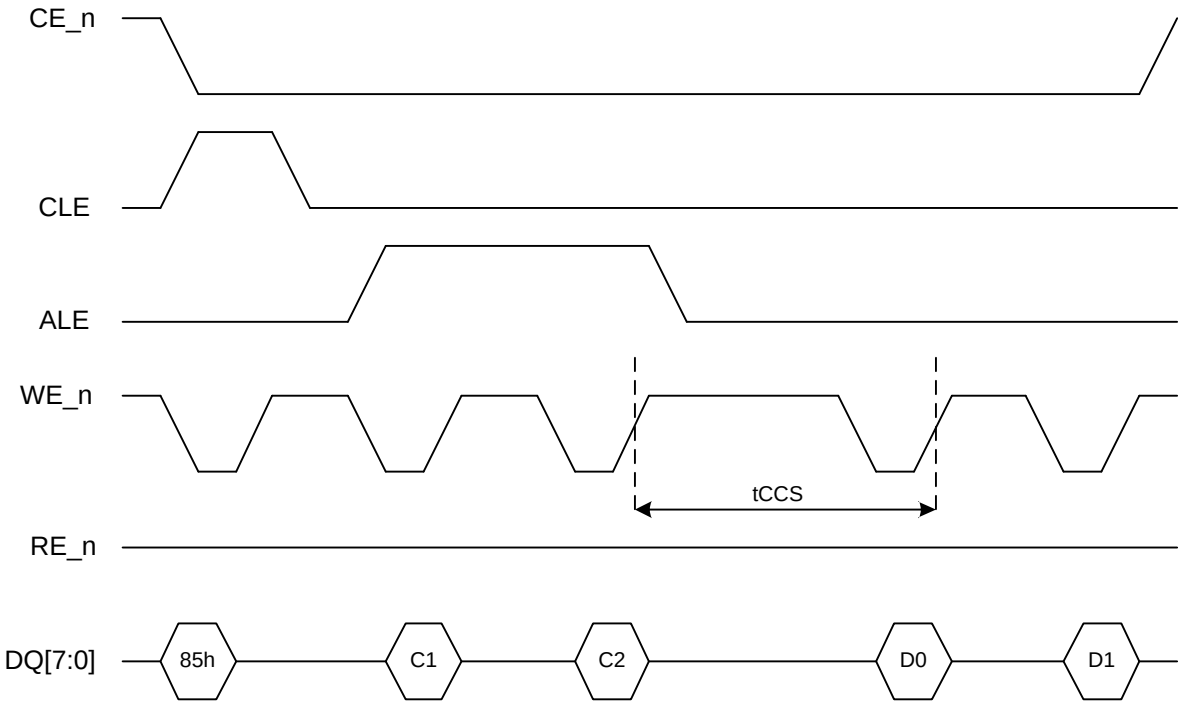
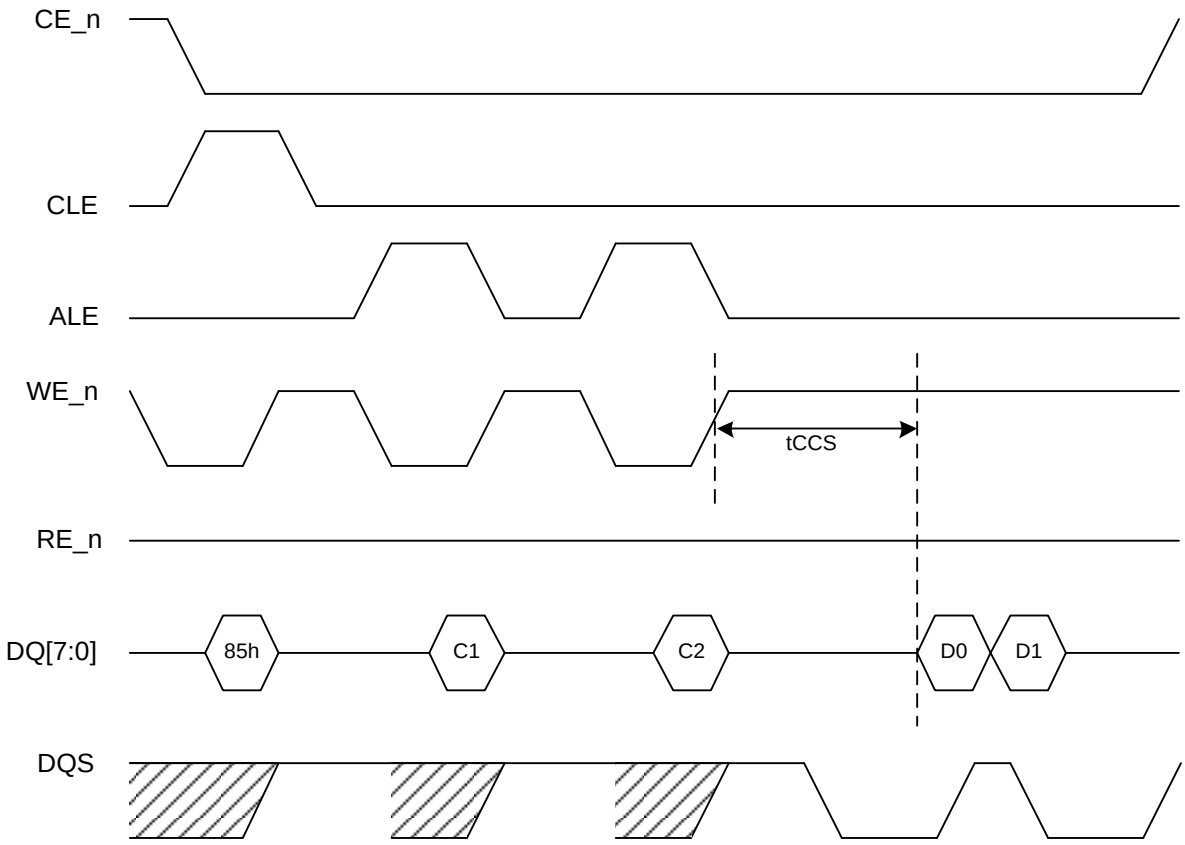


Figure 42. NV-DDR2/NV-DDR3 Data Interface Command Description



Notes:

When the bus state is not a data input or data output cycle, if ALE, CLE and CE_n are all low (i.e. Idle state) then DQS (DQS_t) shall be held high by the host to prevent the device from enabling ODT. If ODT is disabled, then DQS is a don't care during Idle states.

6.1.2. Command Definition

Table 70. Command Sets

Command	1st Sequence Cycle			2nd Sequence Cycle			Acceptable While			Target Level CMDs
	1st Set	Address Cycles	2nd Set	1st Set	Address Cycles	2nd Set	Cache Busy	Array Busy	Other LUN Busy	
Reset	FFh						Y	Y	Y	Y
Synchronous Reset	FCh						Y	Y	Y	Y
Reset LUN	FAh	4					Y	Y	Y	
Hard Reset	FDh								Y	
Read ID	90h	1								
Read Unique ID	EDh	1								
Read Status	70h						Y	Y	Y	
Read Status Enhanced	78h	4					Y	Y	Y	
Read Status Enahnced II	73h	4					Y	Y	Y	
Read Parameter Page	ECh	1								
Page Read	00h	6	30h						Y	
Multi-Plane Page Read	00h	6	32h	00h	6	30h			Y	
Sequential Cache Read	31h							Y	Y	
Multi-Plane Sequential Cache Read	31h							Y	Y	
Random Cache Read	00h	6	31h					Y	Y	
Multi-Plane Random Cache Read	00h	6	32h	00h	6	31h		Y	Y	
Read Cache End								Y	Y	
Page Program	80h	6	10h						Y	
Multi-Plane Page Program	80h	6	11h	80h	6	1Ah/ 10h			Y	
Multi-Plane Page Program (JEDEC)	80h	6	11h	81h	6	1Ah/ 10h			Y	
Cache Program	80h	6	15h					Y	Y	
Multi-Plane Cache Program	80h	6	11h	80h	6	1Ah/ 15h		Y	Y	

Command	1st Sequence Cycle			2nd Sequence Cycle			Acceptable While			Target Level CMDs
	1st Set	Address Cycles	2nd Set	1st Set	Address Cycles	2nd Set	Cache Busy	Array Busy	Other LUN Busy	
One-Pass Page Program	80h		1Ah	80h	6	10h			Y	
Multi-Plane One-Pass Page Program	80h	6	11h	80h	6	1Ah/ 10h			Y	
One-Pass Cache Program	80h	6	1Ah	80h	6	15h/ 10h		Y	Y	
Multi-Plane One-Pass Cache Program	80h	6	11h	80h	6	1Ah/ 15h/ 10h		Y	Y	
Change Write Column	85h	2						Y	Y	
Change Row Address	85h	6						Y	Y	
Change Read Column	05h	2	E0h					Y	Y	
Change Read Column Enhanced	06h	6	E0h					Y	Y	
Change Read Column Enhanced (JEDEC)	00h	6	-	05h	2	E0h		Y	Y	
Block Erase	60h	4	D0h						Y	
Multi-Plane Block Erase	60h	4	D1h	60h	4	D0h			Y	
Multi-Plane Block Erase (JEDEC)	60h	4	-	60h	4	D0h			Y	
Copyback Read	00h	6	35h						Y	
Multi-Plane Copyback Read	00h	6	32h	00h	6	35h			Y	
Copyback Program	85h	6	10h						Y	
Multi-Plane Copyback Program	85h	6	11h	85h	6	10h			Y	
Multi-Plane Copyback Program (JEDEC)	85h	6	11h	81h	6	10h			Y	
Program Suspend	87h	6						Y	Y	
Program Resume	17h	6						Y	Y	
Erase Suspend	67h	4						Y	Y	
Erase Resume	D7h							Y	Y	
Volume Select	E1h	1					Y	Y	Y	Y

Command	1st Sequence Cycle			2nd Sequence Cycle			Acceptable While			Target Level CMDs
	1st Set	Address Cycles	2nd Set	1st Set	Address Cycles	2nd Set	Cache Busy	Array Busy	Other LUN Busy	
ODT Configure	E2h	1								Y
ZQ Calibration Short	D9h	1							Y	
ZQ Calibration Long	F9h	1							Y	
Set Features	EFh	1								Y
Get Features	EEh	1								Y
LUN Set Features	D5h	2							Y	
LUN Get Features	D4h	2							Y	
Fast Partial Page Read	00h	6	20h						Y	
Erased Page Check	00h	6	33h						Y	
SLC Mode Access	DAh								Y	
SLC Mode Abort	DFh								Y	

6.2. Reset Operations

6.2.1. Reset (FFh)

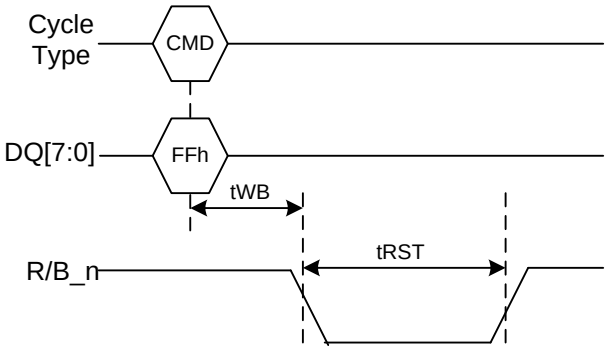
The Reset command puts the target in its default power-up state and no address cycle is needed. If this command is issued in the NV-DDR2 interface, the target will be switched into the SDR data interface. If this command is issued in the NV-DDR3 data interface, the target shall remain in the NV-DDR3 data interface following this command.

The Reset command is required as the first command after power-up. It can do power-on reset to put a target into an initialized state only once during each power cycle. Power-on reset does register reloading. Once the LUN goes through the power-on reset sequence, the Reset command would serve as operation interruption purpose before next power down.

The R/B_n value is unknown when Reset is issued; R/B_n transitions to low tWB after the Reset command is issued, and keeps low for tRST.

The Reset command can abort any operation with which the device is in busy state. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Pass/Fail status bits value in Status Register are cleared to "0". For device status after reset operation, refer to **Table 76 "Status Register Definitionstatus register information"**. If the device is in reset process (R/B_n is low) and the host issues another reset command within tRST, the second reset command will be ignored and NAND will continue to finish the first reset process. If the NAND is already in ready state after the reset process, a new reset command can be accepted by the command register and a new reset operation will be retriggered.

Figure 43. Reset Sequence

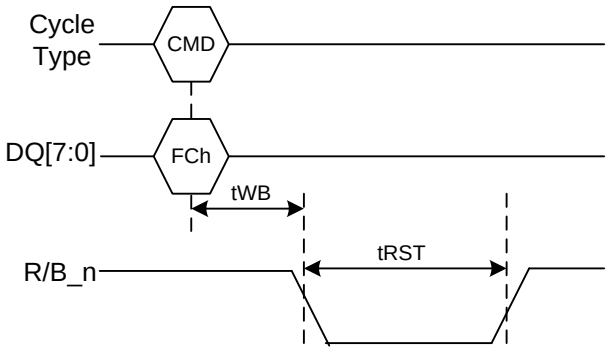


6.2.2. Synchronous Reset (FCh)

The Synchronous Reset command resets the target and all LUNs and no address cycle is needed. The command may be executed with the target in any state. The R/B_n value is unknown when Synchronous Reset is issued; R/B_n is guaranteed to be low tWB after the Synchronous Reset command is issued.

This command shall be supported by devices that support NV-DDR2 or NV-DDR3 data interfaces. This command is only accepted when the NV-DDR2 or NV-DDR3 data interface is used. The host should not issue this command when the device is configured to the SDR data interface. The target shall remain in NV-DDR2 or NV-DDR3 data interface following this command.

Figure 44. Synchronous Reset Sequence

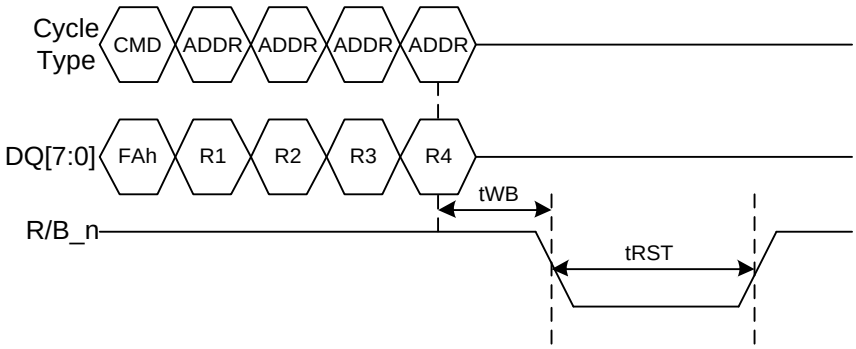


6.2.3. Reset LUN (FAh)

The Reset LUN command is used to reset a particular LUN. This command is accepted by only the LUN addressed as part of the command. The command may be executed with the LUN in any state. The SR[6] value is unknown when Reset LUN is issued; SR[6] is guaranteed to be low tWB after the Reset LUN command is issued. This command does not affect the data interface configuration of the target.

Reset LUN should be used to cancel ongoing command operations. Any program, erase or read operations would be interrupted by the Reset LUN command. If the Reset LUN (FAh) command is issued during program and erase operations, the data integrity in the array is not guaranteed. If the Reset LUN (FAh) command is issued during the read operation, the output data will be invalid.

Figure 45. Reset LUN sequence



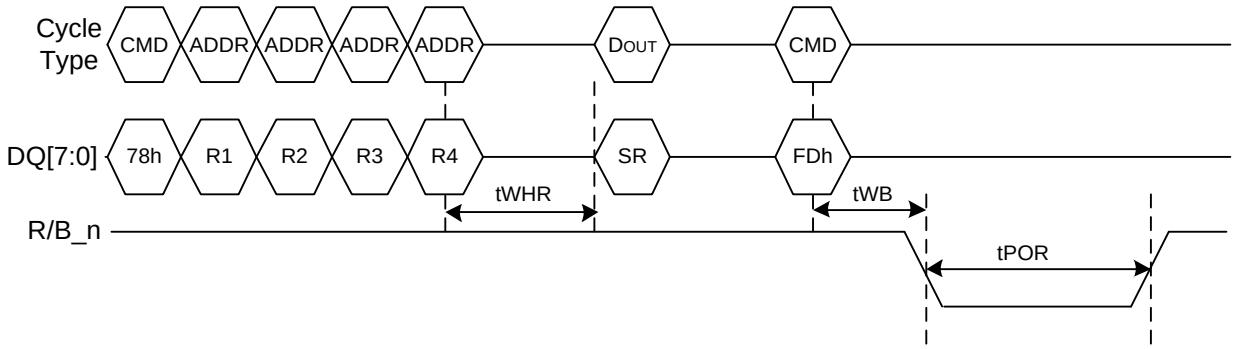
6.2.4. Hard Reset (FDh)

The Hard Reset command performs an initialization to the selected LUN similar to the initialization performed by the first Reset (FFh) command after device power-on. After tPOR, all parameters and configurations shall be initialized to default values with the exception of previously assigned Volume configuration and Electronic Mirroring configuration. If in NV-DDR2 data interface, issuing Hard Reset command places the target in the SDR data interface. If the Hard Reset command is issued in SDR data interface, the target's data interface remains in SDR; if the command is issued when the target is configured in the NV-DDR3 data interface, the target shall remain in the NV-DDR3 data interface following this command.

Before issuing the Hard Reset command, the host is required to issue a Read Status Enhanced (78h) command to select a LUN. Hard Reset supports multiple LUN operations.

The Hard Reset command can be accepted only when the selected LUN is not in busy state.

Figure 46. Hard Reset Sequence



6.3. Read Operations

6.3.1. Read ID (90h)

The Read ID command can identify the target device. By issuing the Read ID command on address 20h, if the target supports the ONFI specification, then the ONFI signature shall be returned at the first four bytes. The ONFI signature is the ASCII encoding of "ONFI" where "O"=4Fh, "N"=4Eh, "F"=46h and "I"=49h. Definition for 5th and 6th byte of Read ID was added for ONFI 4.0. The Power on Interface ID is set only once per power cycle and does not change. If the device exits power-on reset with the SDR or NV-DDR3 power on interface active, issuing the Set Features (EFh) command or LUN Set Features (D5h) command to change the interface will not change the IID value. Read beyond six bytes yields indeterminate output values.

By issuing the Read ID command on address 00h, device returns JEDEC manufacture code and device ID. This NAND Flash device has 5 bytes for device ID, as shown in the table below. When the host issues the Read ID command in the NV-DDR2 or NV-DDR3 data interface, each data byte is received twice. The host shall only latch one copy of each data byte.

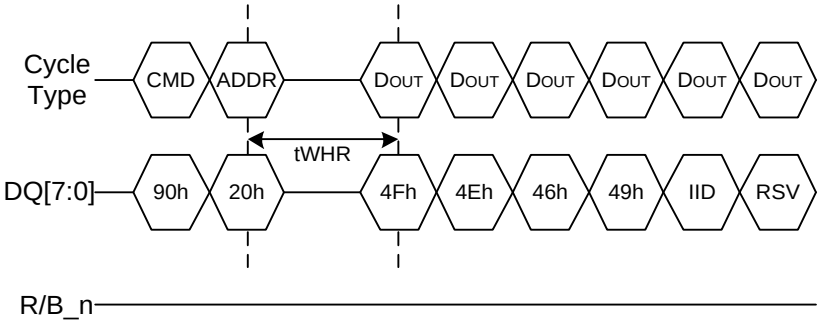
Notes:

1. Read ID is a LUN-level command. After power-up or hard reset, if the host doesn't issue Read Status Enhanced command to do LUN selection, LUN0's ID will be read by default.
2. All LUNs have the same ID for multi-LUN configuration.

Table 71. Read ID Table

Device Identifier Byte	Description
1st	Manufacture code
2nd	Device identifier
3rd	Internal chip number, cell type, voltage
4th	Page size, block size, plane number
5th	Technology (design rule)
6th	Reserved

Figure 47. ID Read sequence for ONFI Signature



Notes:

1. IID: power on interface ID. 00h for SDR; 01h for NV-DDR3
2. RSV: reserved for future use.

Figure 48. ID Read sequence for Manufacturer ID

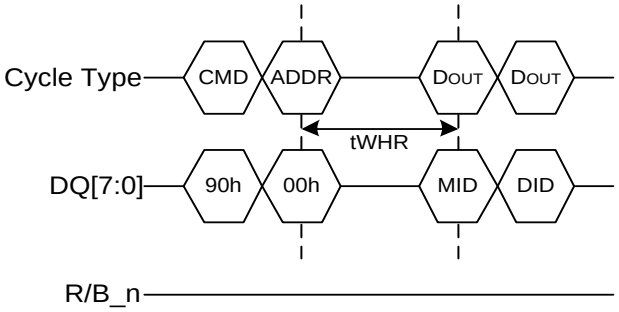


Table 72. DID Details

Byte	Description		DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value
0	Manufacturer ID	YMTC	1	0	0	1	1	0	1	1	9Bh
1	Device ID	256Gb/CE	1	1	0	0	0	0	1	1	C3h
		512Gb/CE	1	1	0	0	0	1	0	0	
		1024Gb/CE	1	1	0	0	0	1	0	1	
		2048Gb/CE	1	1	0	0	0	1	1	0	
2	Number of LUN per CE	1 LUN							0	0	00b
		2 LUNs							0	1	
		4 LUNs							1	0	
		8 LUNs							1	1	
	Cell Type	SLC					0	0			10b
		MLC					0	1			

Byte	Description		DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value
		TLC					1	0			
		QLC					1	1			
	Voltage	3.3V V_{CC}, 3.3V V_{CCQ}		0	0	0					100b
		3.3V V_{CC}, 1.8V V_{CCQ}		0	0	1					
		3.3V V_{CC}, 1.2V V_{CCQ}		0	1	0					
		3.3V V_{CC}, 3.3V/1.8V V_{CCQ}		0	1	1					
		3.3V V_{CC}, 1.8V/1.2V V_{CCQ}		1	0	0					
		Reserved		1	0	1					
		Reserved		1	1	0					
		Reserved		1	1	1					
	Reserved		0								0b
3	Page Size(w/o spare area)	8KB							0	0	01b
		16KB							0	1	
		Reserved							1	0	
		Reserved							1	1	
	Block Size(w/o spare area)	6MB				0	0	0			001b
		18MB				0	0	1			
		Reserved				0	1	0			
		Reserved				0	1	1			
		Reserved				1	0	0			
		Reserved				1	0	1			
		Reserved				1	1	0			
		Reserved				1	1	1			
	Plane Number per LUN	1		0	0						01b
		2		0	1						
		4		1	0						
		8		1	1						
	Reserved		0								0b
4	N/A						N/A	N/A	N/A	N/A	N/A
	Technology	Gen1		0	0	0					001b
		Gen2		0	0	1					
		Gen3		0	1	0					
		Gen4		0	1	1					
		Gen5		1	0	0					
		Reserved		1	0	1					
		Reserved		1	1	0					

Byte	Description		DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value
		Reserved		1	1	1					
	Reserved		0								0b
5	Reserved		0	0	0	0	0	0	0	0	00h

Figure 49. Read ID Timing (SDR)

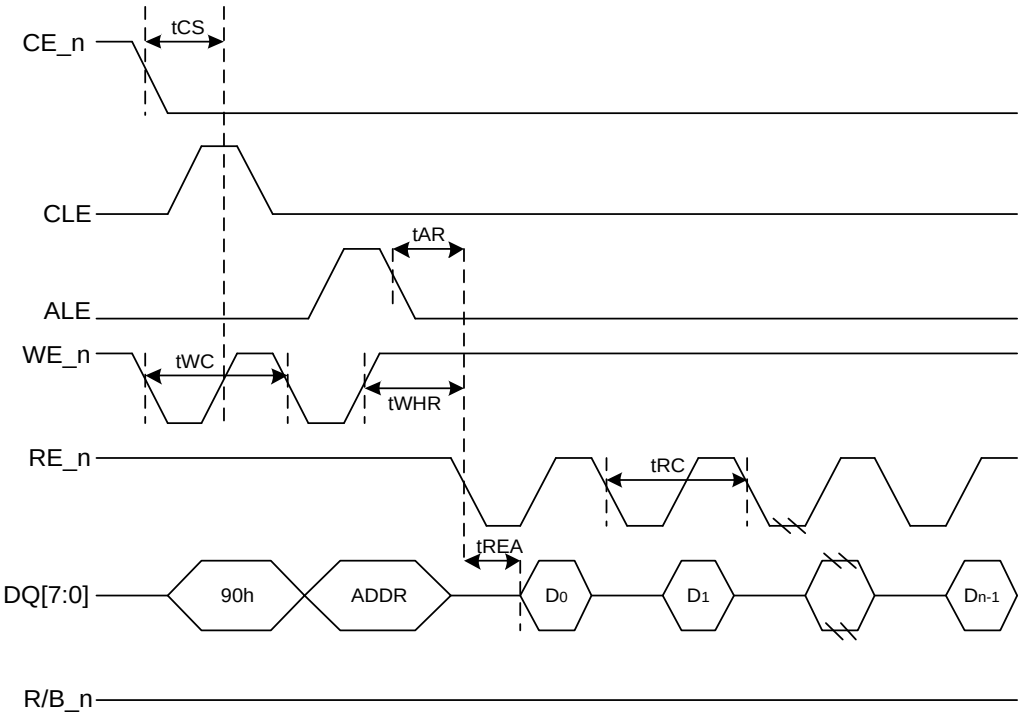
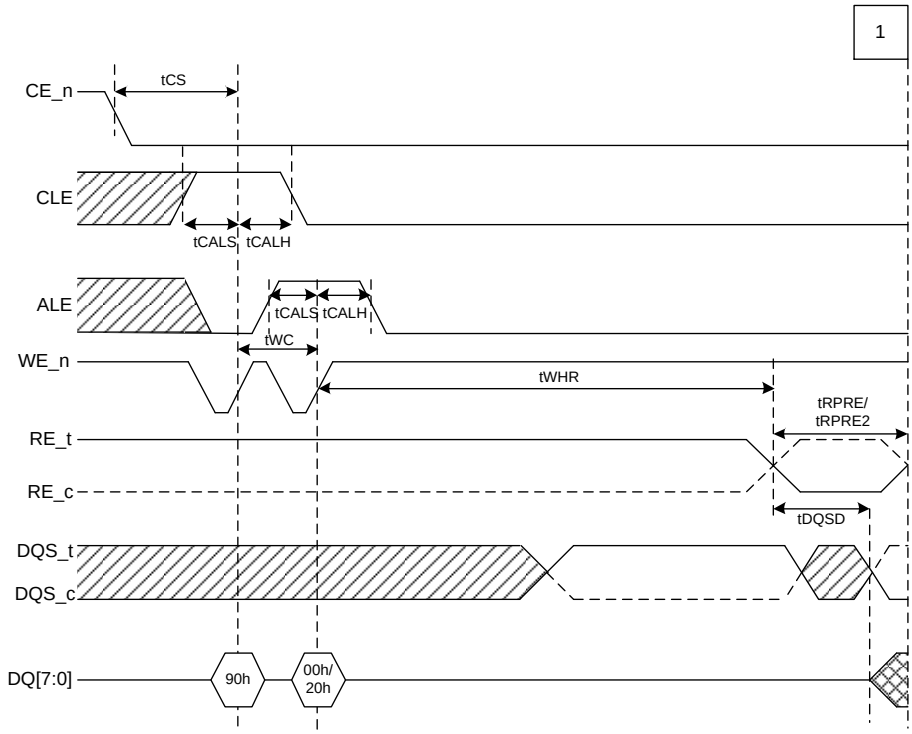
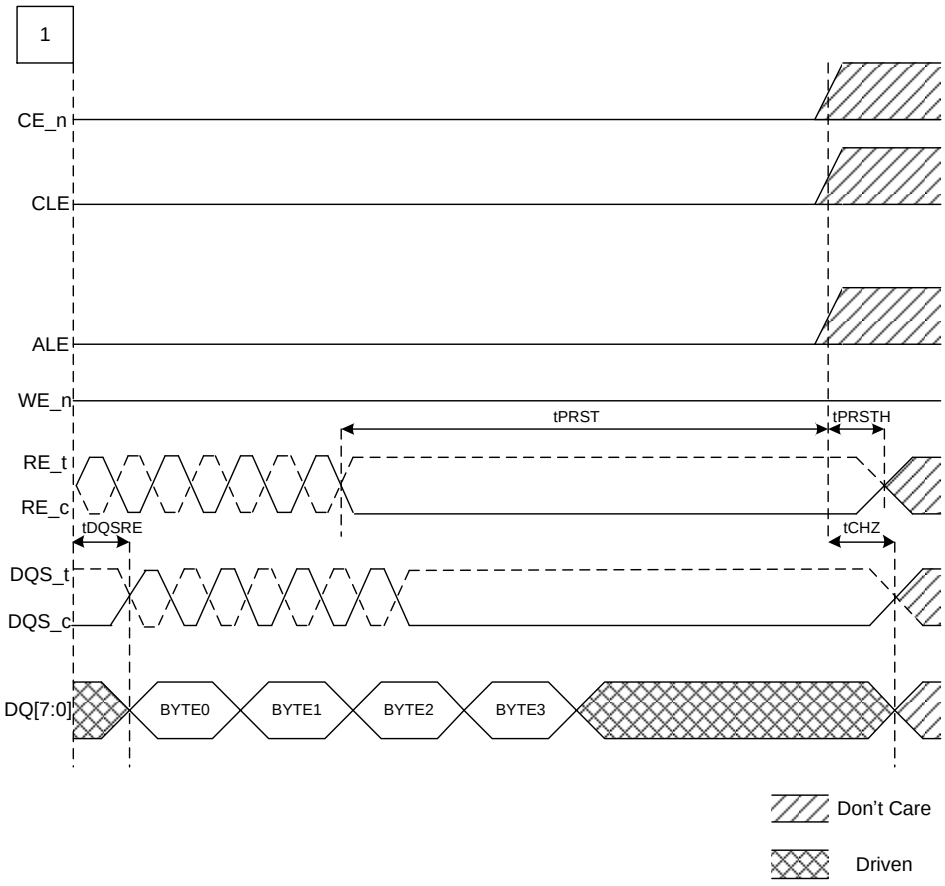


Figure 50. Read ID Timing (NV-DDR2/NV-DDR3)





6.3.2. Read Unique ID (EDh)

The Read Unique ID command on address 00h is used to retrieve the 16 bytes unique ID (UID) for the device. The unique ID when combined with the device manufacturer shall be unique.

The UID data may be stored within the flash array. To allow the host to determine if the UID is without bit errors, the UID is returned with its complement, as shown in the table below. If the XOR of the UID and its bit-wise complement is all ones, then the UID is valid.

Notes:

1. Read Unique ID is a LUN-level command. After power-up or hard reset, if the host doesn't issue Read Status Enhanced command to do LUN selection, LUN0's UID will be read out by default.
2. Each LUN has different UIDs for multi-LUN configuration.

Table 73. UID and Complement

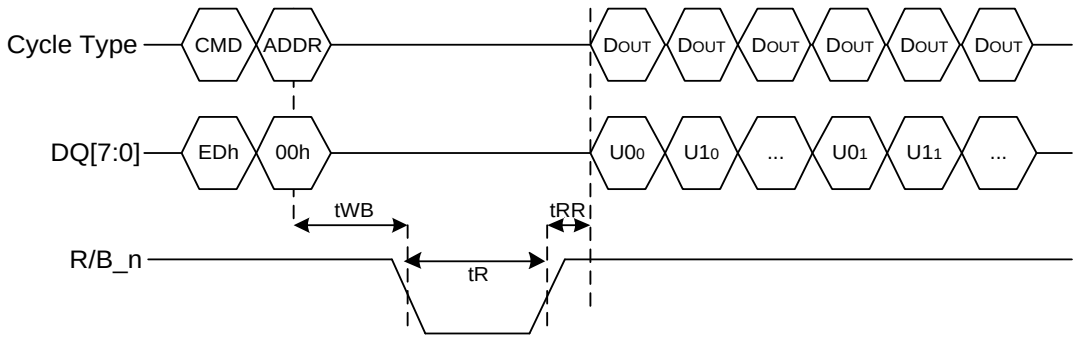
Bytes	Value
0-15	UID
16-31	UID complement (bit-wise)

To accommodate robust retrieval of the UID in case of bit errors, 16 copies of the UID and the corresponding complement shall be stored by the target. For example, reading bytes 32-63 return to the host another copy of the UID and its complement.

The Read Status Enhanced (78h) command shall not be used during execution of the Read Unique ID command.

The host may use any timing mode supported by the target in order to retrieve the UID data.

Figure 51. Read Unique ID sequence



Notes:

U0k-Unk: The kth copy of the UID and its complement. Sixteen copies are stored. Reading beyond 512 bytes returns indeterminate values.

6.3.3. Read Parameter Page (ECh)

The Read Parameter Page command on address 00h retrieves the data structure that describes organization, features, timings and other behavioral parameters of the target.

Values in the parameter page are static and shall not change. The host is not required to read the parameter page after power management events.

The Change Read Column (05h-E0h) command can be issued after tR of the Read Parameter Page command sequence to read specific portions of the parameter page.

At the first time the host executes the Read Parameter Page command after power-on, timing mode 0 shall be used. If the host determines that the target supports more advanced timing modes, those supported timing modes may be used for subsequent execution of the Read Parameter Page command.

The Read Status (70h) command may be used to check the status of Read Parameter Page during execution. After completion of the Read Status command, 00h shall be issued by the host on the command line to continue with the data output flow for the Read Parameter Page command.

The Read Status Enhanced (78h) command and the Change Read Column Enhanced (06h-E0h) command shall not be used during execution of the Read Parameter Page command.

The following table defines the parameter page data structure. For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte. Reading bytes beyond the end of the final parameter page copy returns indeterminate values.

Values are reported in the parameter page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the chip will return how many data bytes are in a page.

Notes:

1. Read Parameter Page is a LUN-level command. After power-up or hard reset, if the host doesn't issue Read Status Enhanced command to do LUN selection, LUN0's parameter page will be read out by default.
2. All LUNs have the same parameter page for multi-LUN configuration.

Table 74. Parameter Page Data (TBD)

All TBD items are 00h or other data temporarily. They will be updated in later version.

Byte	Value	Description
Revision information and features block		
0-3	4Fh 4Eh 46h 49h	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"
4-5	FEh 03h	Revision number 10-15 Reserved (0) 9 1 = supports ONFI version 4.0 8 1 = supports ONFI version 3.2 7 1 = supports ONFI version 3.1 6 1 = supports ONFI version 3.0 5 1 = supports ONFI version 2.3 4 1 = supports ONFI version 2.2 3 1 = supports ONFI version 2.1 2 1 = supports ONFI version 2.0 1 1 = supports ONFI version 1.0 0 Reserved (0)
6-7	DAh FDh	Features supported 15 1 = supports package electrical specification 14 1 = supports ZQ calibration 13 1 = supports NV-DDR3 12 1 = supports external VPP 11 1 = supports volume addressing 10 1 = supports NV-DDR2

Byte	Value	Description
		9 1 = supports EZ NAND 8 1 = supports program page register clear enhancement 7 1 = supports extended parameter page 6 1 = supports multi-plane read operations 5 1 = supports NV-DDR 4 1 = supports odd to even page Copyback 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width
8-9	FFh 3Eh	Optional commands supported 14-15 Reserved (0) 13 1 = supports ZQ calibration (long and short) 12 1 = supports LUN Get and LUN Set Features 11 1 = supports ODT configure 10 1 = supports Volume Select 9 1 = supports Reset LUN 8 1 = supports Small Data Move 7 1 = supports Change Row Address 6 1 = supports Change Read Column Enhanced 5 1 = supports Read Unique ID 4 1 = supports Copyback 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache commands 0 1 = supports Page Cache Program command
10	0Fh	ONFI-JEDEC JTG primary advanced command support 4-7 Reserved (0) 3 1 = supports Multi-plane Block Erase 2 1 = supports Multi-plane Copyback Program 1 1 = supports Multi-plane Page Program 0 1 = supports Random Data Out
11	00h	Reserved (0)
12-13	All 00h	Extended parameter page length
14	10h	Number of parameter pages
15-31	All 00h	Reserved (0)
Manufacturer information block		
32-43	59h,4Dh,54h,43h,20h 20h,20h,20h,20h,20h	Device manufacturer (12 ASCII characters) YMTC

Byte	Value	Description
	20h,20h	
44-63	BGA132 64GB: 59h,4Dh,4Eh,30h,38h, 54h,45h,31h,42h,31h, 44h,43h,33h,42h,00h, 00h, 00h,00h,00h,00h 128GB: 59h,4Dh,4Eh,30h,38h, 54h,45h,31h,42h,31h, 48h,43h,33h,42h,00h, 00h, 00h,00h,00h,00h 256GB: 59h,4Dh,4Eh,30h,38h, 54h,45h,31h,42h,31h, 52h,43h,33h,42h,00h, 00h, 00h,00h,00h,00h BGA272 128GB: 59h,4Dh,4Eh,30h,38h, 54h,45h,31h,42h,33h, 51h,43h,33h,42h,00h, 00h, 00h,00h,00h,00h 256GB: 59h,4Dh,4Eh,30h,38h, 54h,45h,31h,42h,33h, 4Bh,43h,33h,42h,00h, 00h, 00h,00h,00h,00h 256GB: 59h,4Dh,4Eh,30h,38h, 54h,45h,31h,42h,33h, 4Ch,43h,33h,42h,00h, 00h, 00h,00h,00h,00h 512GB: 59h,4Dh,4Eh,30h,38h, 54h,45h,31h,42h,33h, 50h,43h,33h,42h,00h, 00h, 00h,00h,00h,00h Wafer:	Device model (20 ASCII characters) DDP BGA132 64GB: YMN08TE1B1DC3B QDP BGA132 128GB: YMN08TE1B1HC3B ODP BGA132 256GB: YMN08TE1B1RC3B QDP BGA272 128GB: YMN08TE1B3QC3B ODP BGA272 256GB: YMN08TE1B3KC3B ODP BGA272 256GB: YMN08TE1B3LC3B HDP BGA272 512GB: YMN08TE1B3PC3B Wafer: YMN08TE1W00C3B

Byte	Value	Description
	59h,4Dh,4Eh,30h,38h, 54h,45h,31h,57h,30h, 30h,43h,33h,42h,00h, 00h, 00h,00h,00h,00h	
64	9Bh	JEDEC manufacturer ID
65-66	Dynamic	Date code
67-79	All 00h	Reserved (0)
Memory organization block		
80-83	00h 40h 00h 00h	Number of data bytes per page
84-85	00h 08h	Number of spare bytes per page
86-91	All 00h	Reserved (0)
92-95	80h 04h 00h 00h	Number of pages per block
96-99	DCh 07h 00h 00h	Number of blocks per logical unit (LUN)
100	64GB: 02h 128GB：04h 256GB: 08h 512GB: 10h Wafer: 01h	Number of logical units (LUNs)
101	24h	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles
102	03h	Number of bits per cell
103-104	TBD	Bad blocks maximum per LUN
105-106	TBD	Block endurance, Value * $10^{multiplier}$ byte 105=value byte 106=multiplier
107	04h	Guaranteed valid blocks at beginning of target
108-109	TBD	Block endurance for guaranteed valid blocks
110	01h	Number of programs per page

Byte	Value	Description
111	00h	Reserved (0)
112	78h	Number of bits ECC correctability
113	01h	Number of plane address bits 4-7 Reserved (0) 0-3 Number of plane address bits
114	16h	Multi-plane operation attributes 6-7 Reserved (0) 5 1 = lower bit XNOR block address restriction 4 1 = read cache supported 3 1 =address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 1 =overlapped interleaving support 0 = concurrent interleaving support
115-127	All 00h	Reserved (0)
Electrical parameters block		
128	03h	I/O pin capacitance
129-130	3Fh 00h	SDR Timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1
131-132	All 00h	Reserved (0)
133-134	TBD	tPROG Maximum page program time (µs)
135-136	TBD	tBERS Maximum block erase time (µs)
137-138	TBD	tR Maximum page read time (µs)
139-140	90h 01h	tCCS Minimum change column setup time (ns)
141	00h	NV-DDR timing mode support 6-7 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode1 0 1 = supports timing mode 0

Byte	Value	Description
142	FFh	NV-DDR2 timing mode support 7 1 = supports timing mode 7 6 1 = supports timing mode 6 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode1 0 1 = supports timing mode 0
143	08h	NV-DDR2 features 4-7 Reserved (0) 3 1 = device requires Vpp enablement sequence 2 1 = device supports CLK stopped for data input 1 1 = typical capacitance values present 0 1=tCAD value to use
144-145	All 00h	Reserved (0)
146-147	02h	I/O pin capacitance, typical
148-149	02h	Input pin capacitance, typical
150	03h	Input pin capacitance, maximum
151	03h	Driver strength support 3-7 Reserved (0) 2 1 = supports 18 Ohms drive strength 1 1 = supports 25 Ohms drive strength 0 1 = supports driver strength settings
152-153	TBD	tR Maximum multi-plane page read time (µs)
154-155	2Ch 01h	tADL Program page register clear enhancement tADL value (ns)
156-157	All 00h	Reserved (0)
158	3Bh	NV-DDR2/3 features 6-7 Reserved (0) 5 1 = external V_{REFQ} required for ≥ 200 MT/s 4 1 = supports differential signaling for DQS 3 1 = supports differential signaling for RE_n 2 1 = supports ODT value of 30 Ohms 1 1 = supports matrix termination ODT 0 1 = supports self-termination ODT
159	44h	NV-DDR2/3 warmup cycles 4-7 Data Input warmup cycles support 0-3 Data Output warmup cycles support

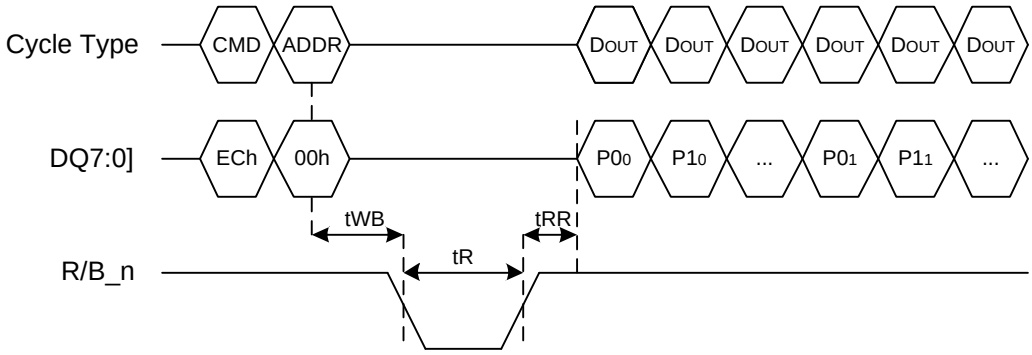
Byte	Value	Description
160-161	FFh 00h	NV-DDR3 timing mode support 8-15 Reserved (0) 7 1 = supports timing mode 10 6 1 = supports timing mode 9 5 1 = supports timing mode 8 4 1 = supports timing mode 7 3 1 = supports timing mode 6 2 1 = supports timing mode 5 1 1 = supports timing mode 4 0 1 = supports timing modes 0-3
162	01h	NV-DDR2 timing mode support 3-7 Reserved (0) 2 1 = supports NV-DDR2 timing mode 10 1 1 = supports NV-DDR2 timing mode 9 0 1 = supports NV-DDR2 timing mode 8
163	00h	Reserved (0)
Vendor Block		
164-165	01h 00h	Vendor specific Revision number
166-167	FFh 06h	Vendor specific command supported 11-15 Reserved (0) 10 1 = supports synchronous reset 9 1 = supports one-pass programming 8 1 = supports initialization read retry 7 1 = supports hard reset 6 1 = supports program suspend/resume 5 1 = supports erase suspend/resume 4 1 = supports erased page check 3 1 = supports read status enhanced II 2 1 = support fast partial page read 1 1 = supports SLC mode 0 1 = supports soft data single bit read
168-169	CFh DEh	Vendor specific feature supported 15 1 = supports enhanced slc mode 14 1 = supports write protection 13 1 = CE_n pin reduction 12 1 = supports temperature sensor readout 11 1 = supports internal VREFQ 10 1 = supports target sleep mode

Byte	Value	Description
		9 1 = supports lun sleep mode 8 1 = supports R/B_n configuration 7 1 = supports page buffer operation 6 1 = supports signal integrity check 5 1 = supports automatic read level calibration 4 1 = supports fast buffer release 3 1 = supports read offset 2 1 = supports cell mode 1 1 = supports peak power limitation 0 1 = supports power interruption detection mode
170	07h	Additional driver strength settings 3-7 Reserved (0) 2 1 = supports 50 Ohms drive strength 1 1 =supports 35 Ohms drive strength 0 1 = supports programmable output drive strength
171-253	All 00h	Reserved (0)
254-255	CRC Calculation	Integrity CRC[1]
Redundant Parameter Pages (15 copies)		
256-511	Copy 1	Value of Bytes 0-255
512-767	Copy 2	Value of Bytes 0-255
...		Value of Bytes 0-255
3840-4095	Copy 15	Value of Bytes 0-255

Notes:

1. The integrity CRC (Cyclic Redundancy Check) field is used to verify that the contents of the parameter page were transferred correctly to the host. The CRC of the parameter page is a word (16-bit) field. The CRC calculation covers all of data between byte 0 and byte 253 of the parameter page inclusive. The CRC shall be calculated on byte (8-bit) quantities starting with byte 0 in the parameter page. The bits in the 8-bit quantity are processed from the most significant bit (bit 7) to the least significant bit (bit 0). The CRC shall be calculated using the following 16-bit generator polynomial: G(X) = X16 + X15 + X2 + 1. The polynomial in hex may be represented as 8005h. The CRC value shall be initialized with a value of 4F4Eh before the calculation begins. There is no XOR applied to the final CRC value after it is calculated. There is no reversal of the data bytes or the CRC calculated value.

Figure 52. Read Parameter Page Sequence



6.3.4. Read Status (70h)

After issuing the Read Status command to the command register, a read cycle outputs the content of the Status Register to the DQ pins at the falling edge of CE_n or RE_n, whichever occurs last. Updated status can be read by toggling CE_n or RE_n. Note that before the Read Status command is issued, a single LUN should be selected.

For single plane operation, the Read Status command returns the value in the status register which reflects the status of last operation. For multi-plane operation, the Read Status returns the composite value for status register bits that are independent per plane. See **Table 75 "Composite Status Value"**.

The Read Status command may be issued using the SDR, NV-DDR2 or NV-DDR3 data interfaces. When issuing Status Read in the NV-DDR2 or NV-DDR3 data interface, each data byte is received twice. The host shall only latch one copy of each data byte.

Once device enters into Read Status mode, the command register remains in Read Status command mode until another valid command is written to the command register.

Table 75. Composite Status Value

Status Register Bit	Composite Status Value
Bit 0, FAIL	OR
Bit 1, FAIL C	OR

Table 76. Status Register Definition

Bit	Status Register	Page Program	Block Erase	Read	Cache Read	Cache Program	Definition
7	WPN	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected: "0" Not Protected: "1"

6	RDY	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Data Cache Read/Busy Busy: "0" Ready: "1"
5	ARDY	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready /Busy	Flash Array Read/Busy Busy: "0" Ready: "1"
4	PDD	Detection	Detection	Detection	Detection	Detection	Power Droop Detection Not Detected: "0" Detected: "1"
3	ESPD	N/A	Suspend	N/A	N/A	N/A	Erase Suspend Not Suspended: "0" Suspended: "1"
2	PSPD	Suspend	N/A	N/A	N/A	Suspend	Program Suspend Not Suspended: "0" Suspended: "1"
1	FAILC	N/A	N/A	N/A	N/A	Pass/Fail	command issued prior to the last command Pass: "0" Fail: "1"
0	FAIL	Pass/Fail	Pass/Fail	N/A	N/A	Pass/Fail	Last command Pass: "0" Fail: "1"

Notes:

1. If the RDY bit is cleared to zero, all other bits in the status byte (except WP_n) are invalid and shall be ignored by the host. This bit impacts the value of R/B_n;
2. FAILC bit is not valid until after the second 15h command or the 10h command has been transferred in a Page Cache Program sequence. When program cache is not supported, this bit is not used and shall be cleared to zero.

Figure 53. Read Status Sequence

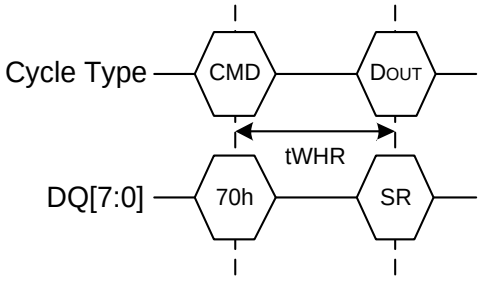


Figure 54. Read Status Timing (SDR)

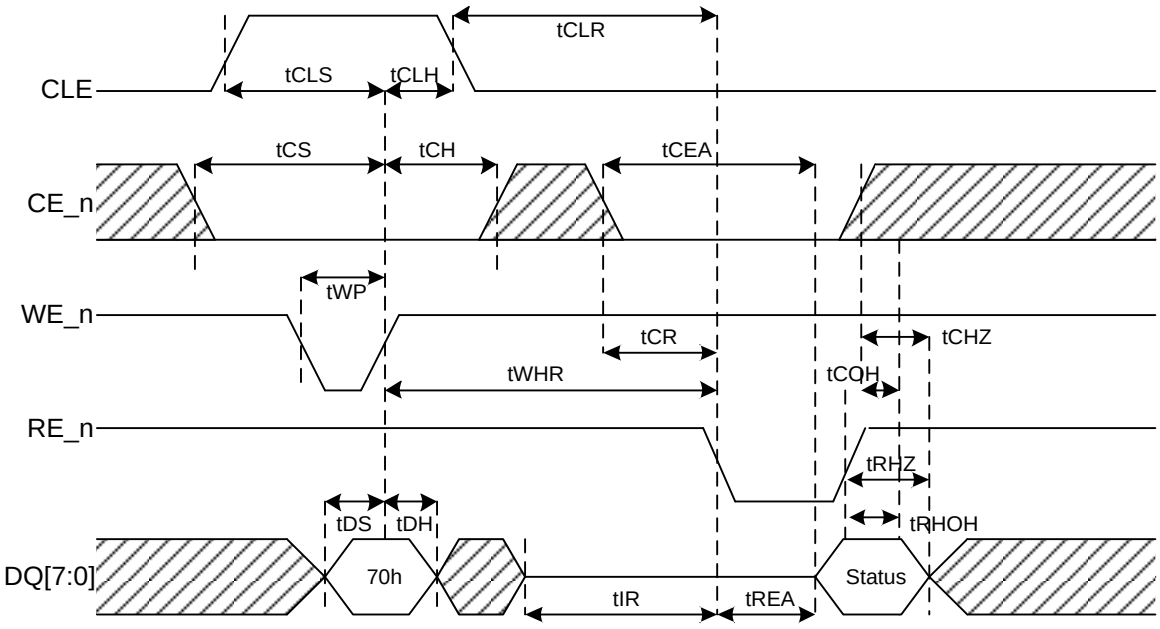
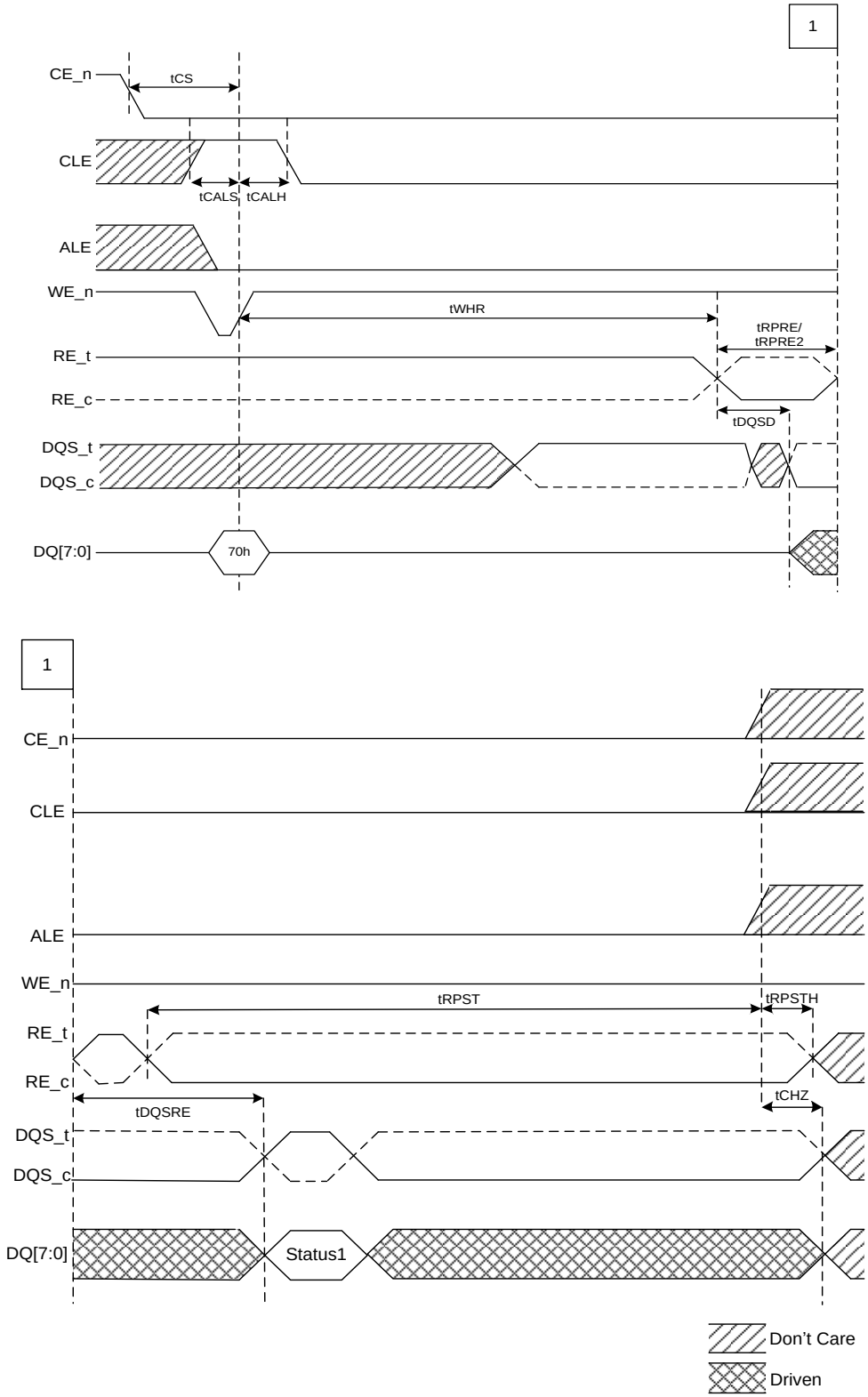


Figure 55. Read Status Timing (NV-DDR2/NV-DDR3)



Notes:

When the bus state is not a data input or data output cycle, if ALE, CLE and CE_n are all low (i.e. Idle state) then DQS (DQS_t) shall be held high by the host to prevent the device from enabling ODT. If ODT is disabled, then DQS is Don't Care during Idle states.

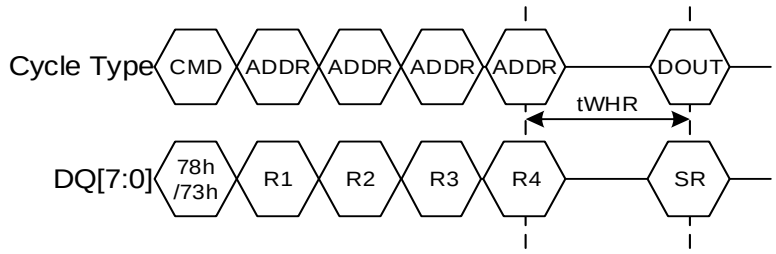
6.3.5. Read Status Enhanced (78h)

The Read Status Enhanced command retrieves the status value for a previous operation on the particular LUN and plane address specified. Therefore, each status register bit is dedicated for a single plane, not a composite value. For Multi-Plane operation, Host should check the Pass/Fail status on both planes by issue different plane addresses. If the row address entered is invalid, the status value returned has an indeterminate value. The host uses the Read Status Enhanced command for LUN selection. Note that Read Status Enhanced has no effect on which page buffer is selected for data output within the LUN.

The Read Status Enhanced II (73h) command retrieves the status value for a previous operation on the particular LUN. For Multi-Plane operation, the host should check the Pass/Fail status on both planes based on Bit [3:0] values. The host uses the Read Status Enhanced II command for LUN selection. Note that Read Status Enhanced II has no effect on which page buffer is selected for data output within the LUN.

When issuing Read Status Enhanced or Read Status Enhanced II in the NV-DDR2 or NV-DDR3 data interface, each data byte is received twice. The host shall only latch one copy of each data byte.

Figure 56. Read Status Enhanced Sequence



Notes:

R1-R4: Row addresses that contain the LUN and plane address to retrieve status. Row address bits not associated with the LUN and plane address are not used. R1 is the least significant byte.

Table 77. Read Status Enhanced Definition

Bit	Status Register	Page Program	Block Erase	Read	Cache Read	Cache Program	Definition
7	WPN	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected: "0" Not Protected: "1"

Bit	Status Register	Page Program	Block Erase	Read	Cache Read	Cache Program	Definition
6	RDY	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Data Cache Read/Busy Busy: "0" Ready: "1"
5	ARDY	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready /Busy	Flash Array Read/Busy Busy: "0" Ready: "1"
4	N/A	N/A	N/A	N/A	N/A	N/A	N/A
3	N/A	N/A	N/A	N/A	N/A	N/A	N/A
2	N/A	N/A	N/A	N/A	N/A	N/A	N/A
1	Plane FAILC[1]	N/A	N/A	N/A	N/A	Pass/Fail	Command Issued Prior to the Last Command Pass: "0"' Fail: "1"
0	Plane FAIL[1]	Pass/Fail	Pass/Fail	N/A	N/A	Pass/Fail	Last Command Pass: "0"' Fail: "1"

Notes:

1. Based on the plane address input, the Plane FAIL and Plane FAILC status reports Plane pass/fail status; If the RDY bit is cleared to zero, all other bits in the status byte (except WP_n) are invalid and shall be ignored by the host. This bit impacts the value of R/B_n;
2. Plane FAILC bit is not valid until after the second 15h command or the 10h command has been transferred in a Page Cache Program sequence. When program cache is not supported, this bit is not used and shall be cleared to zero.

Table 78. Read Status Enhanced II Definition

Bit	Status Register	Page Program	Block Erase	Read	Cache Read	Cache Program	Definition
7	WPN	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected: "0" Not Protected: "1"
6	RDY	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Data Cache Read/Busy Busy: "0" Ready: "1"
5	ARDY	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready /Busy	Flash Array Read/Busy Busy: "0" Ready: "1"
4	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Bit	Status Register	Page Program	Block Erase	Read	Cache Read	Cache Program	Definition
3	Plane1 FAILC[1]	N/A	N/A	N/A	N/A	Pass/Fail	Command Issued Prior to the Last Command Pass: "0" Fail: "1"
2	Plane1 FAIL[1]	Pass/Fail	Pass/Fail	N/A	N/A	Pass/Fail	Last Command Pass: "0" Fail: "1"
1	Plane0 FAILC[1]	N/A	N/A	N/A	N/A	Pass/Fail	Command Issued Prior to the Last Command Pass: "0" Fail: "1"
0	Plane0 FAIL[1]	Pass/Fail	Pass/Fail	N/A	N/A	Pass/Fail	Last Command Pass: "0" Fail: "1"

Notes:

1. Based on the plane address input, the Plane FAIL and Plane FAILC status reports Plane pass/fail status; Plane FALC bit is not valid until after the second 15h command or the 10h command has been transferred in a Page Cache Program sequence. When program cache is not supported, this bit is not used and shall be cleared to zero.
2. If the RDY bit is cleared to zero, all other bits in the status byte (except WP_n) are invalid and shall be ignored by the host. This bit impacts the value of R/B_n;

6.3.6. Page Read (00h-30h)

This Page Read command is used to read a page of data (16K+2048bytes) identified by a row address for the LUN specified. The page of data is made available to be read from the page buffer starting at the column address specified.

The page of data is transferred to the page buffer within tR (transfer from flash array to page buffer). The host may detect the completion of this data transfer (tR) by either checking the R/B_n pin level, or issuing the Read Status commands and monitoring SR[6] (ready/busy) through RE_n toggling. After Read Status is complete, the host shall re-issue a command value of 00h to start reading data. The device may output random data in a page instead of the consecutive sequential data by writing Change Read Column (05h-E0h) or Change Read Column Enhanced (06h-E0h) command. Change Read Column can be operated multiple times regardless of how many times it is done in a page. In between 05h-E0h or 06h-E0h on the same page, there should not be any other operation. Otherwise the date stored in the page buffer would be lost.

Reading beyond the end of a page results in invalid values returned to the host. Within one page read, device output is undetermined if the host continues toggling RE_n after last byte has been read out.

Figure 57. Page Read Sequence

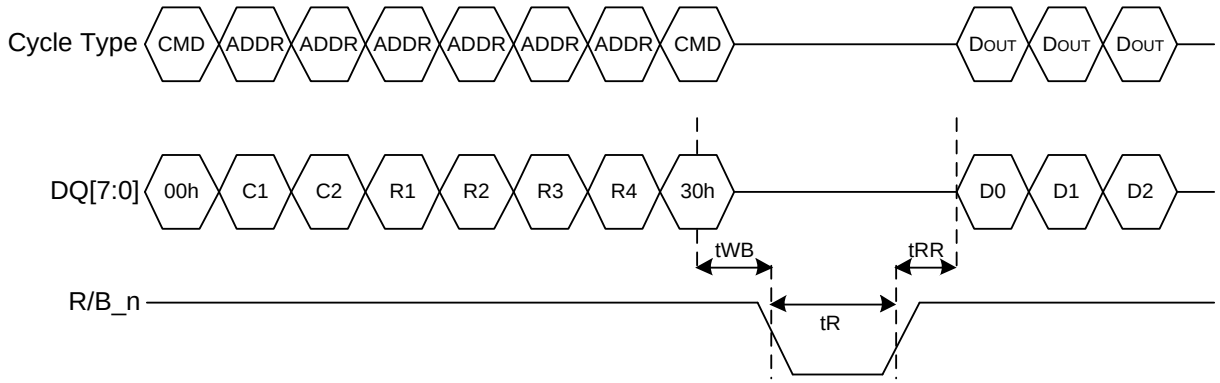
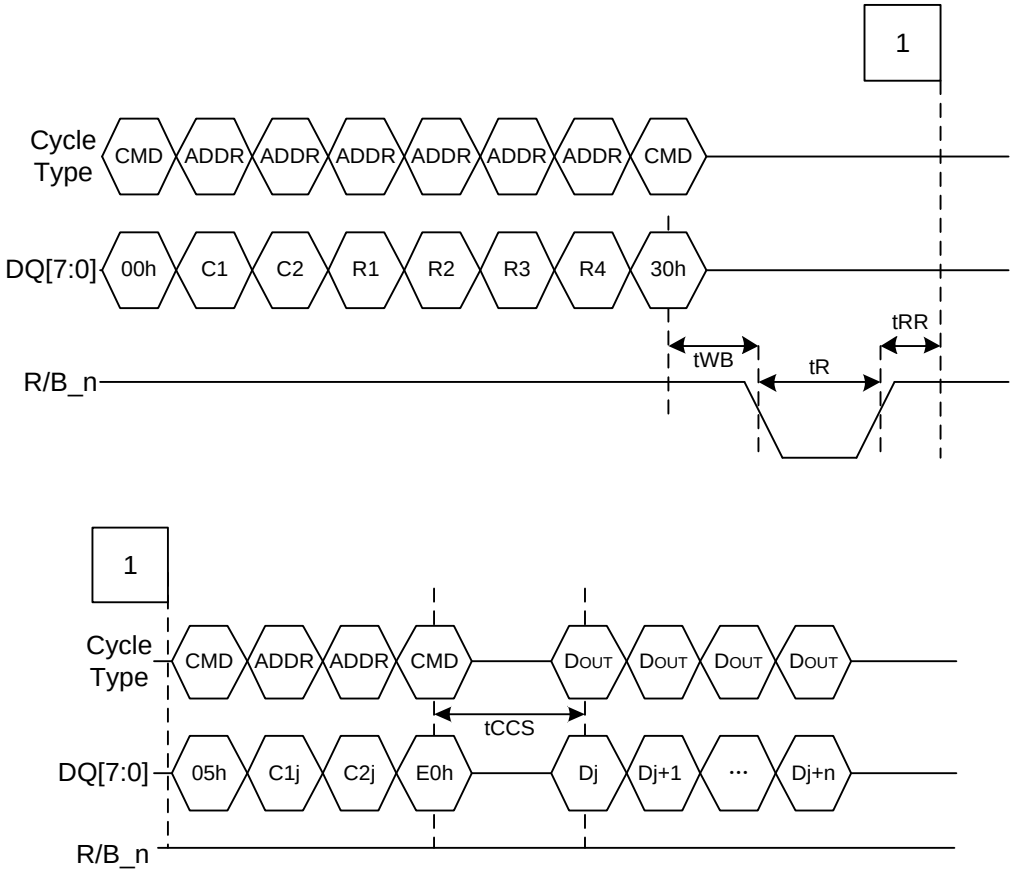
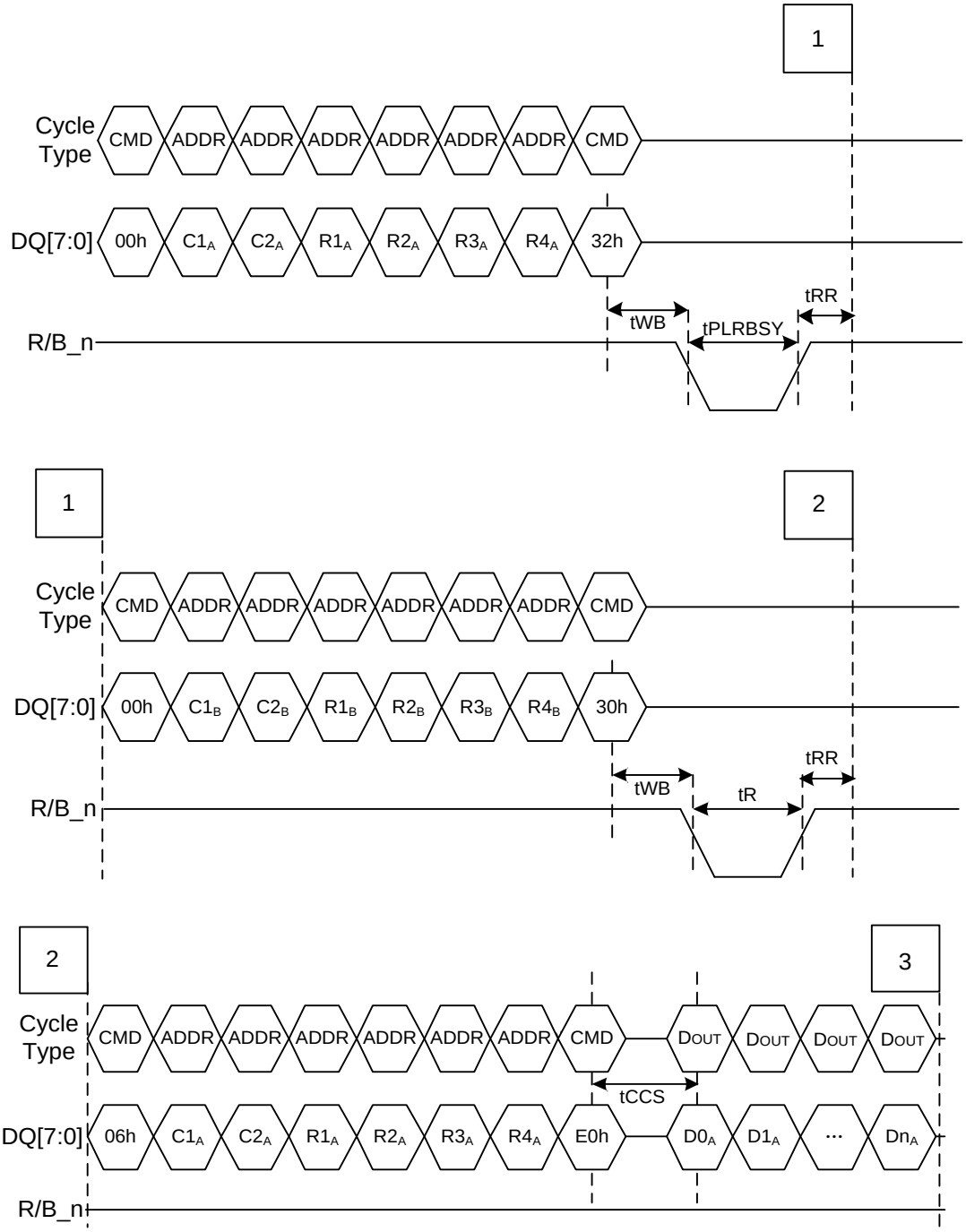


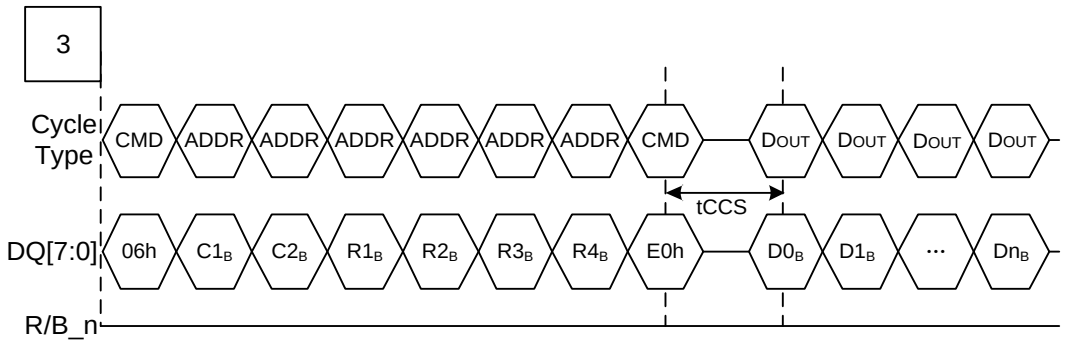
Figure 58. Page Read with Random Data Output Sequence



This NAND device supports multi-plane operation. Multi-Plane Page Read sequence is shown as below. For multi-plane page read, plane A & B should have the same page address. Different page read between two planes within one multi-plane page read command is not supported.

Figure 59. Multi-Plane Page Read Sequence





6.3.7. Cache Read

The Cache Read function includes Sequential Cache Read (31h) and Random Cache read (00h-31h), which permit a page to be read from the page buffer while another page is simultaneously read from the Flash array. The Page Read (00h-30h) command shall be issued prior to the initial Sequential or Random Cache Read command in a Cache Read sequence.

The first Cache Read command (Sequential or Random) shall be issued after the Page Read operation is complete (SR[6] is set to one). The host may enter the address of the next page to be read from the Flash array by issuing 00h. If the host does not enter an address to retrieve, the next sequential page is read. For both Sequential and Random Cache Read, data output always begins at column address 00h if no Random data output is required by the host. The device may output random data in a page instead of the consecutive sequential data by writing Change Read Column (05h-E0h) or Change Read Column Enhanced (06h-E0h) command.

When the Cache Read command (Sequential or Random) is issued, SR[6] is cleared to zero (busy). After the operation is complete and SR[6] is set to one (ready), the host may begin to read the data from the previous Page Read or Cache Read (Sequential or Random) operation. Issuing an additional Cache Read (Sequential or Random) command copies the data most recently read from the array into the page buffer. When no more pages are to be read, the final page is copied into the page buffer by issuing the Cache Read End (3Fh) command.

The host shall not issue a Sequential Cache Read command after the last page of a block is read. If commands are issued to multiple LUNs at the same time, the host shall execute a Read Status Enhanced (78h) command to select the LUN prior to issuing a Sequential Cache Read or Cache Read End command for that LUN.

Figure 60. Sequential Cache Read Sequence

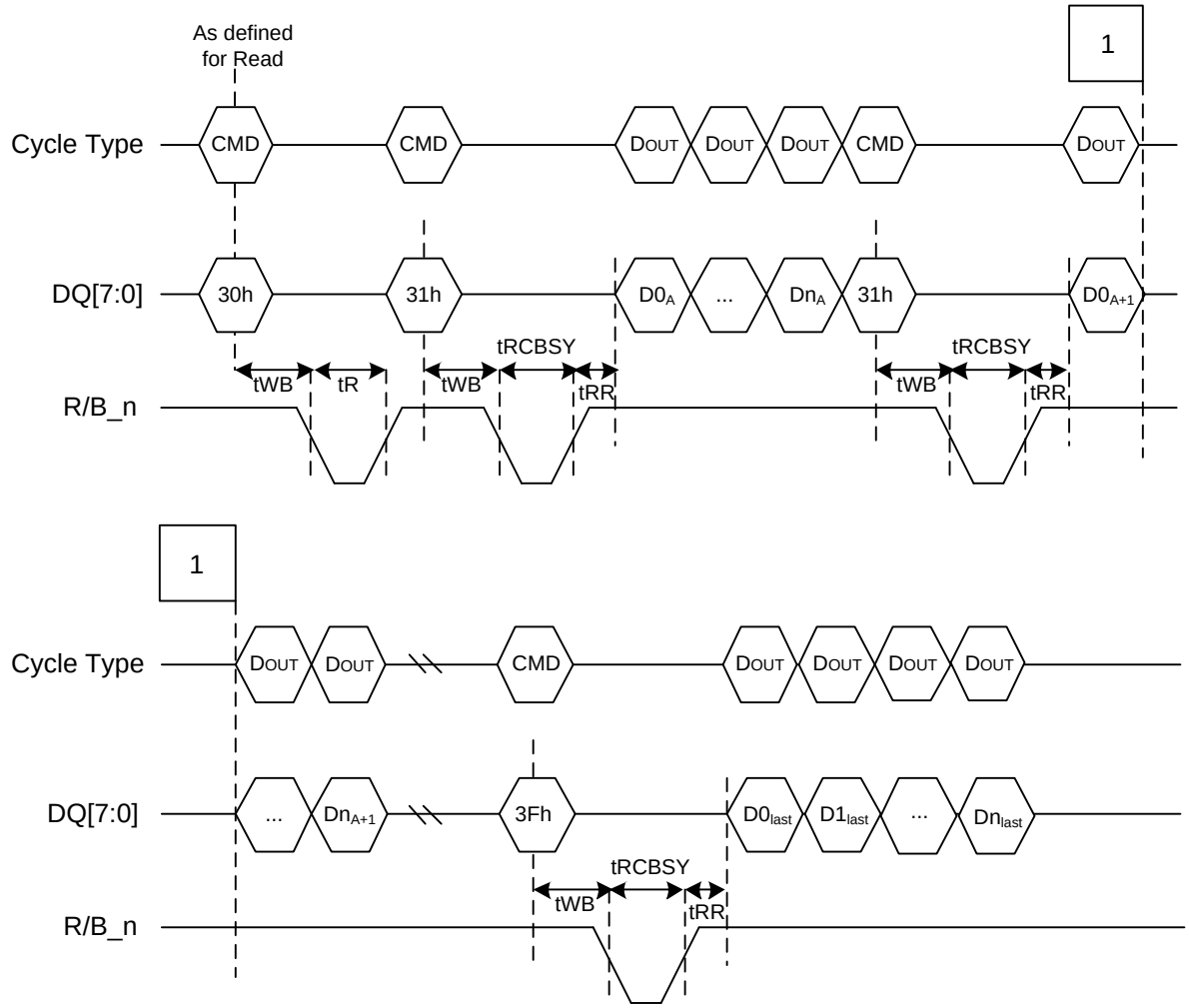


Figure 61. Sequential Cache Read Random Data Output Sequence

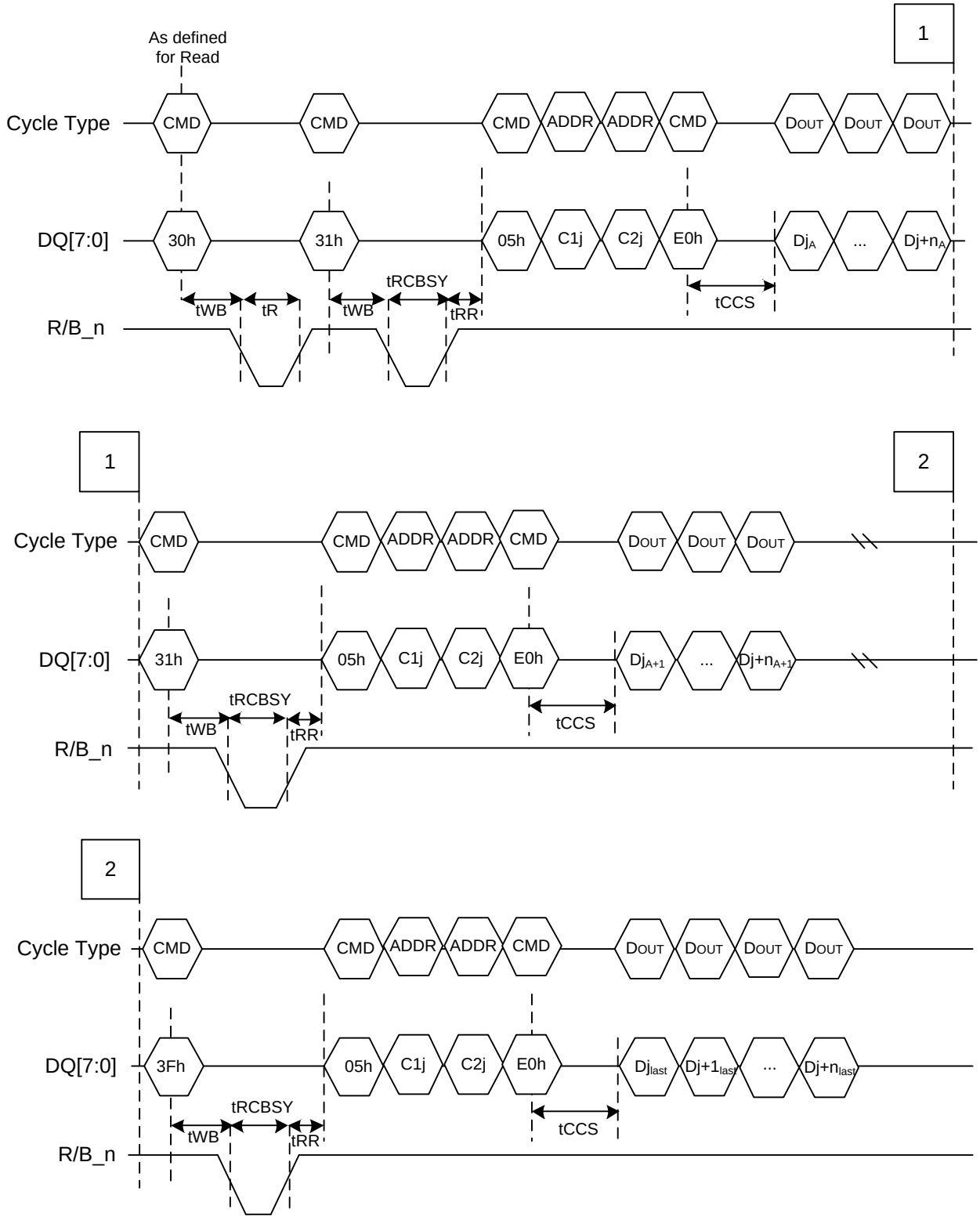


Figure 62. Random Cache Read Sequence

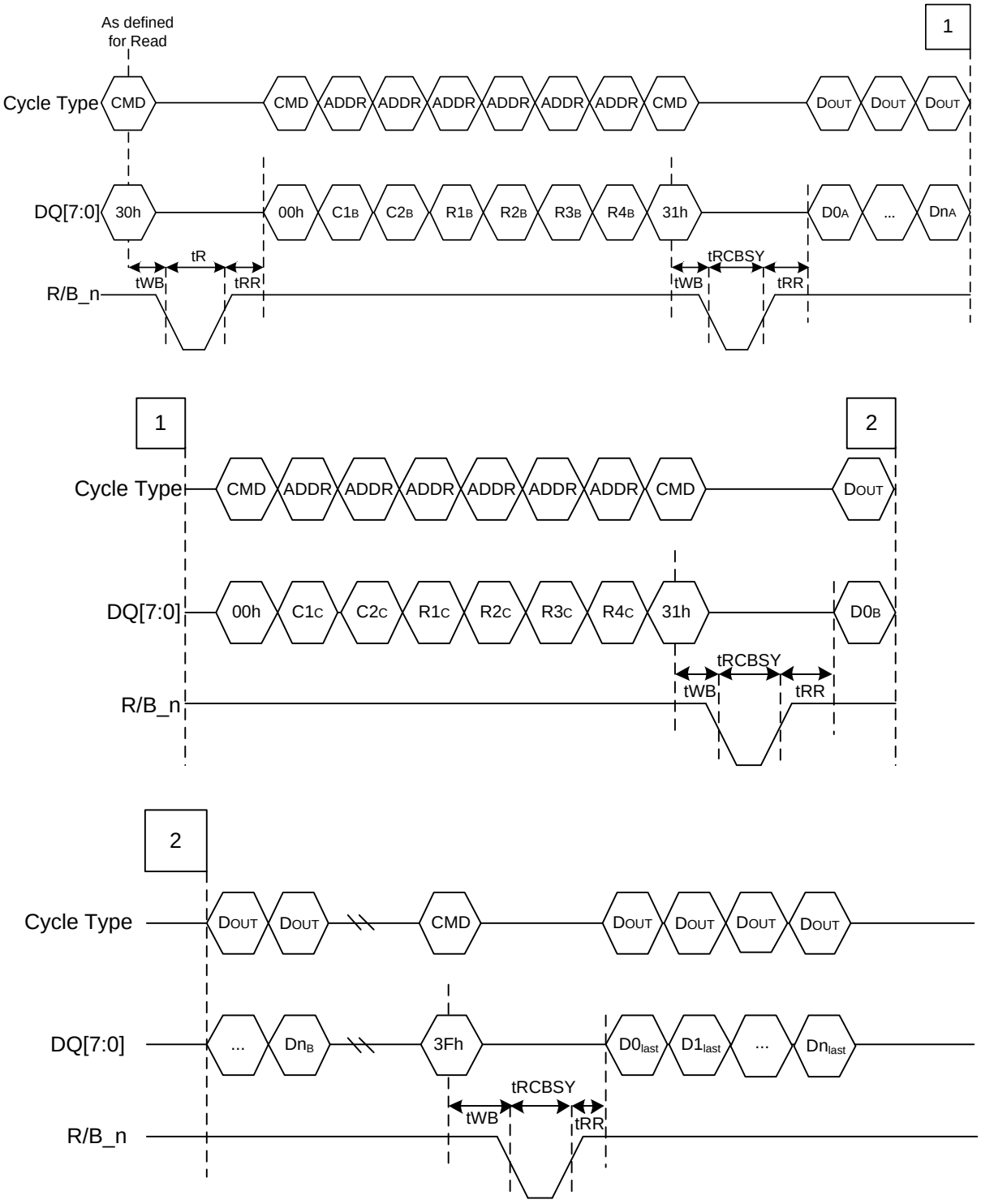
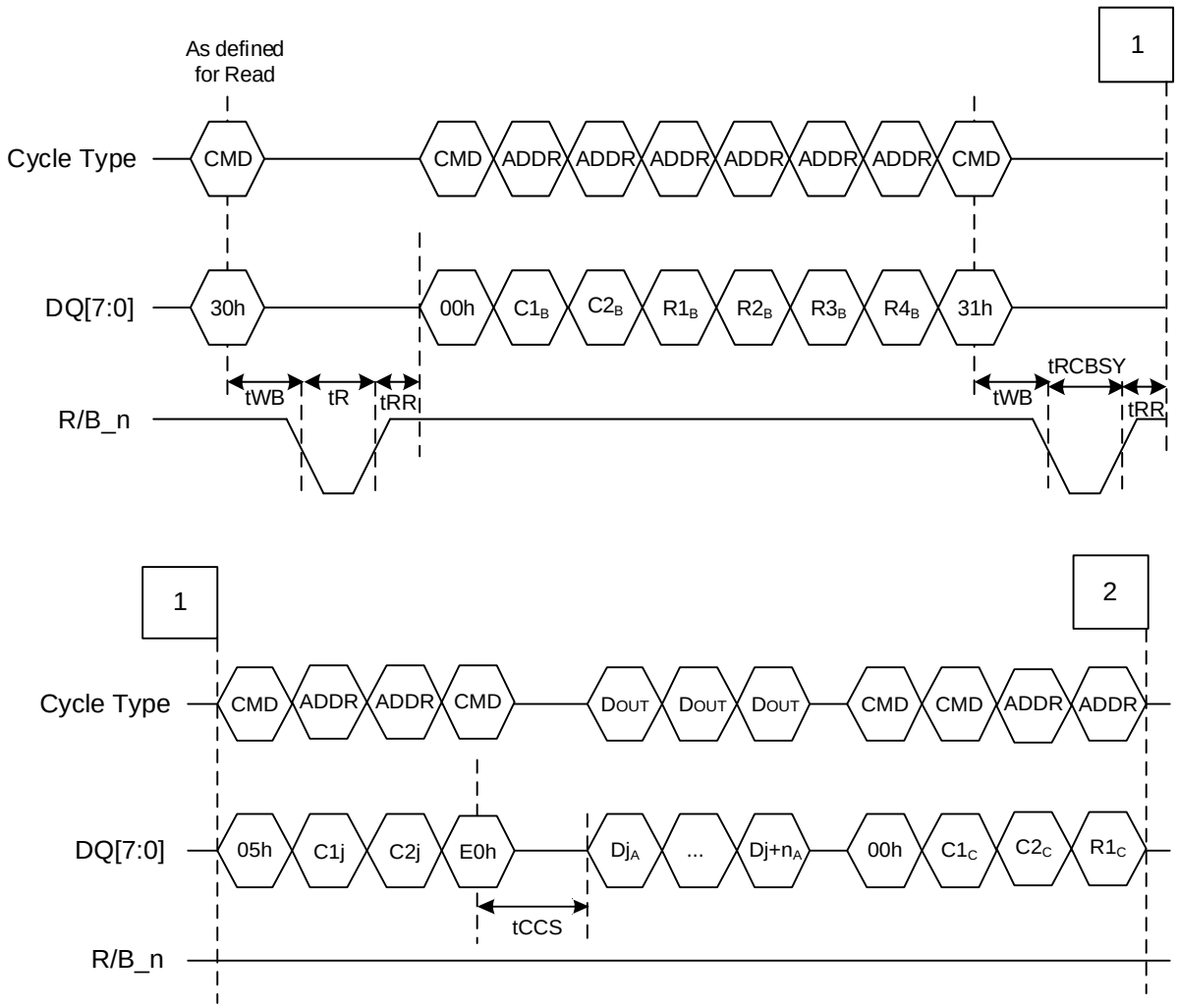
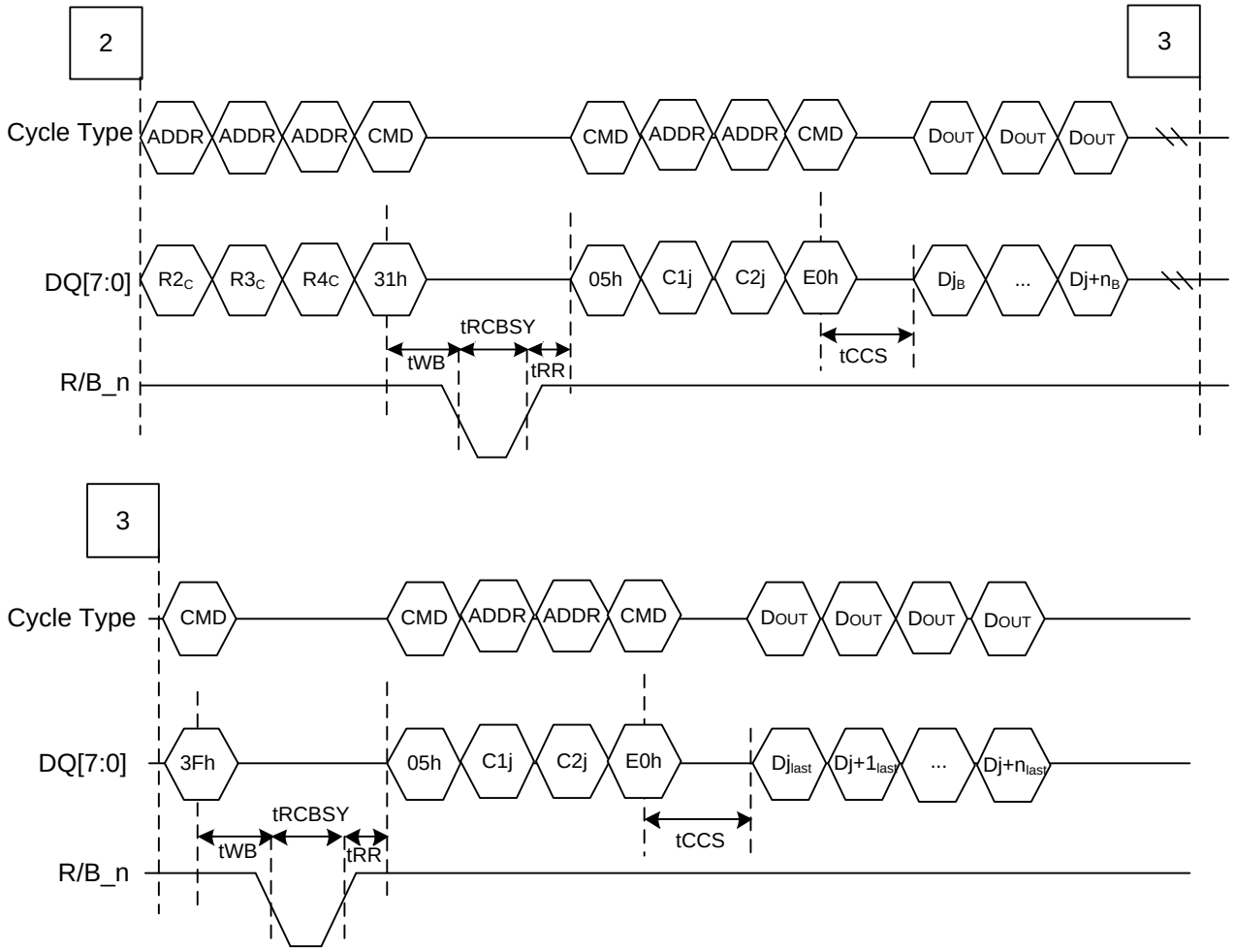


Figure 63. Random Cache Read Random Data Output Sequence





This NAND device supports multi-plane operation. Multi-Plane Sequential Cache Read sequence and Multi-Plane Random Cache Read sequence are shown as below. For multi-plane Cache Read, plane A & B should have the same page address. Different page read between two planes within one multi-plane page read command is not supported.

Figure 64. Multi-Plane Sequential Cache Read Sequence

<CMD:00h> <ADD:Column&Row(PlaneA/pageA)> <CMD:32h> tWB tPLRBSY
<CMD:00h> <ADD:Column&Row(PlaneB/pageB)> <CMD:30h> tWB tR
<CMD:31h> tWB tRCBSY tRR
<CMD:06h> <ADD:Column&Row(PlaneA/pageA/columnN)> <CMD:E0h> tCCS
<DOUT:Dn(PlaneA/pageA)> <DOUT:Dn+1(PlaneA/pageA)>...
<CMD:06h> <ADD:Column&Row(PlaneB/pageB/columnN)> <CMD:E0h> tCCS
<DOUT:Dn(PlaneB/pageB)> <DOUT:Dn+1(PlaneB/pageB)>...
<CMD:31h> tWB tRCBSY tRR
<CMD:06h> <ADD:Column&Row(PlaneA/pageA+1/columnN)> <CMD:E0h> tCCS
<DOUT:Dn(PlaneA/pageA+1)> <DOUT:Dn+1(PlaneA/pageA+1)>...

<CMD:06h> <ADD:Column&Row(PlaneB/pageB+1/columnN)> <CMD:E0h> tCCS
<DOUT:Dn(PlaneB/pageB+1)> <DOUT:Dn+1(PlaneB/pageB+1)>…
…
<CMD:3Fh> tWB tRCBSY tRR
<CMD:06h> <ADD:Column&Row(PlaneA/last page/columnN)> <CMD:E0h> tCCS
<DOUT:Dn(PlaneA/last page)> <DOUT:Dn+1(PlaneA/last page)>…
<CMD:06h> <ADD:Column&Row(PlaneB/last page/columnN)> <CMD:E0h> tCCS
<DOUT:Dn(PlaneB/last page)> <DOUT:Dn+1(PlaneB/last page)>…

Figure 65. Multi-Plane Random Cache Read sequence

<CMD:00h> <ADD:Column&Row(PlaneA/pageA)> <CMD:32h> tWB tPLRBSY
<CMD:00h> <ADD:Column&Row(PlaneB/pageB)> <CMD:30h> tWB tR
<CMD:00h> <ADD:Column&Row(PlaneA/pageC)> <CMD:32h> tWB tPLRBSY
<CMD:00h> <ADD:Column&Row(PlaneB/pageD)><CMD:31h> tWB tRCBSY tRR
<CMD:06h> <ADD:Column&Row(PlaneA/pageA/columnN)> <CMD:E0h> tCCS
<DOUT:Dn(PlaneA/pageA)> <DOUT:Dn+1(PlaneA/pageA)>…
<CMD:06h> <ADD:Column&Row(PlaneB/pageB/columnN)> <CMD:E0h> tCCS
<DOUT:Dn(PlaneB/pageB)> <DOUT:Dn+1(PlaneB/pageB)>…
<CMD:00h> <ADD:Column&Row(PlaneA/pageE)> <CMD:32h> tWB tPLRBSY
<CMD:00h> <ADD:Column&Row(PlaneB/pageF)><CMD:31h> tWB tRCBSY tRR
<CMD:06h> <ADD:Column&Row(PlaneA/pageC/columnN)> <CMD:E0h> tCCS
<DOUT:Dn(PlaneA/pageC)> <DOUT:Dn+1(PlaneA/pageC)>…
<CMD:06h> <ADD:Column&Row(PlaneB/pageD/columnN)> <CMD:E0h> tCCS
<DOUT:Dn(PlaneB/pageD)> <DOUT:Dn+1(PlaneB/pageD)>…
…
<CMD:3Fh> tWB tRCBSY tRR
<CMD:06h> <ADD:Column&Row(PlaneA/last page/columnN)> <CMD:E0h> tCCS
<DOUT:Dn(PlaneA/last page)> <DOUT:Dn+1(PlaneA/last page)>…
<CMD:06h> <ADD:Column&Row(PlaneB/last page/columnN)> <CMD:E0h> tCCS
<DOUT:Dn(PlaneB/last page)> <DOUT:Dn+1(PlaneB/last page)>…

6.3.8. Fast Partial Page Read (00h-20h)

The Fast Partial Page Read command provides fastest possible read of a partial page, with 6 address cycles. The row address provides page location, and column address provides which portion in a page will be read. The host can provide any address in the column address range of the chunk to be read. The flexible partial page read operation transfers 4KB+512bytes in NAND array cache register. Any data outside the selected chunk column address range will be invalid.

Multi-Plane Fast Partial Page Read allows the host to read two different 4KB chunk in each plane. The host can input the different initial column address range on each plane to indicate which chunk to read. Fast Partial Page Read doesn't support Cache Read mode.

Figure 66. Fast Partial Page Read Sequence

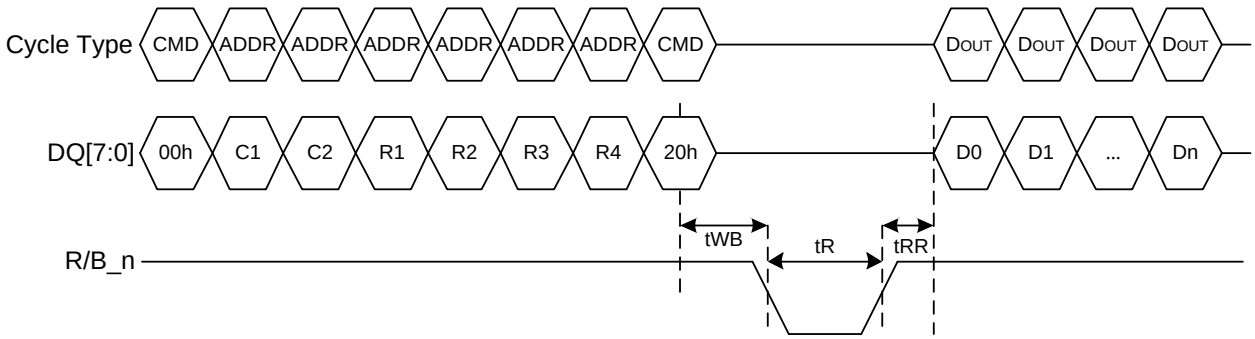
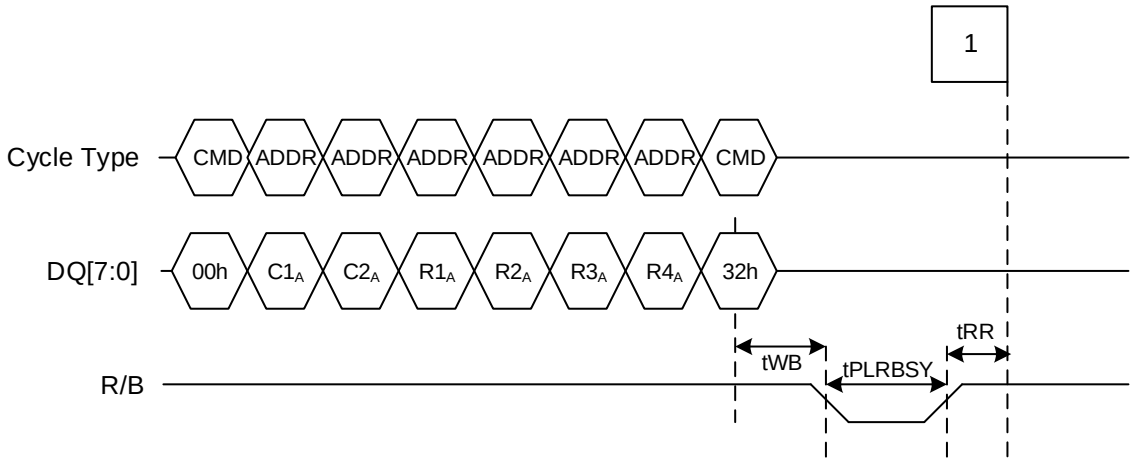


Figure 67. Multi-Plane Fast Partial Page Read Sequence



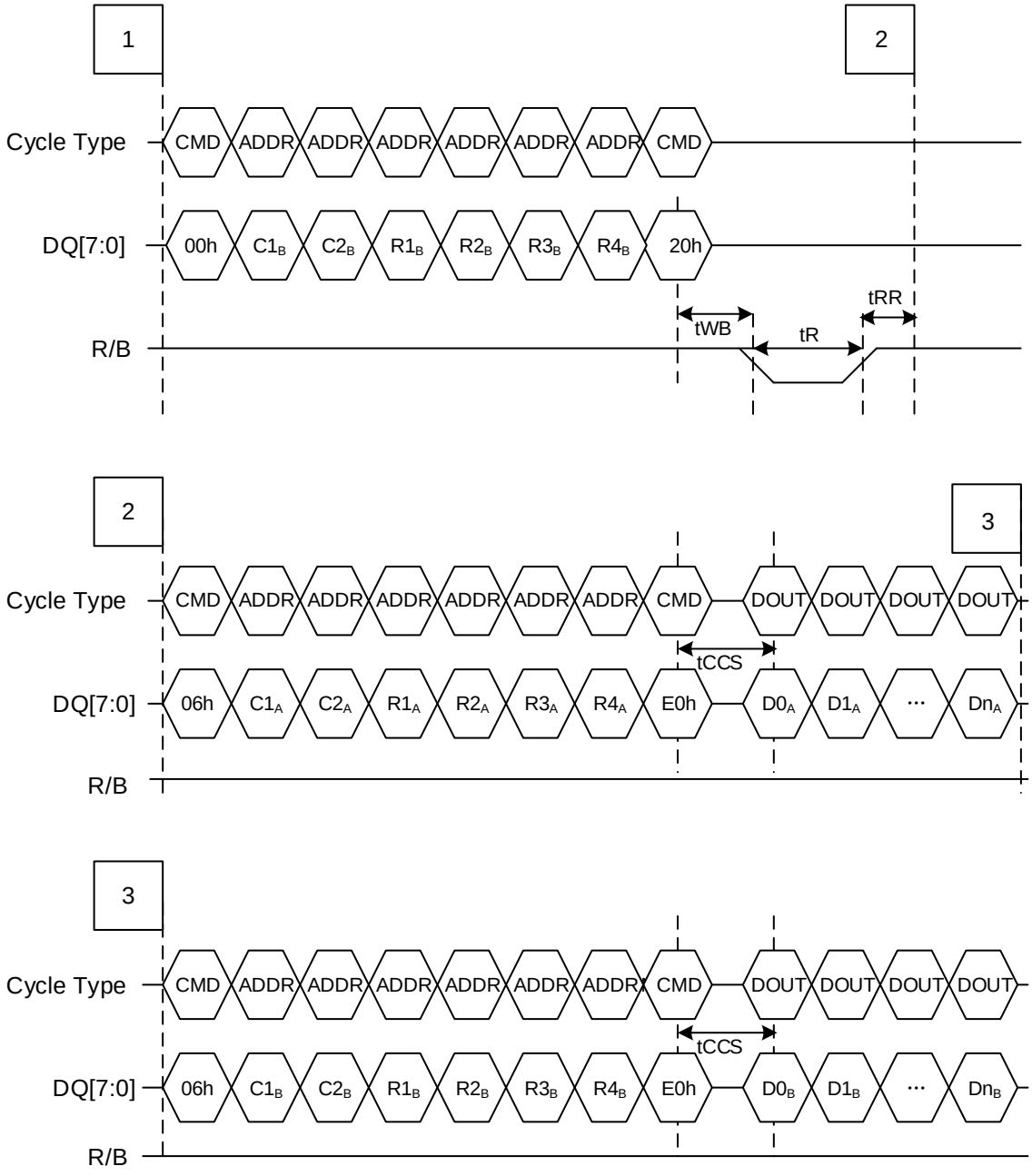


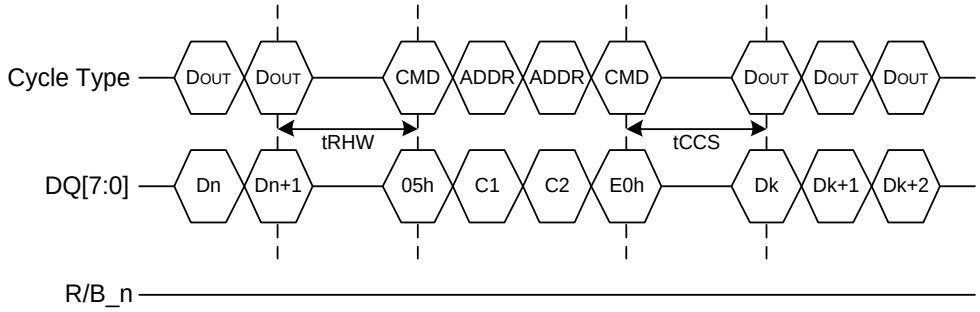
Table 79. Column Address in Fast Partial Page Read

4KB Option	Initial Column Address Range
Chunk 0	0h~11FFh
Chunk 1	1200h~23FFh
Chunk 2	2400h~35FFh
Chunk 3	3600h~47FFh

6.3.9. Change Read Column (05h-E0h)

The Change Read Column command changes the column address from which data is being read in the page buffer for the selected LUN. Change Read Column shall only be issued when the LUN is in a read idle condition. The host shall not read data from the LUN until tCCS ns after the E0h command is written to the LUN. Change Read Column can be operated multiple times regardless of how many times it is done in a page. In between 05h-E0h on the same page, there should not be any other operation. Otherwise the date stored in the page buffer would be lost.

Figure 68. Change Read Column Sequence



6.3.10. Change Read Column Enhanced (06h-E0h)

The Change Read Column Enhanced command changes the LUN address, plane address and column address from which data is being read in a page previously retrieved with the Read command. This command is used when independent LUN operations or multi-plane operations are being performed such that the entire address for the new column needs to be given.

The Change Read Column Enhanced command shall not be issued by the host unless it is supported as indicated in the parameter page. The Change Read Column Enhanced command shall not be issued while Target level data output commands (Read ID, Read Parameter Page, Read Unique ID, Get Features) are executing or immediately following Target level commands.

Change Read Column Enhanced causes idle LUNs (SR[6] is one) that are not selected to turn off their output buffers. This ensures that only the LUN selected by the Change Read Column Enhanced command responds to subsequent data output. If unselected LUNs are active (SR[6] is zero) when Change Read Column Enhanced is issued, then the host shall issue a Read Status Enhanced (78h) command prior to subsequent data output to ensure all LUNs that are not selected turn off their output buffers.

Figure 69. Change Read Column Enhanced Sequence

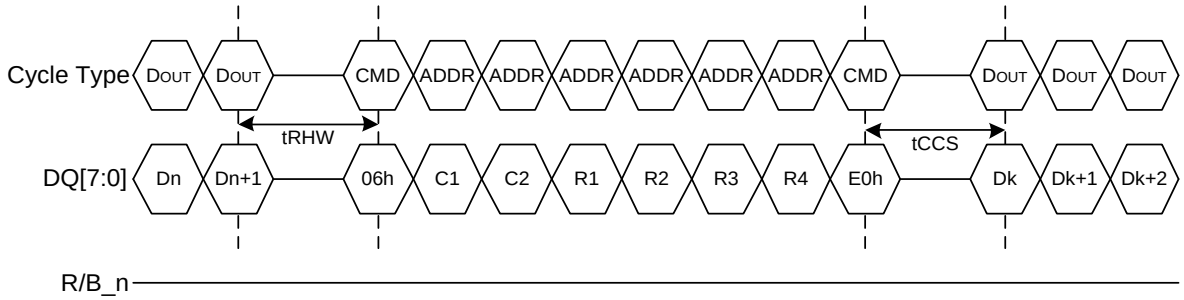
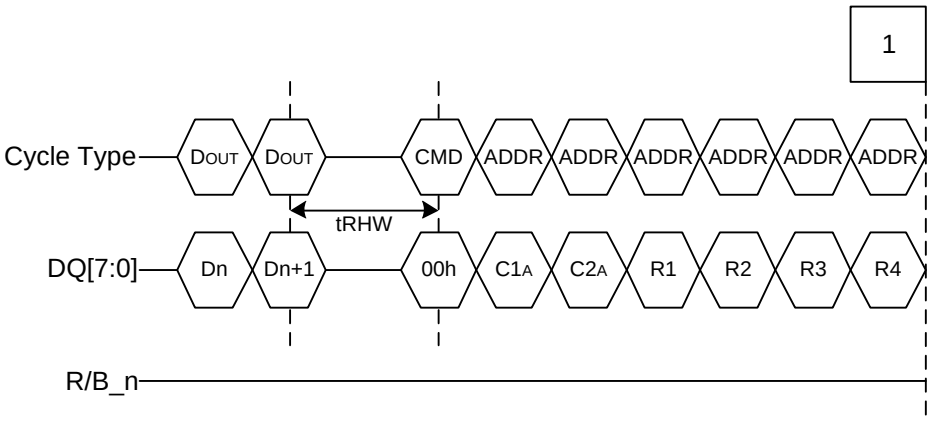
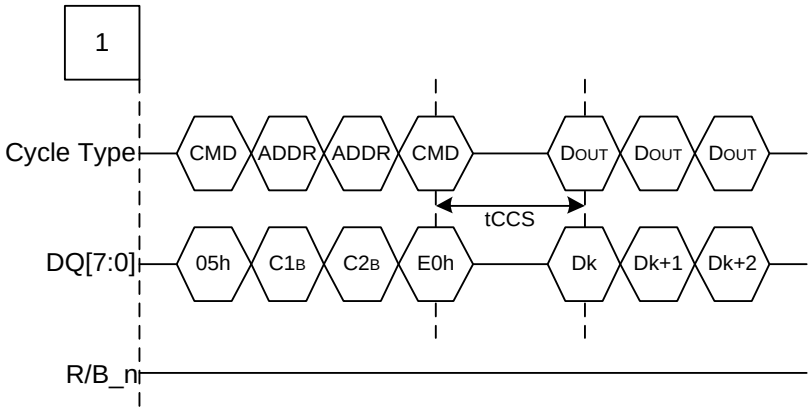


Figure 70. Change Read Column Enhanced Sequence (ONFI-JEDEC Joint Taskgroup Primary Definition)



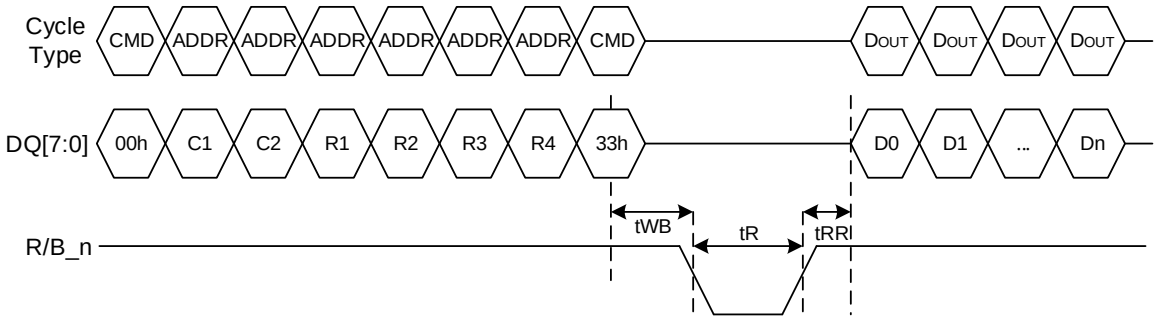


6.3.11. Erased Page Check (00h-33h)

The Erased Page Check command with 6 address cycles provides a method to ensure that a page is fully erased prior to programming data onto the page. This feature is primarily used when recovering from a power loss event, where it is possible that the page is partially programmed but data still indicates that the page is in an erased state.

The host can detect the completion of an Erased Page Check by monitoring the R/B_n output, or SR[6] of the status register. After the operation is completed, the host should check SR[0]. If SR[0] is zero, this page is erased. If SR[0] is one, this page is not erased.

Figure 71. Erased Page Check Sequence



6.4. Program Operations

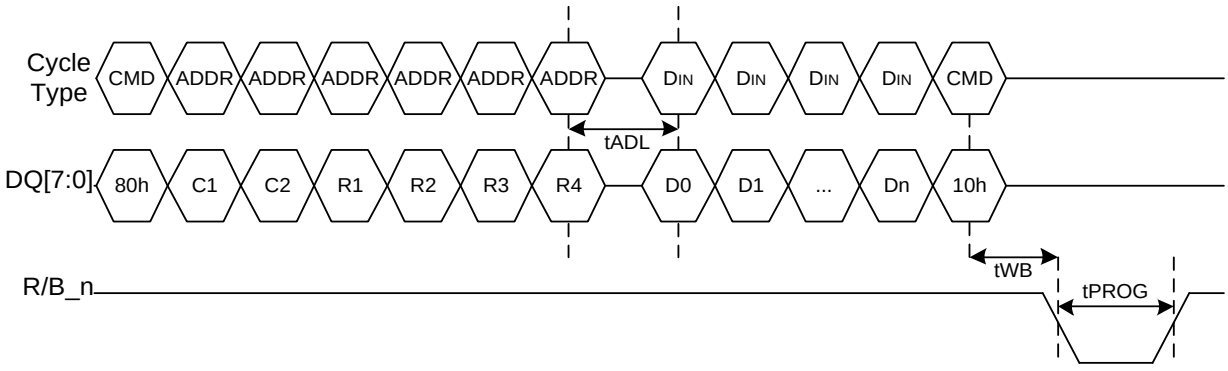
6.4.1. Page Program (80h-10h)

The Page Program command transfers a page or a portion of page data to the page buffer and then programs the data into Flash array. A page program cycle consists of a serial data loading period in which up to 16K+2048 bytes of data may be loaded into the page buffer, followed by a programming period when the loaded data is programmed into an appropriate cell. Note that users can't input more than 16K + 2048 byte of data, otherwise program operation is not guaranteed.

The serial data loading period begins by issuing the Serial Data Input command (80h), followed by the 6 cycle address cycles and then serial data. 80h clears page register for new data loading. The device supports random data input in a page. The column address of next data, which will be entered, may be changed by the Change Row Address command and Change Write Column command. Change Row Address and Change Write Column can be operated multiple times regardless of how many times it is done in a page.

After the host issues the Confirm command (10h), the programming process is initiated and completed within tPROG. Once the program process starts, the host can detect the completion of a program cycle by monitoring the RB_n output, or the SR[6] of the Status Register by Read Status command. Only the Read Status command, Read Status Enhancement command, all Reset commands (FFh, FAh and FCh) and the Suspend command are valid while programming is in progress. When the Page Program is complete, the SR[0] may be checked. The command register remains in Read Status command mode until another valid command is written to the command register.

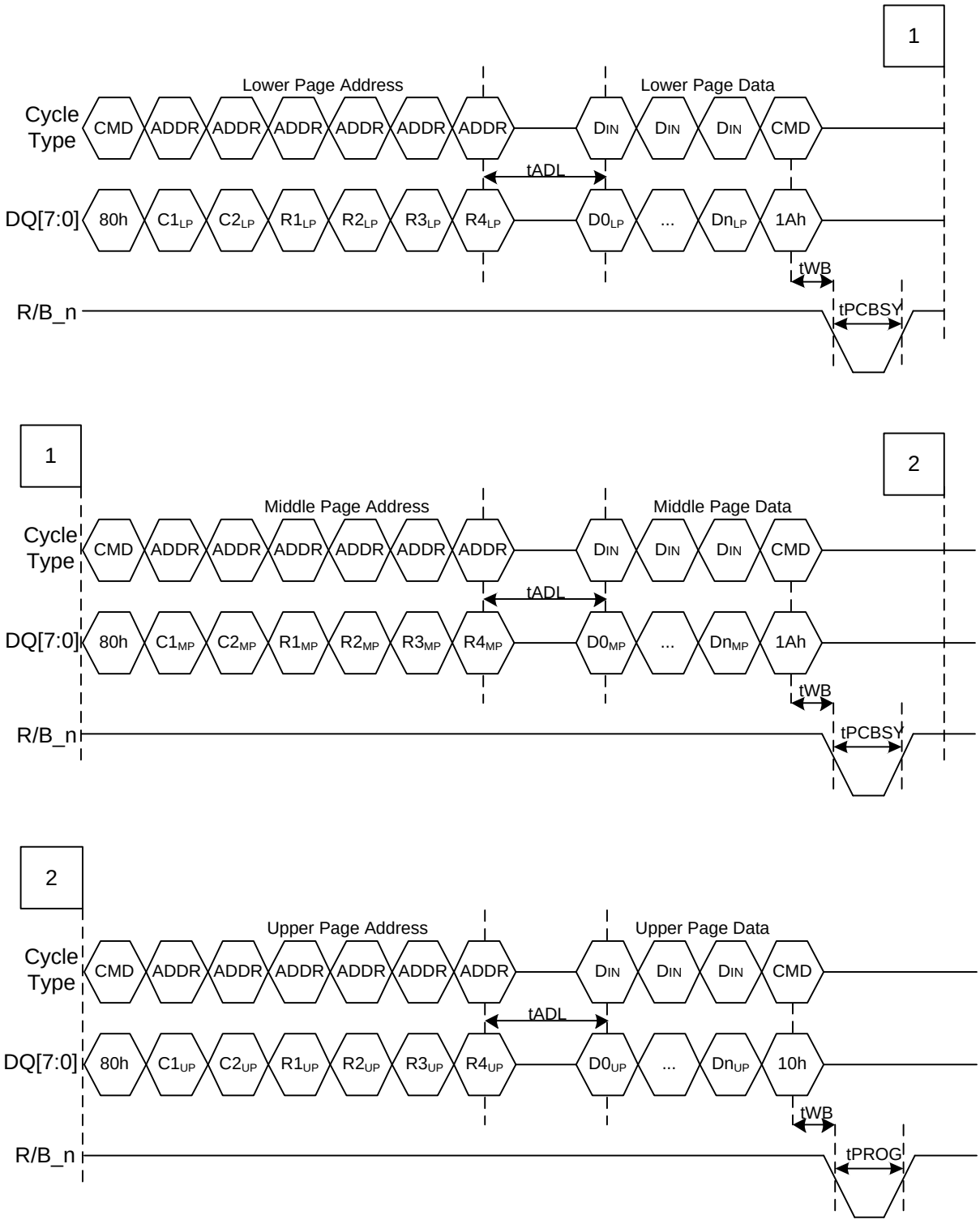
Figure 72. Page Program Sequence



This NAND Flash device supports one-pass program. Since three pages (LP/MP/UP) need programming, data latch command code 1Ah is defined. Following 80h-1Ah, one page of data will be transferred to internal data register. The host should always load the Lower page first, then Middle and Upper pages. Until all pages of data to be programmed are already transferred to internal registers, 10h is issued to begin programming to the flash array.

6.4.1.1. One-Pass Program

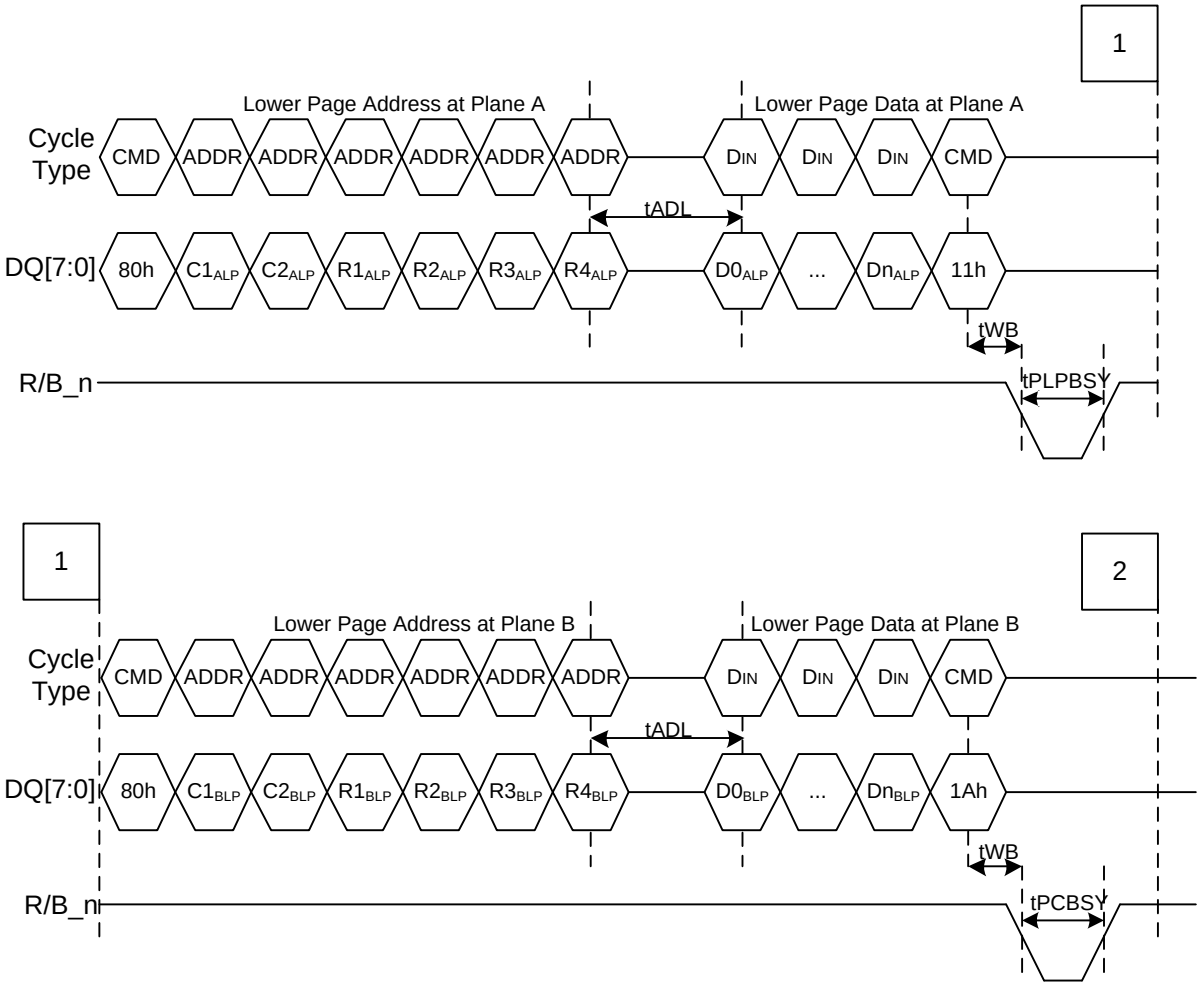
Figure 73. One-Pass Program Sequence

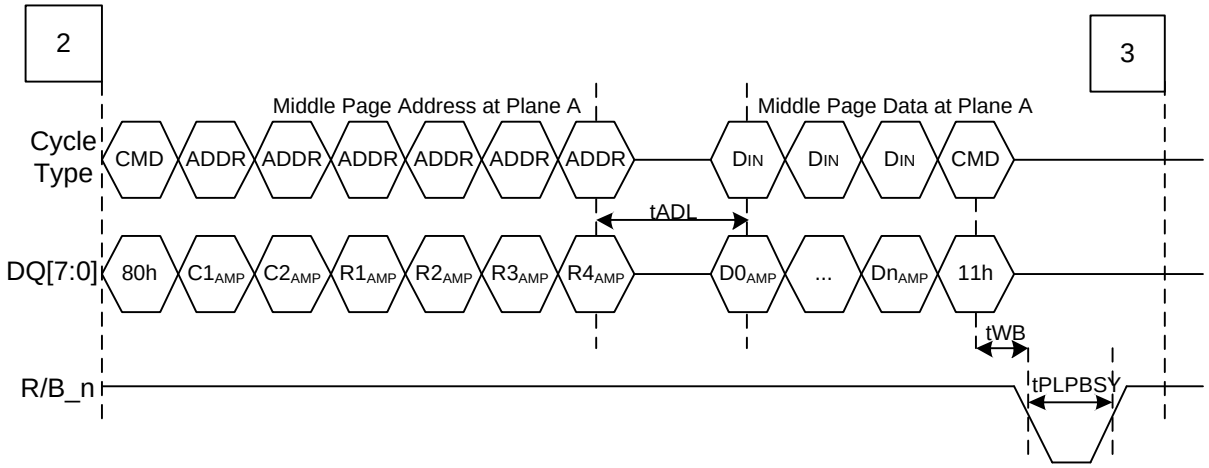


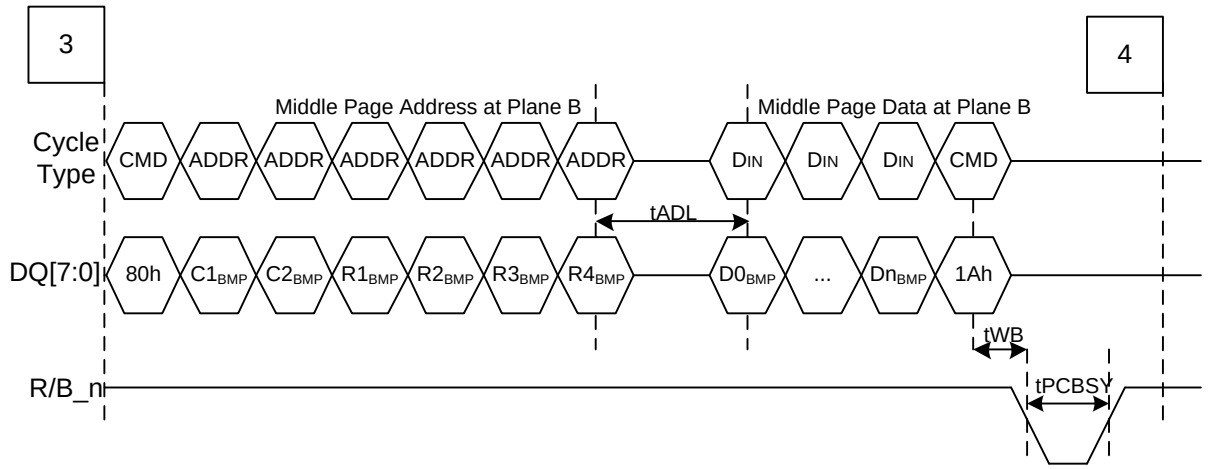
Notes: Lower, middle, and upper pages must be programmed at the same time.

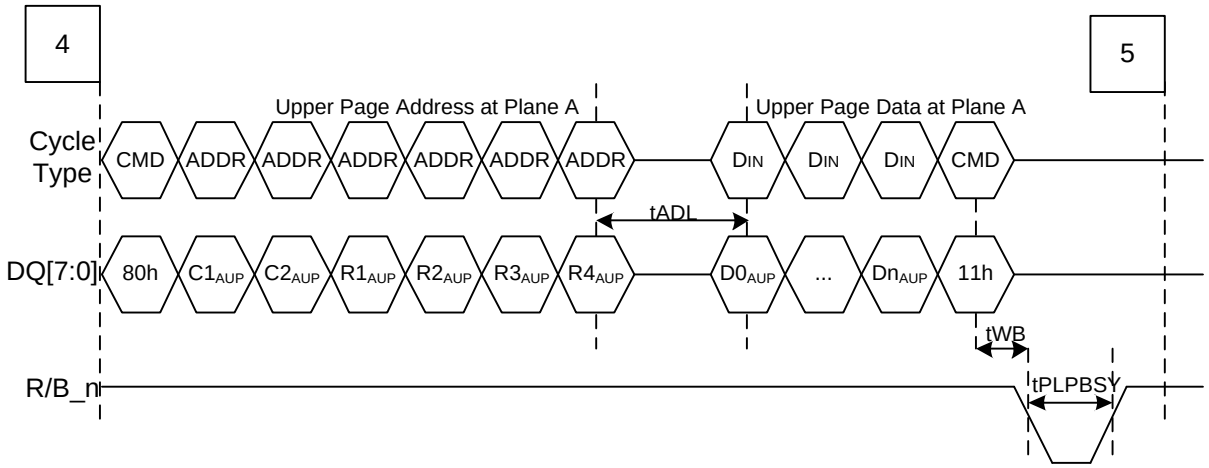
This NAND device supports multi-plane operation. The page address must be the same between two planes. Multi-Plane one-pass program sequence is shown as below.

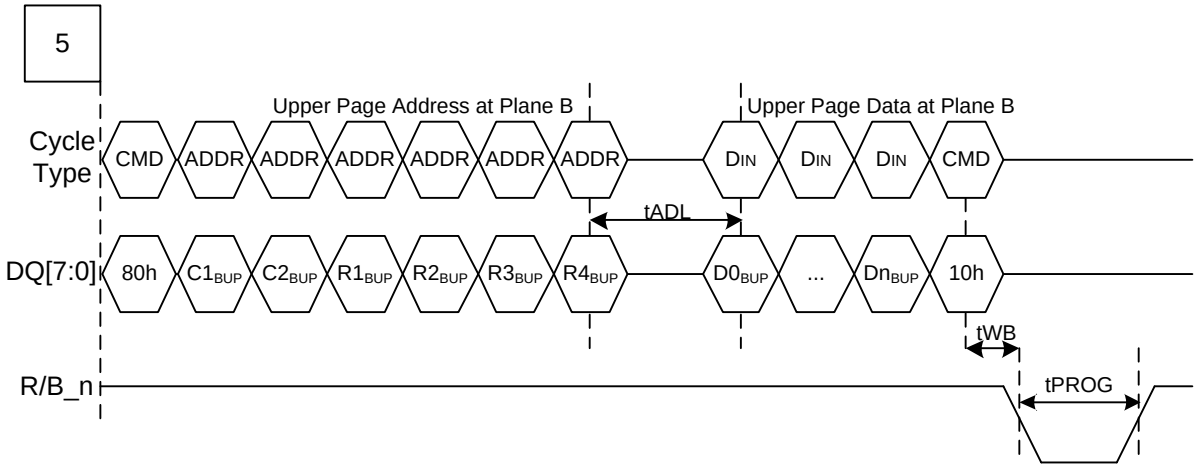
Figure 74. Multi-Plane One-Pass Program Sequence











6.4.2. Cache Program

There are two types of page buffers: Cache page buffer and Data page buffer. Cache Program is an extension of the standard page program which is executed with both data page buffer and cache page buffer. The Cache Program (80h-15h) command allows data insertion for one page while program of another page is under execution. Cache program is available only within a block.

After the serial data input command (80h) is loaded to the command register, followed by 6 cycles of address, a full page of data is latched into the cache register. Once the Cache Program command (15h) is loaded to the command register, the data in the cache page buffer is transferred into the data page buffer for cell programming. During the data transfer, device remains in busy state for a short time (tPCBSY). After all data is transferred into the data page buffer, the device returns to the ready state and allows loading the next WL/String program data into the cache page buffer through another cache program command sequence. Cell programming of the data in the data page buffer and loading of the next data into the cache page buffer is consequently processed through a pipeline model.

The Read Status commands (70h/78h) may be issued to check the status of the cache page buffer, and the pass/fail status of the cache program operation.

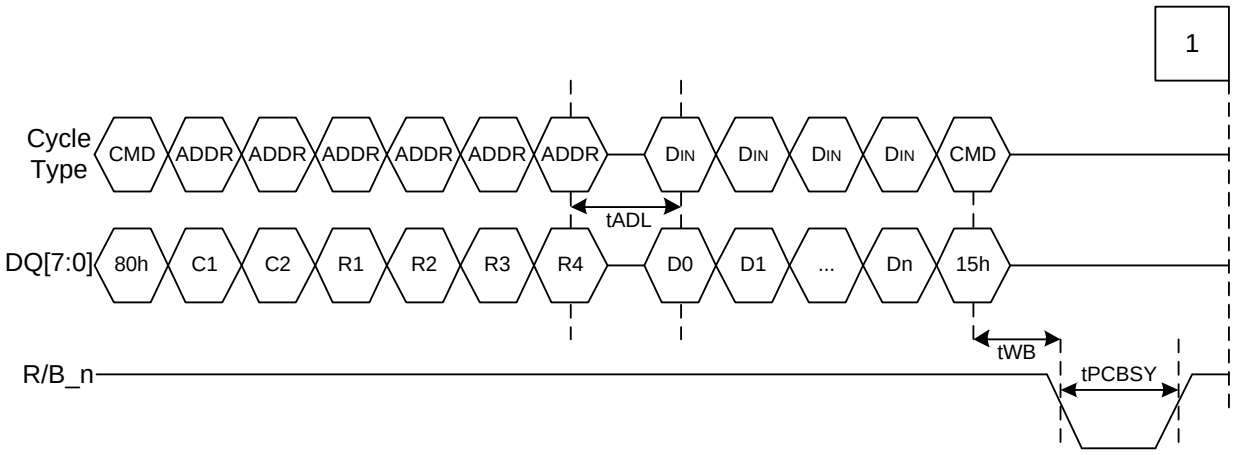
If the system monitors the progress of the operation only with R/B_n, the last page of the target program sequence must be programmed with the Page Program Confirm command (10h). Within the same set of cache program command sequences, system can't switch to block address (LUN addresses). If switching block or LUN is needed, system should close the current cache program command sets with Page Program Confirm command (10h) for the last program page within the same block or LUN, then re-start the next set of cache program command sequences on different block or LUN.

If the Cache Program command (15h) is used instead, Status bit SR[5] must be polled to find out if the last programming is finished before starting any other operation.

Status Register Check Method:

1. SR[6] indicates when the cache register is ready to accept new data.
2. SR[5] can be used to determine when the cell programming of the current data register contents is completed.
3. SR[1] can be used to identify if the previous page (page N-1) has been successfully programmed or not in cache program operation. SR[1] can be polled upon SR[6] changing to "1".
4. SR[0] is used to identify if any error has been detected by the program/erase controller while programming page N. SR[0] can be polled upon SR[5] changing to "1".
5. SR[1] may be read together with SR[0].

Figure 75. Cache Program sequence



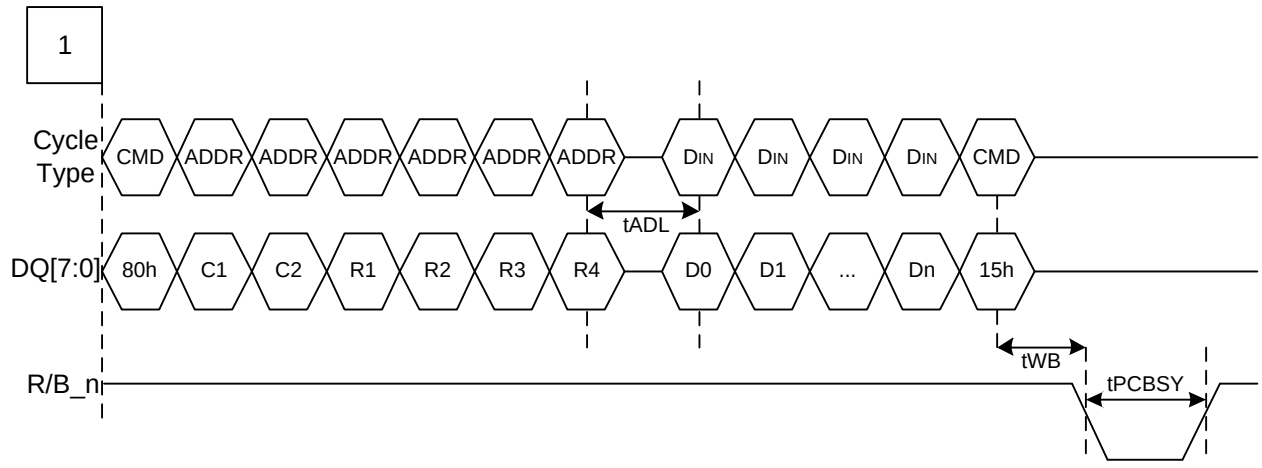
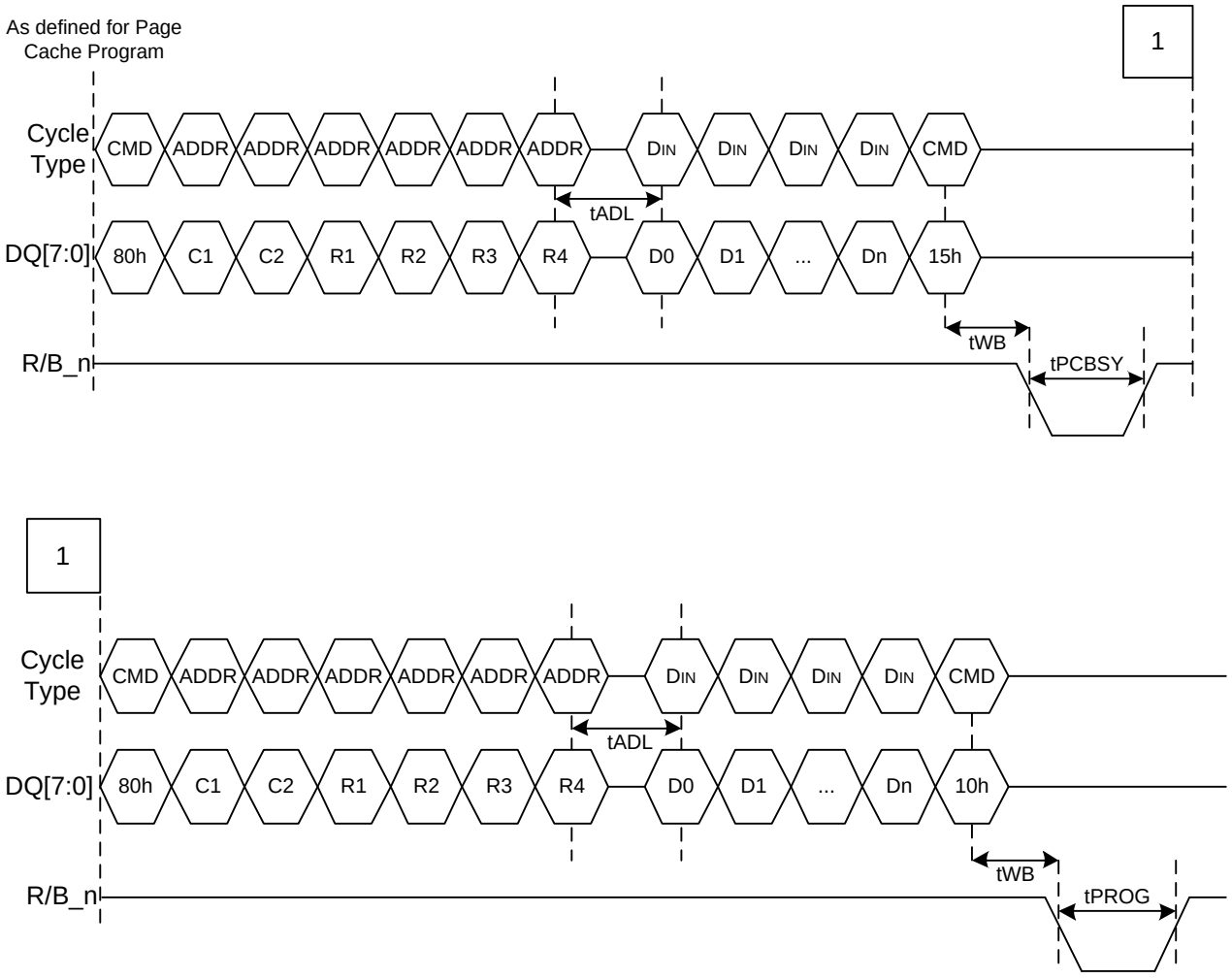


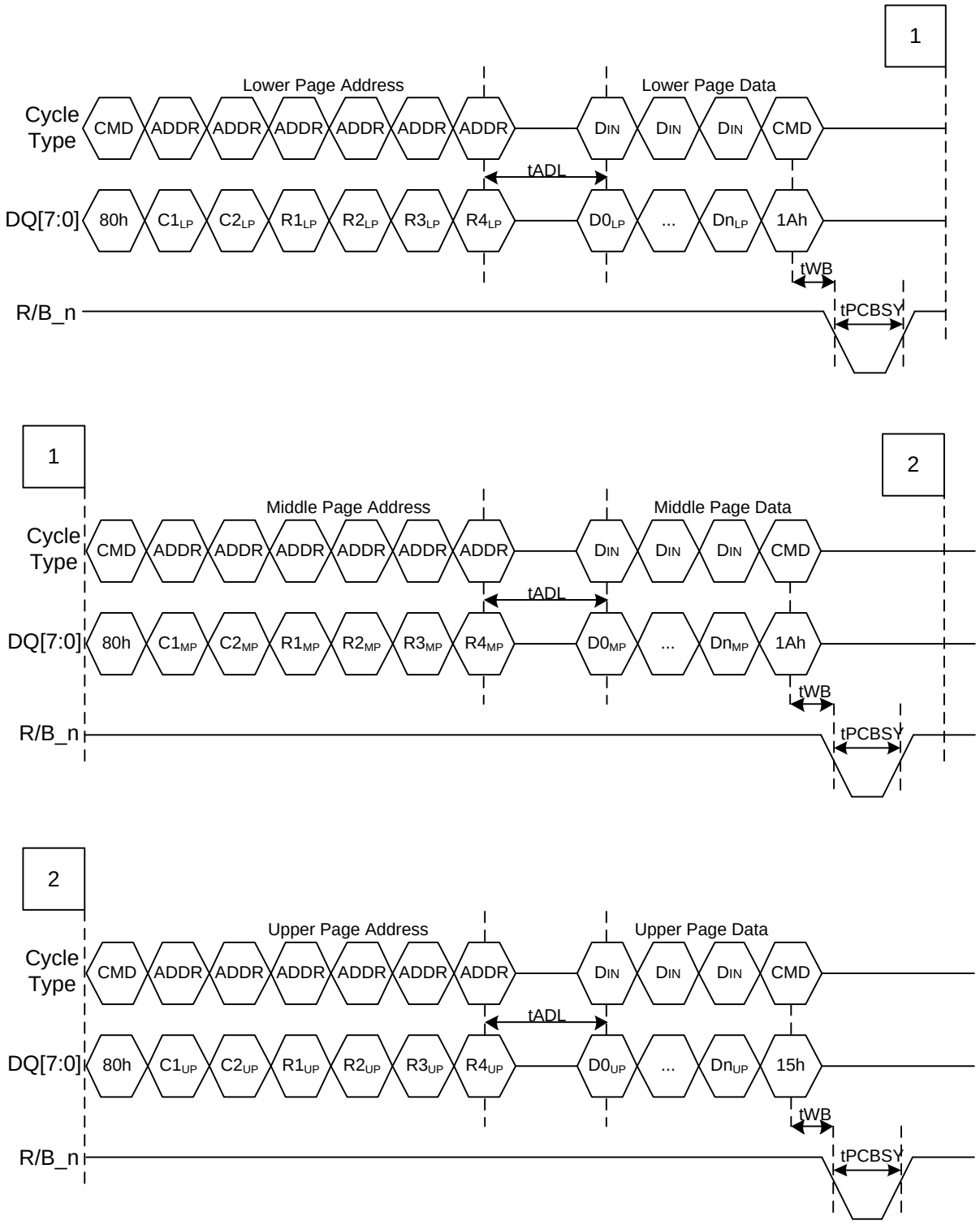
Figure 76. End Cache Program sequence



For TLC cache program, the host still needs to follow the Page Program command sequence to load Lower page first with 80h-1Ah, then load Middle page with 80h-1Ah and Upper page with 80h-15h to trigger TLC cache program.

6.4.2.1. One-Pass Cache Program

Figure 77. One-Pass Cache Program Sequence



This NAND device supports multi-plane operation. The page address must be the same between two planes. Multi-Plane One-Pass Cache Program sequence is as below.

Figure 78. Multi-Plane One-Pass Cache Program Sequence

<CMD:80h> <ADDR:Column&Row (PlaneA/LPA)> tADL <DIN:PlaneA/LPA> <CMD:11h> tWB tPLPBSY
<CMD:80h> <ADDR:Column&Row (PlaneB/LPB)> tADL <DIN:PlaneB/LPB> <CMD:1Ah> tWB tPCBSY
<CMD:80h> <ADDR: Column&Row (PlaneA/MPA)> tADL <DIN:PlaneA/MPA> <CMD:11h> tWB tPLPBSY
<CMD:80h> <ADDR: Column&Row (PlaneB/MPB)> tADL <DIN: PlaneB/MPB> <CMD:1Ah> tWB tPCBSY
<CMD:80h> <ADDR: Column&Row (PlaneA/UPA)> tADL <DIN:PlaneA/UPA> <CMD:11h> tWB tPLPBSY
<CMD:80h> <ADDR: Column&Row (PlaneB/UPB)> tADL <DIN: PlaneB/UPB> <CMD:15h> tWB tPCBSY
<CMD:80h> <ADDR:Column&Row (PlaneA/LPC)> tADL <DIN:PlaneA/LPC> <CMD:11h> tWB tPLPBSY
<CMD:80h> <ADDR:Column&Row (PlaneB/LPD)> tADL <DIN:PlaneB/LPD> <CMD:1Ah> tWB tPCBSY
<CMD:80h> <ADDR: Column&Row (PlaneA/MPC)> tADL <DIN:PlaneA/MPC> <CMD:11h> tWB tPLPBSY
<CMD:80h> <ADDR: Column&Row (PlaneB/MPD)> tADL <DIN: PlaneB/MPD> <CMD:1Ah> tWB tPCBSY
<CMD:80h> <ADDR: Column&Row (PlaneA/UPC)> tADL <DIN:PlaneA/UPC> <CMD:11h> tWB tPLPBSY
<CMD:80h> <ADDR: Column&Row (PlaneB/UPD)> tADL <DIN: PlaneB/UPD> <CMD:15h> tWB tPCBSY
……
<CMD:80h> <ADDR:Column&Row (PlaneA/last LP)> tADL <DIN:PlaneA/last LP> <CMD:11h> tWB tPLPBSY
<CMD:80h> <ADDR:Column&Row (PlaneB/last LP)> tADL <DIN:PlaneB/last LP> <CMD:1Ah> tWB tPCBSY
<CMD:80h> <ADDR: Column&Row (PlaneA/last MP)> tADL <DIN:PlaneA/last MP> <CMD:11h>tWB tPLPBSY
<CMD:80h> <ADDR: Column&Row (PlaneB/last MP)> tADL <DIN: PlaneB/last MP> <CMD:1Ah> tWB tPCBSY
<CMD:80h> <ADDR: Column&Row (PlaneA/last UP)> tADL <DIN:PlaneA/last UP> <CMD:11h> tWB tPLPBSY
<CMD:80h> <ADDR: Column&Row (PlaneB/last UP)> tADL <DIN: PlaneB/last UP> <CMD:10h> tWB tPROG

Notes:

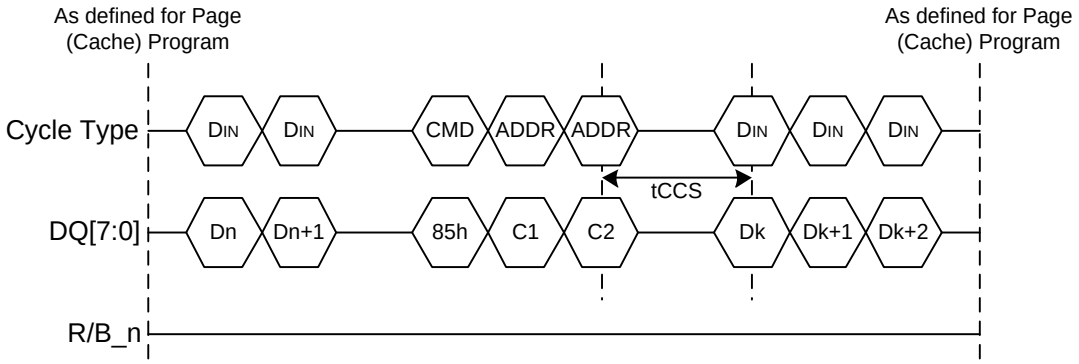
The ONFI-JEDEC Joint Taskgroup has defined the subsequent first cycles after the initial program sequence in a Multi-plane Page Program as 81h. Refer to the parameter page to determine if the device supports subsequent first cycles in a program sequence as 81h.

6.4.3. Change Write Column (85h)

The Change Write Column (85h) command changes the column address being written to in the page buffer for the selected LUN.

The host shall not write data to the LUN until tCCS ns after the last column address is written to the LUN.

Figure 79. Change Write Column Sequence



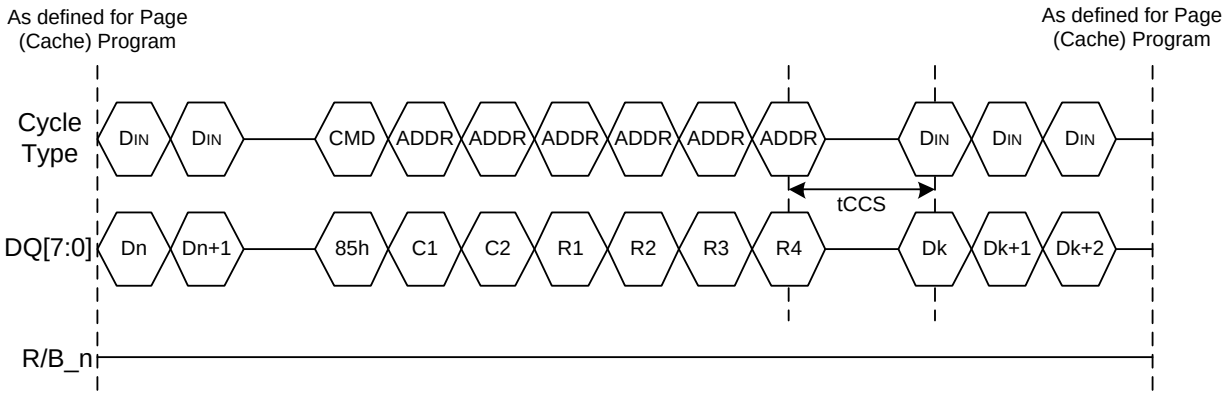
6.4.4. Change Row Address (85h)

The Change Row Address command changes the row and column address being written to for the selected LUN. This mechanism may be used to adjust the block address, page address, and column address for a Program that is in execution. The LUN and plane address shall be the same as the Program that is in execution and the previous input data Dn, Dn+1 will be written to the new page and block in the same Plane.

The host shall not write data to the LUN until tCCS ns after the last row address is written to the LUN.

For TLC program, the page data input order should always input Lower page data followed by Middle page data and input the Upper page data the last. In case of inputting data out of Lower, Middle, Upper page order, it may cause data lost for the out of order pages.

Figure 80. Change Row Address Sequence



6.4.4.1. TLC Program Suspend

This device supports only TLC program suspend, but does not support SLC program suspend.

The TLC Program Suspend (87h) command is used to interrupt a program operation for a specified LUN with 6 address cycles; the block, plane, page and column address are ignored. The command can be issued at any time during a program operation. The command is ignored if the device is already in suspending mode or the device is not busy in program progress.

Once the command is issued, it is necessary to issue Read Status (70h) command and polling SR[6] to find out when the program controller has paused. Once SR[6] turns from zero to one, then the host should check SR[2]. If SR[2] is one, it means that the program operation is successfully suspended. If SR[2] is zero, it means that the program operation is already complete and LUN is not suspended. The suspend latency is defined by tPSPD. If any error happens, SR[0] is set to one.

When the specified LUN is in program suspend mode, for the operations on the same LUN, only the following commands are allowed:

Reset Commands (FFh, FAh, FCh) would cancel the suspended program operation and reset the Status Bits to 'b0. Programmed data is not guaranteed.

Page read operation and Multi-Plane read operation on different blocks on the same LUN is allowed. Host should toggle out the data before issue the Program resume command to prevent data lost from the read result. If reading from the same page in program suspend, the output data is undetermined (internal implementation is that this read equals to bad block read).

All the Status Read commands, ZQ calibration, Set Feature and Get Feature commands are allowed. During Program Suspend, the program pass/fail status is not valid.

Mode switching is allowed during Program Suspend.

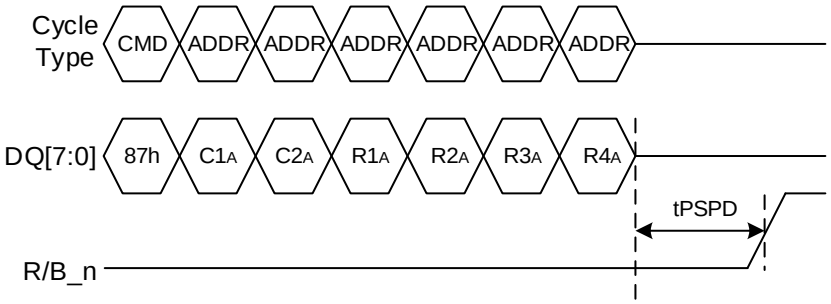
If the Multi-Plane program operation is ongoing, Program Suspend commands will suspend both planes at the same time.

The total program time will be affected by program suspend operation. The host should take tPSPD and tRESUME time into the consideration for total tPROG.

Due to limited number of the page buffers, Program suspend is not supported in cache program mode and page buffer fast release mode.

During program suspend, it is forbidden to use Set Features/LUN Set Features to change settings.

Figure 81. Program Suspend Sequence

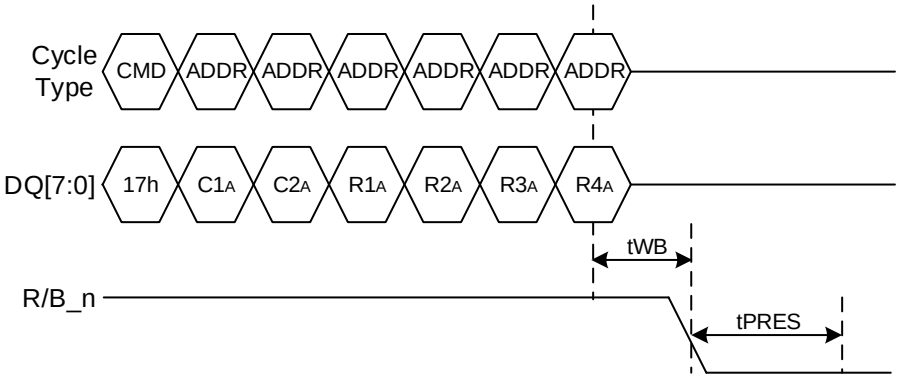


6.4.5. Program Resume

To resume a suspended program operation for a specified LUN, issue Program Resume (17h) command with 6 address cycles; the block, plane, page and column address are ignored. The command is ignored if the device is not in suspending mode. The resume latency is defined by tPRES, to improve the effectiveness of program operation and avoid infinite program time. Host is allowed to issue the next Program Suspend command if polling SR[2] to return '0' by issuing Read Status (70h) command.

If the previous suspended operation is Multi-Plane program operation, both planes will be resumed at the same time.

Figure 82. TLC Program Resume Sequence



6.5. Copyback Operations

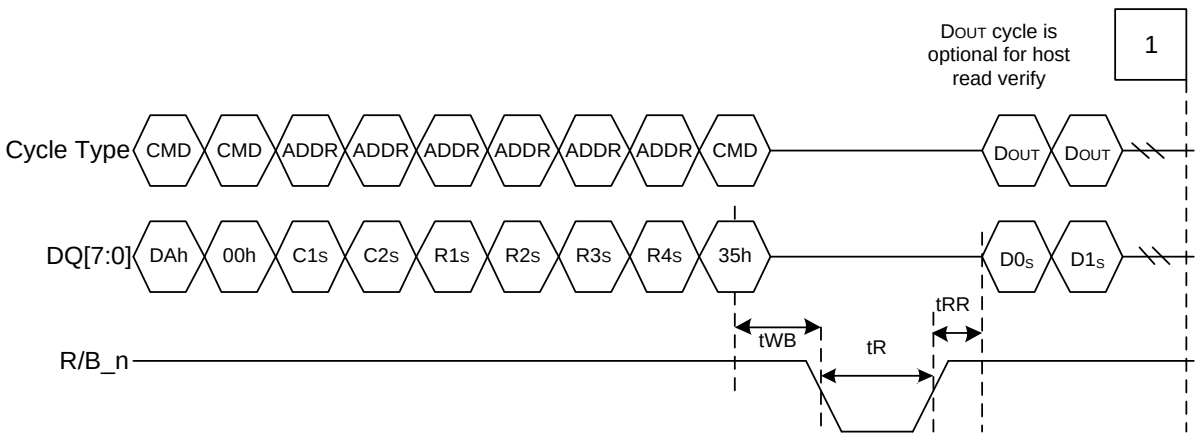
6.5.1. Copyback Read (00h-35h)/Copyback Program (85h-10h)

The Copyback command is used to quickly and efficiently copy data stored in one page to another page on the same plane, same LUN without utilizing an external memory. The data read from the source location may be read by the host using the Change Read Column (05h-E0h) command as needed. After completing any data read out, the host may perform data modification using the Change Write Column (85h) command as needed.

00h-35h command code performs a read operation which moves the whole 16K+2048 byte data from the address of the source page into the internal data buffer. As soon as the device returns to ready state, optional data read-out is allowed by toggling RE_n. Then data input cycle for modifying a portion or multiple distant portions of the source page is allowed by issuing 85h command code. The Page Program Confirm command code (10h) is required to actually begin the programming operation. Serial Data Input command (80h) would reset the data buffer value to all FFh, system should not use Serial Data Input command (80h) for Copyback function.

For Copyback TLC program, the page data copy order should always input Lower page data followed by Middle page data and input the Upper page data the last. In case of inputting data out of Lower, Middle, Upper page order, it may cause data lost for the out of order pages.

Figure 83. Copyback Sequence (SLC to SLC)



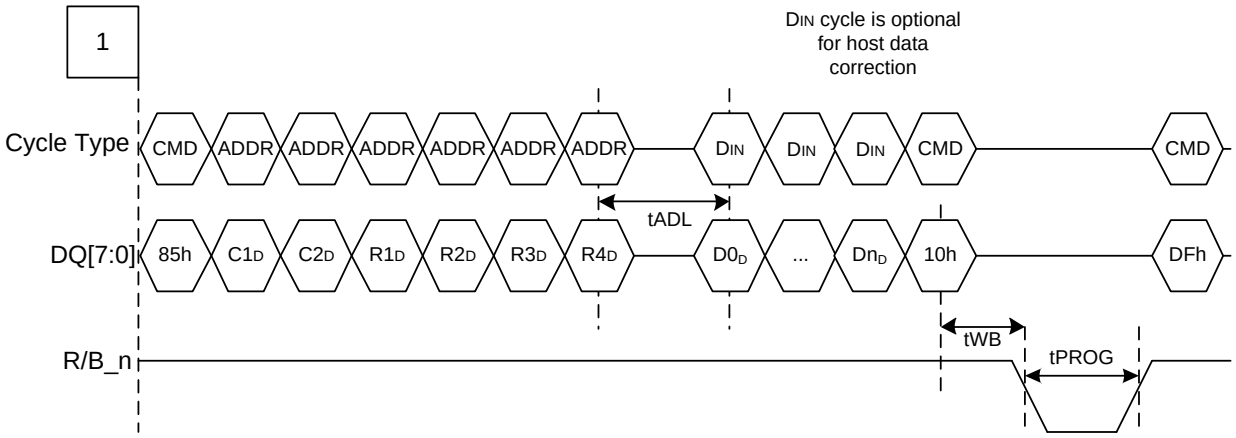
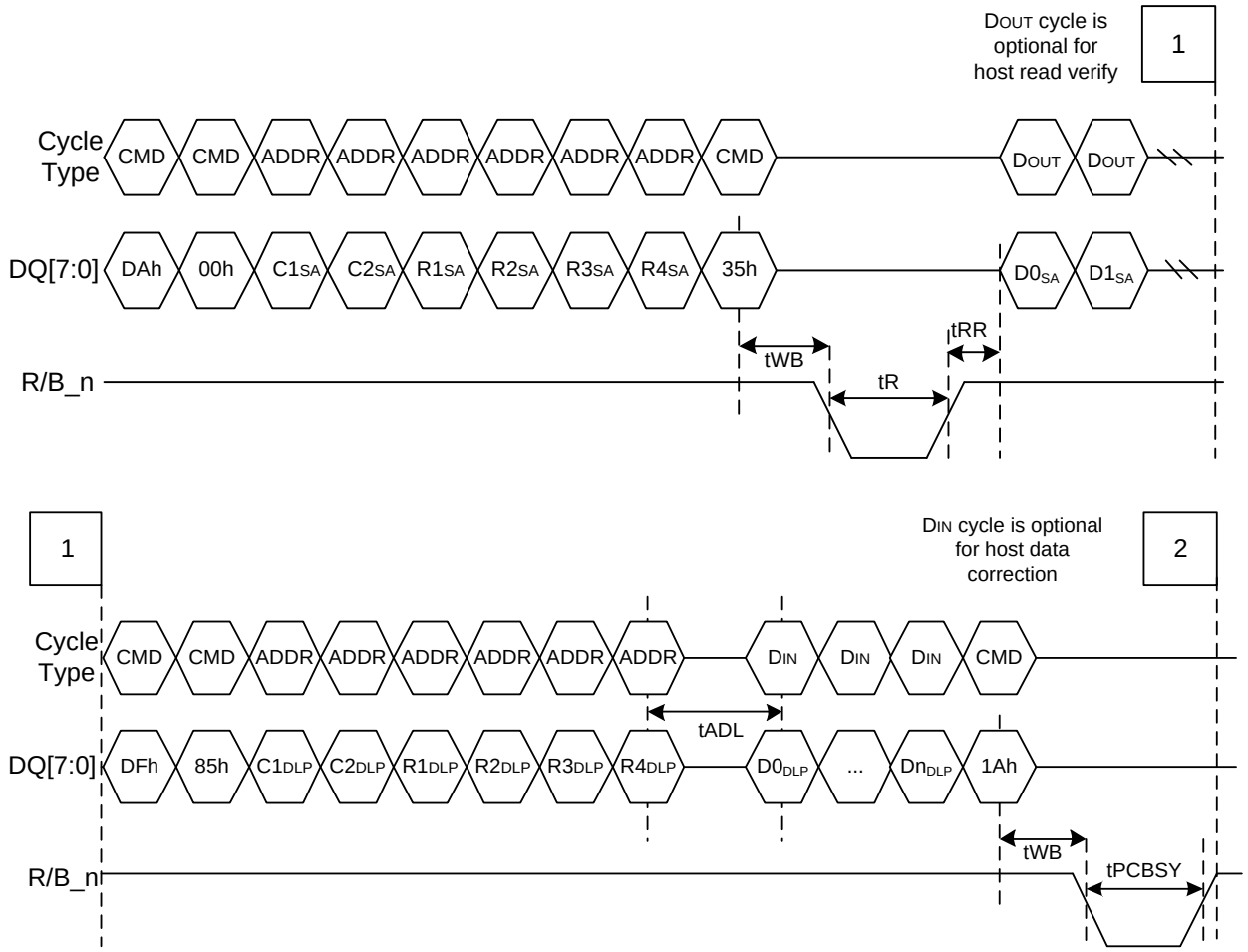
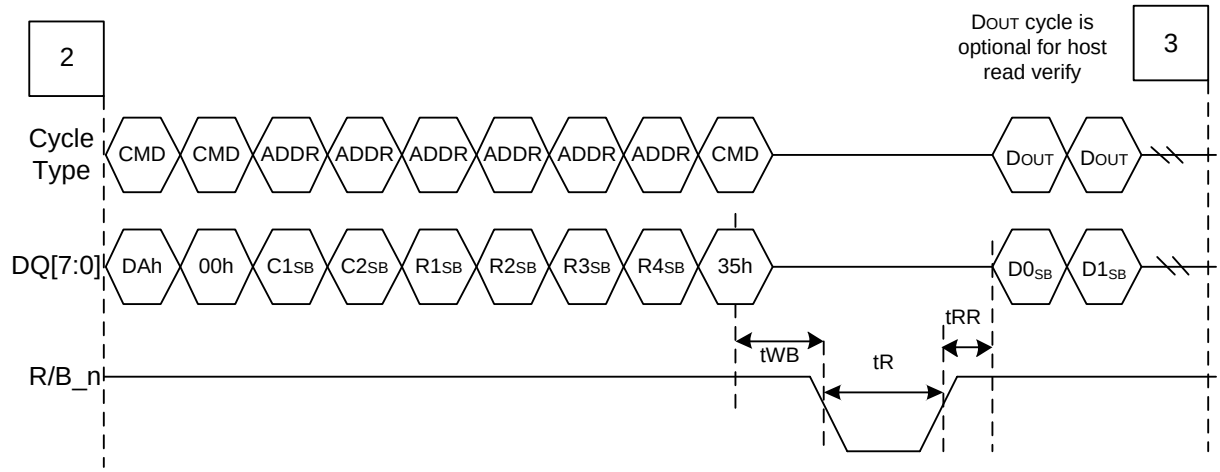
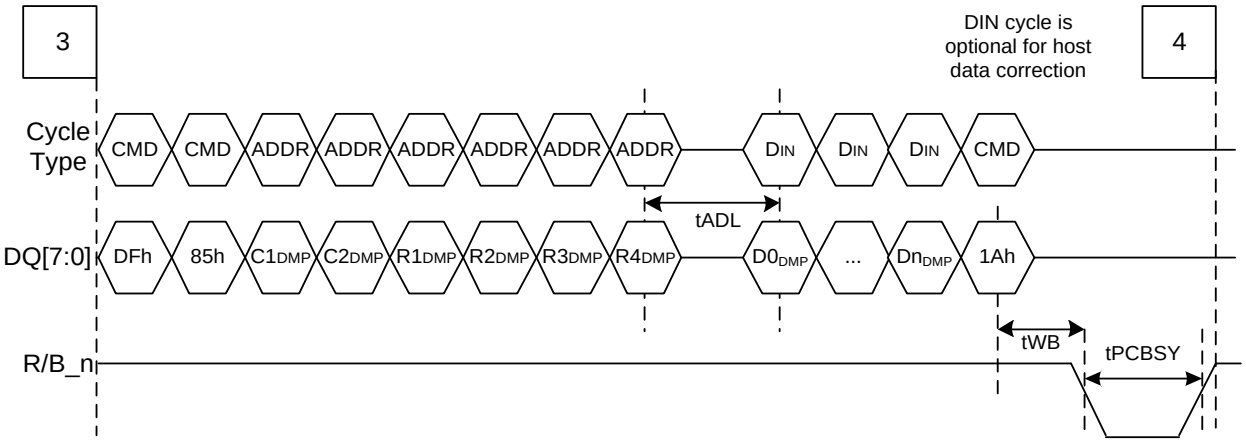
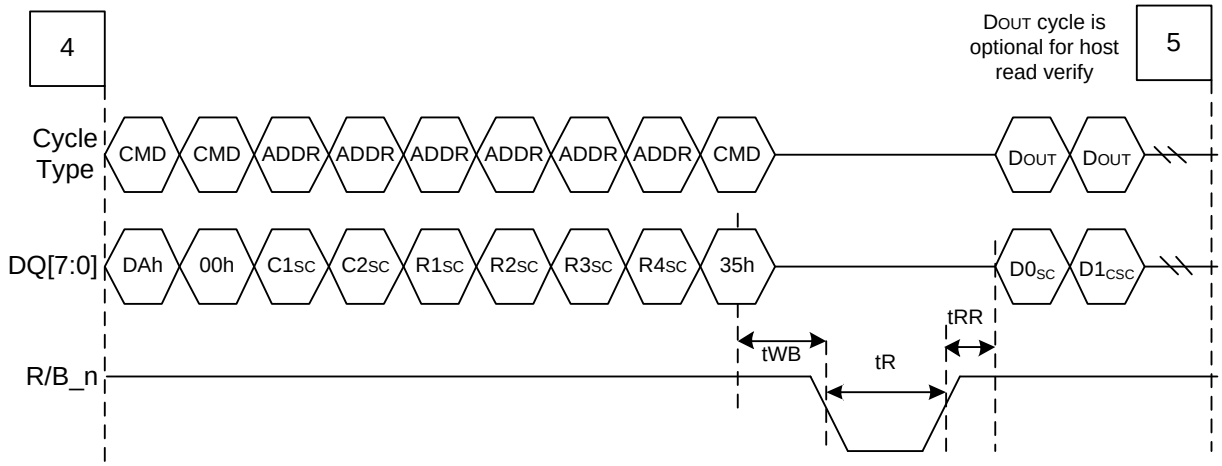


Figure 84. Copyback Sequence (SLC to TLC)









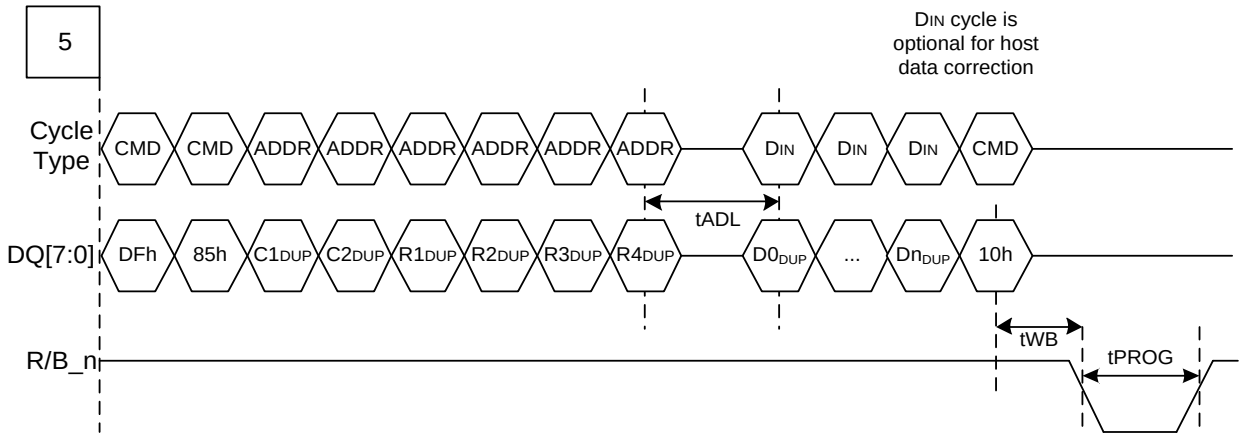
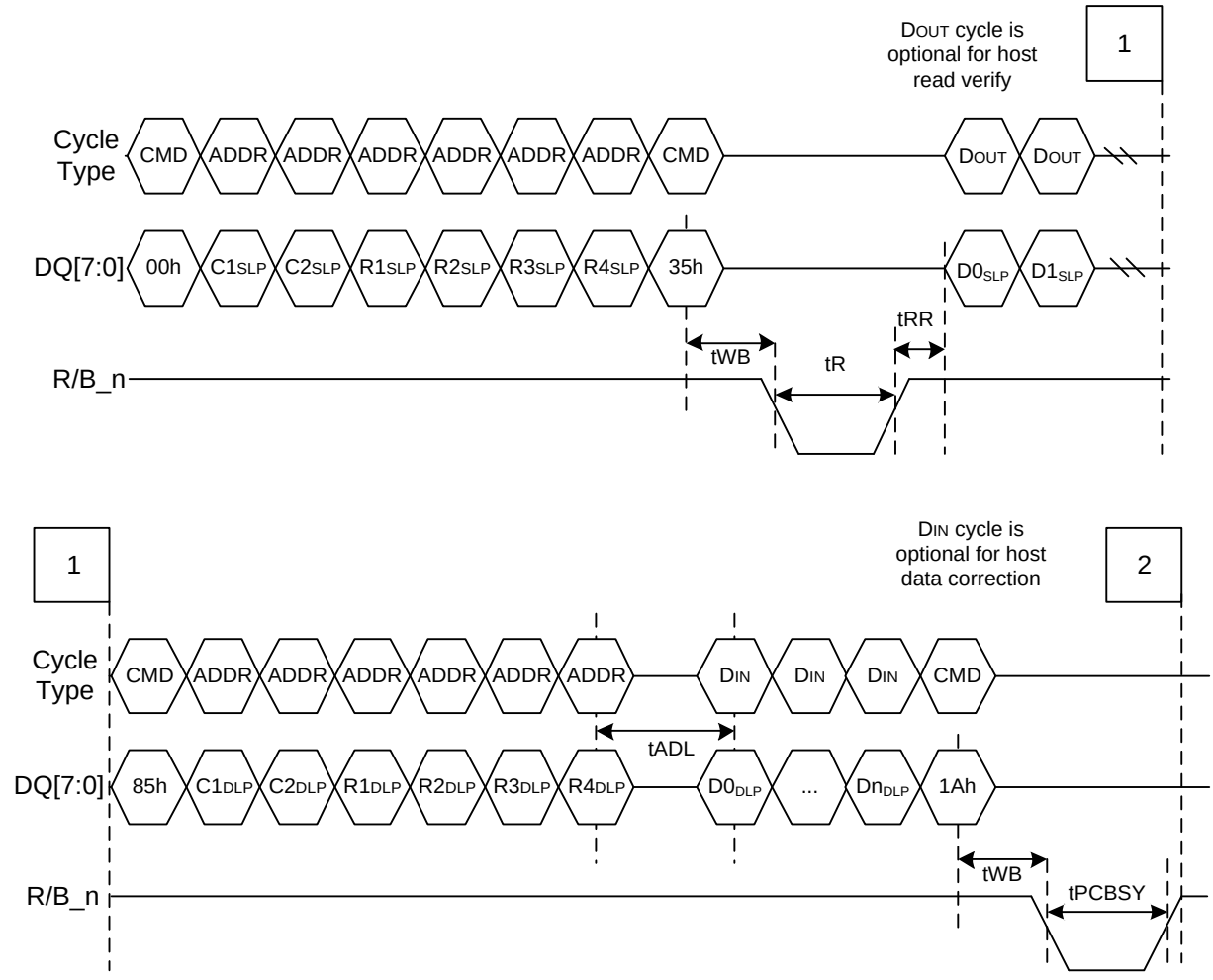
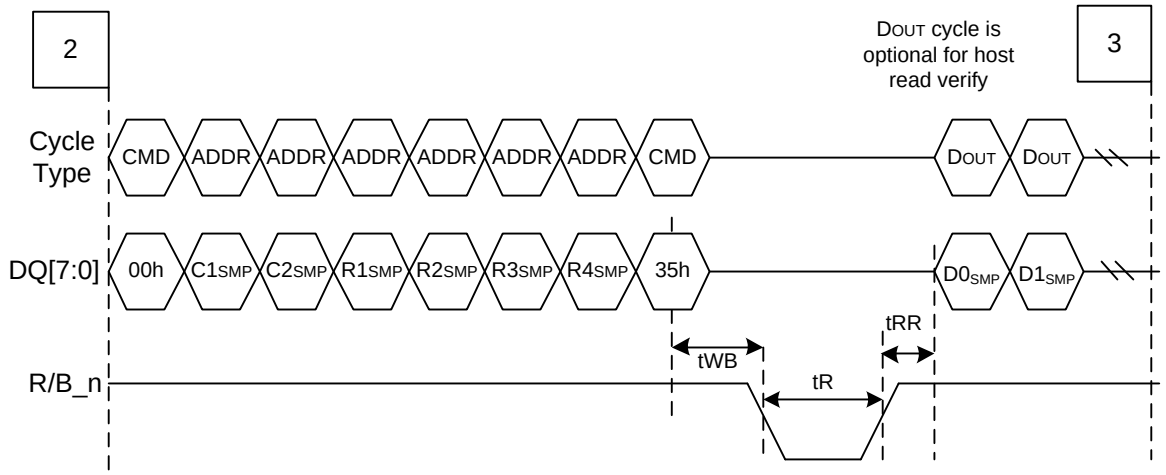
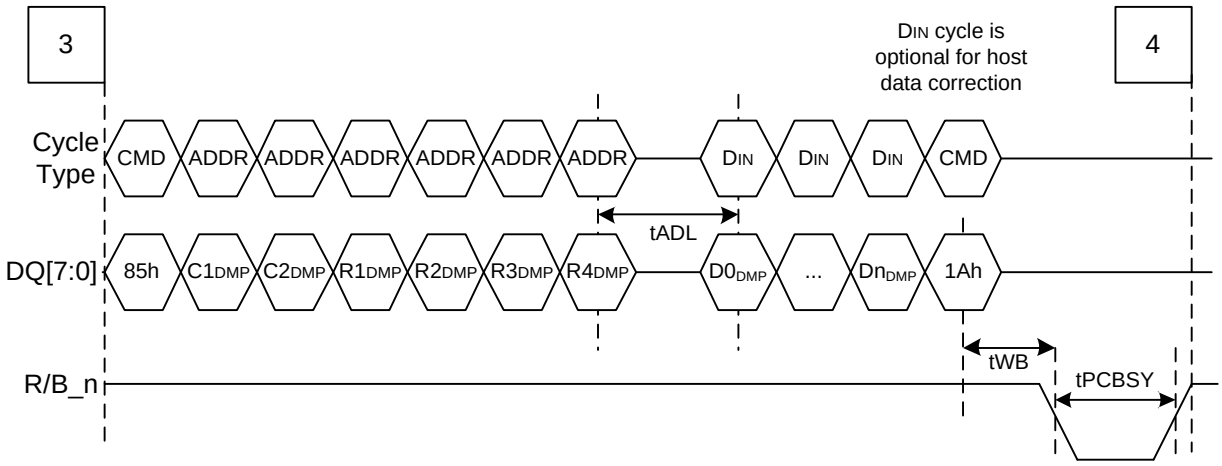
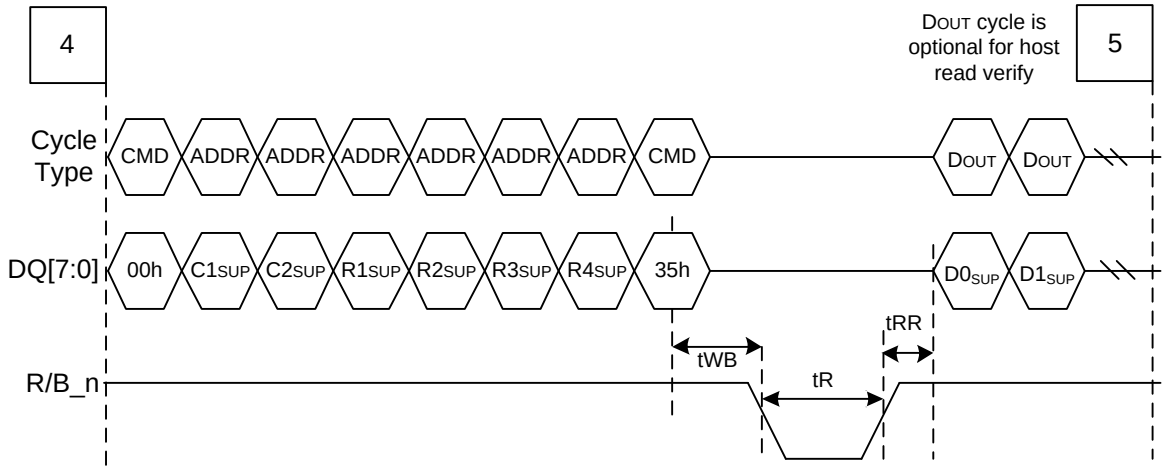


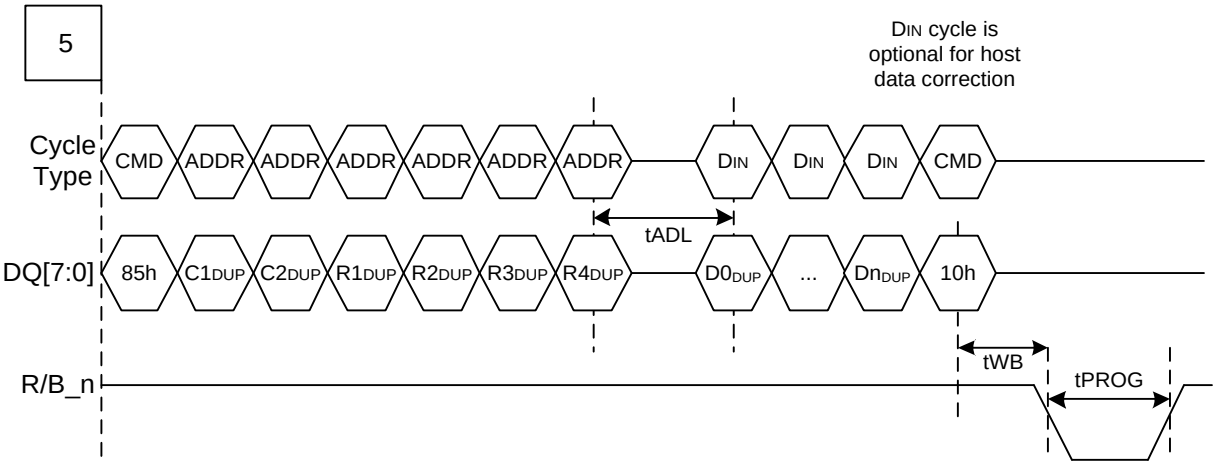
Figure 85. Copyback Sequence (TLC to TLC)





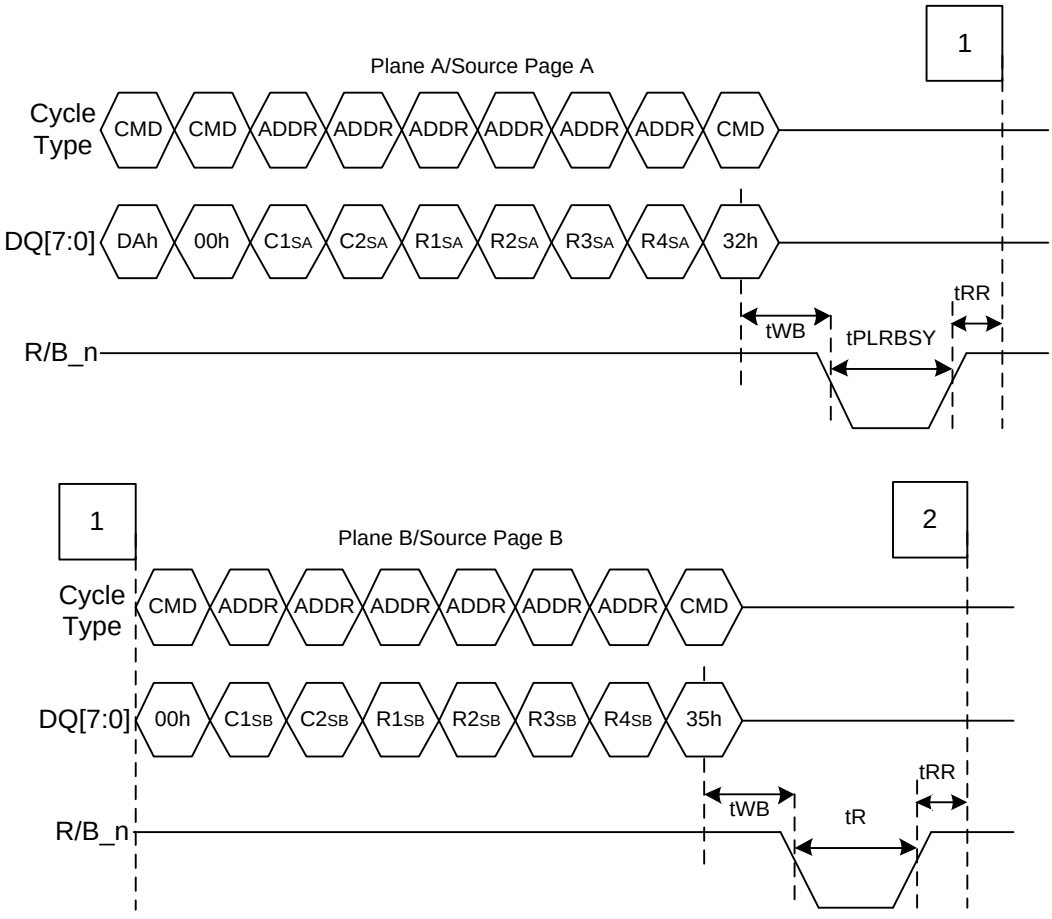


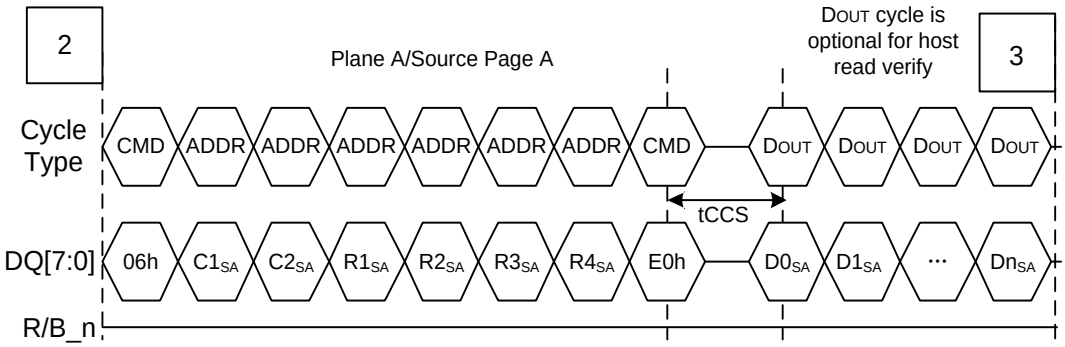


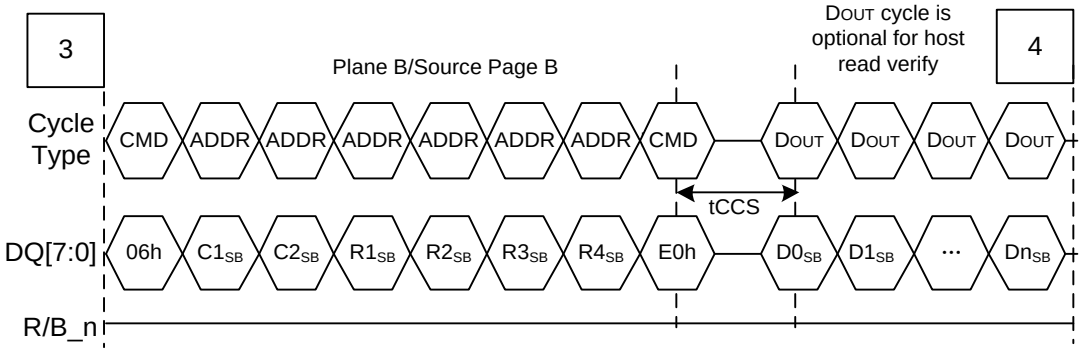


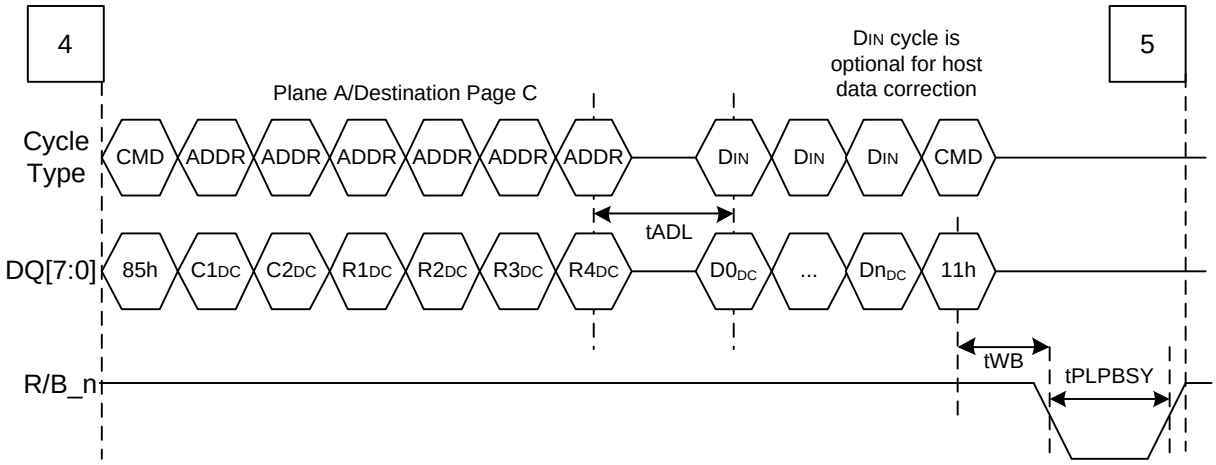
This NAND device supports multi-plane operation. The page address must be the same between two planes. Multi-Plane Copyback sequence is shown as below.

Figure 86. Multi-Plane Copyback Sequence (SLC to SLC)









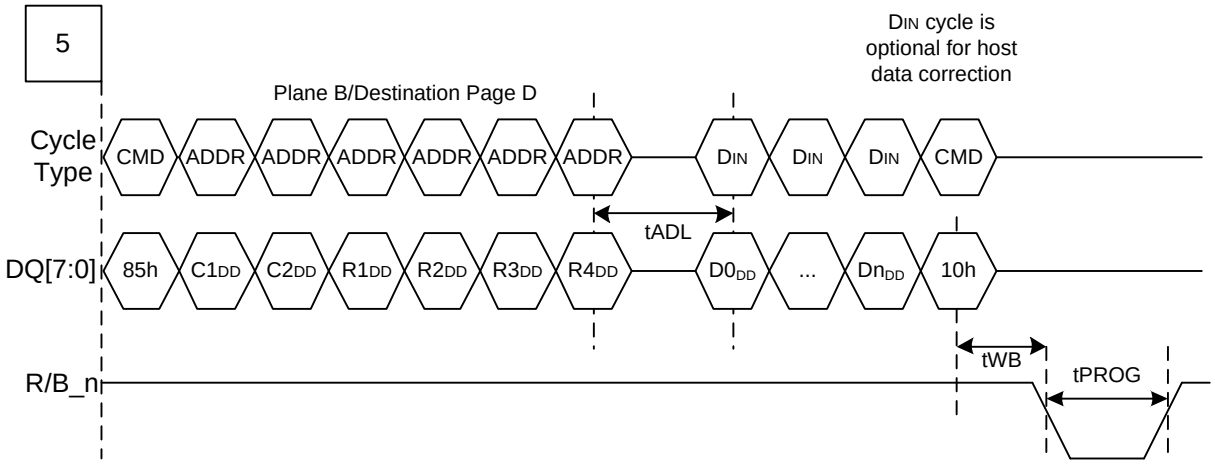


Figure 87. Multi-Plane Copyback Sequence (SLC to TLC)

<CMD:DAh>

<CMD:00h> <ADDR:Column&Row (PlaneA/source pageA)> <CMD:32h> tWB tPLRBSY

<CMD:00h> <ADDR:Column&Row (PlaneB/source pageB)> <CMD:35h> tWB tR

<CMD:06h> <ADD:Column&Row(PlaneA/pageA/columnN)> <CMD:E0h> tCCS

<DOUT:Dn(PlaneA/pageA)> <DOUT:Dn+1(PlaneA/pageA)>… (optional for host read verify)

<CMD:06h> <ADD:Column&Row(PlaneB/pageB/columnN)> <CMD:E0h> tCCS

<DOUT:Dn(PlaneB/pageB)> <DOUT:Dn+1(PlaneB/pageB>… (optional for host read verify)

<CMD:DFh>

<CMD:85h> <ADDR:Column&Row (PlaneA/destination LP)> tADL <DIN:modified data> <CMD:11h> tWB tPLPBSY (optional for modified data if error found in previous read verify)

<CMD:85h> <ADDR:Column&Row (PlaneB/destination LP)> tADL <DIN:modified data> <CMD:1Ah> tWB tPCBSY (optional for modified data if error found in previous read verify)

<CMD:DAh>

<CMD:00h> <ADDR:Column&Row (PlaneA/source pageC)> <CMD:32h> tWB tPLRBSY

<CMD:00h> <ADDR:Column&Row (PlaneB/source pageD)> <CMD:35h> tWB tR

<CMD:06h> <ADD:Column&Row(PlaneA/pageA/columnN)> <CMD:E0h> tCCS

<DOUT:Dn(PlaneA/pageA)> <DOUT:Dn+1(PlaneA/pageC)>… (optional for host read verify)

<CMD:06h> <ADD:Column&Row(PlaneB/pageD/columnN)> <CMD:E0h> tCCS

<DOUT:Dn(PlaneB/pageD)> <DOUT:Dn+1(PlaneB/pageD>… (optional for host read verify)

<CMD:DFh>

<CMD:85h> <ADDR:Column&Row (PlaneA/destination MP)> tADL <DIN:modified data> <CMD:11h> tWB tPLPBSY (optional for modified data if error found in previous read verify)

<CMD:85h> <ADDR:Column&Row (PlaneB/destination MP)> tADL <DIN:modified data> <CMD:1Ah> tWB tPCBSY (optional for modified data if error found in previous read verify)

<CMD:DAh>

<CMD:00h> <ADDR:Column&Row (PlaneA/source pageE)> <CMD:32h> tWB tPLRBSY

<CMD:00h> <ADDR:Column&Row (PlaneB/source pageF)> <CMD:35h> tWB tR

<CMD:06h> <ADD:Column&Row(PlaneA/pageE/columnN)> <CMD:E0h> tCCS
<DOUT:Dn(PlaneA/pageE)> <DOUT:Dn+1(PlaneA/pageE)>… (optional for host read verify)
<CMD:06h> <ADD:Column&Row(PlaneB/pageB/columnN)> <CMD:E0h> tCCS
<DOUT:Dn(PlaneB/pageF)> <DOUT:Dn+1(PlaneB/pageF>… (optional for host read verify)
<CMD:DFh>
<CMD:85h> <ADDR:Column&Row (PlaneA/destination UP)> tADL <DIN:modified data> <CMD:11h> tWB tPLPBSY (optional for modified data if error found in previous read verify)
<CMD:85h> <ADDR:Column&Row (PlaneB/destination UP)> tADL <DIN:modified data> <CMD:10h> tWB tPROG(optional for modified data if error found in previous read verify)

Notes:

The ONFI-JEDEC Joint Taskgroup has defined the subsequent first cycles after the initial program sequence in a Multi-plane Page Program as 81h. Refer to the parameter page to determine if the device supports subsequent first cycles in a program sequence as 81h.

Figure 88. Multi-Plane Copyback Sequence (TLC to TLC)

<CMD:00h> <ADDR:Column&Row (PlaneA/source LP)> <CMD:32h> tWB tPLRBSY
<CMD:00h> <ADDR:Column&Row (PlaneB/source LP)> <CMD:35h> tWB tR
<CMD:06h> <ADDR:Row(PlaneA/source LP)> <CMD:E0h> tCCS <DOUT:D0> <DOUT:D1>… (optional for host read verify)
<CMD:06h> <ADDR:Row(PlaneB/source LP)> <CMD:E0h> tCCS <DOUT:D0> <DOUT:D1>… (optional for host read verify)
<CMD:85h> <ADDR:Column&Row (PlaneA/destination LP)> tADL <DIN:modified data> <CMD:11h> tWB tPLPBSY (optional for correction data if error found in previous read verify)
<CMD:85h> <ADDR:Column&Row (PlaneB/destination LP)> tADL <DIN:modified data> <CMD:1Ah> tWB tPCBSY (optional for correction data if error found in previous read verify)
<CMD:00h> <ADDR:Column&Row (PlaneA/source MP)> <CMD:32h> tWB tPLRBSY
<CMD:00h> <ADDR:Column&Row (PlaneB/source MP)> <CMD:35h> tWB tR
<CMD:06h> <ADDR:Row(PlaneA/source MP)> <CMD:E0h> tCCS <DOUT:D0> <DOUT:D1>… (optional for host read verify)
<CMD:06h> <ADDR:Row(PlaneB/source MP)> <CMD:E0h> tCCS <DOUT:D0> <DOUT:D1>… (optional for host read verify)
<CMD:85h> <ADDR:Column&Row (PlaneA/destination MP)> tADL <DIN:modified data> <CMD:11h> tWB tPLPBSY (optional for correction data if error found in previous read verify)
<CMD:85h> <ADDR:Column&Row (PlaneB/destination MP)> tADL <DIN:modified data> <CMD:1Ah> tWB tPCBSY (optional for correction data if error found in previous read verify)
<CMD:00h> <ADDR:Column&Row (PlaneA/source UP)> <CMD:32h> tWB tPLRBSY
<CMD:00h> <ADDR:Column&Row (PlaneB/source UP)> <CMD:35h> tWB tR
<CMD:06h> <ADDR:Row(PlaneA/source UP)> <CMD:E0h> tCCS <DOUT:D0> <DOUT:D1>… (optional for host read verify)
<CMD:06h> <ADDR:Row(PlaneB/source UP)> <CMD:E0h> tCCS <DOUT:D0> <DOUT:D1>… (optional for host read verify)

<CMD:85h> <ADDR:Column&Row (PlaneA/destination UP)> tADL <DIN:modified data> <CMD:11h> tWB tPLPBSY (optional for correction data if error found in previous read verify)

<CMD:85h> <ADDR:Column&Row (PlaneB/destination UP)> tADL <DIN:modified data> <CMD:10h> tWB tPROG (optional for correction data if error found in previous read verify)

Notes:

The ONFI-JEDEC Joint Taskgroup has defined the subsequent first cycles after the initial program sequence in a Multi-plane Page Program as 81h. Refer to the parameter page to determine if the device supports subsequent first cycles in a program sequence as 81h.

6.6. Erase Operations

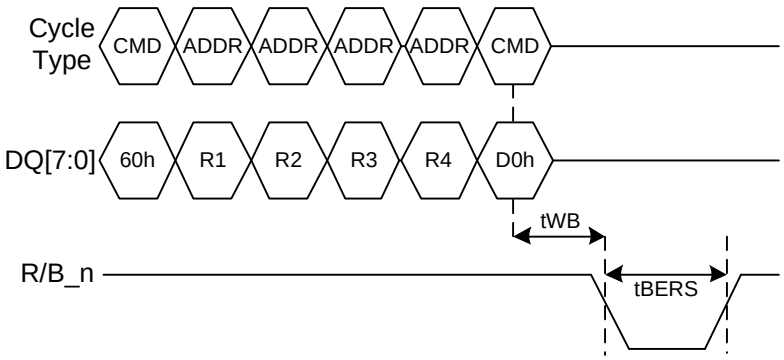
6.6.1. Block Erase (60h-D0h)

The Block Erase command is used to erase a single block. Block address loading is accomplished in 4 cycles initiated by an Erase Setup command (60h). Only block addresses are valid while page addresses are ignored. The Erase Confirm command (D0h) following the block address loading begins the internal erasing process. This two-step sequence of setup followed by execution command prevents memory contents from being accidentally erased due to external noise conditions.

Once the erase process starts, the Read Status commands (70h/78h) may be issued to read the status register. The host can detect the completion of an erase by monitoring the RB_n output, or SR[6] of the status register. Only the Read Status command, all Reset commands and Suspend command are valid while erasing is in progress. When the erase operation is completed, SR[0] may be checked. A Block Erase operation shall be considered successful if SR[0] returns zero after completion of the Block Erase operation. SR[0] is valid for this command after SR[6] transitions from zero to one.

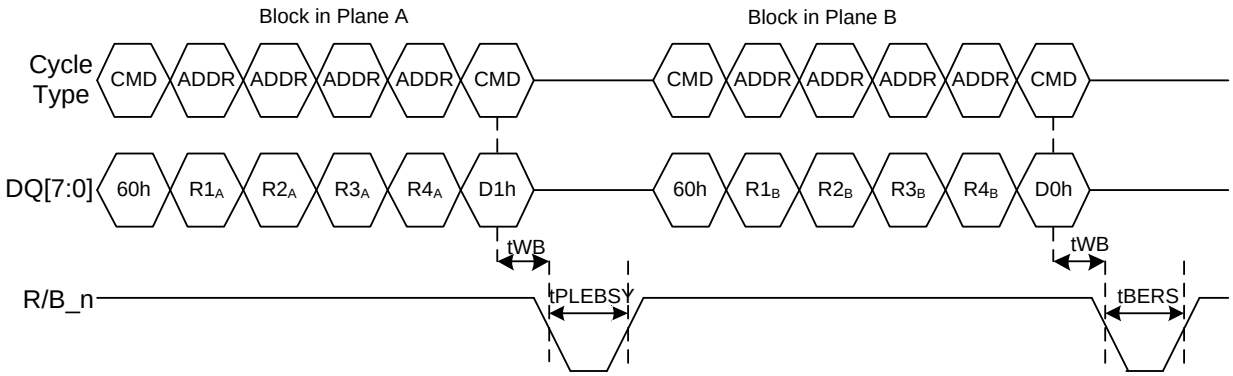
If the host attempts to erase a factory marked bad block, then the device shall not proceed with the requested operation and shall set the FAIL bit to one for the operation.

Figure 89. Block Erase Sequence



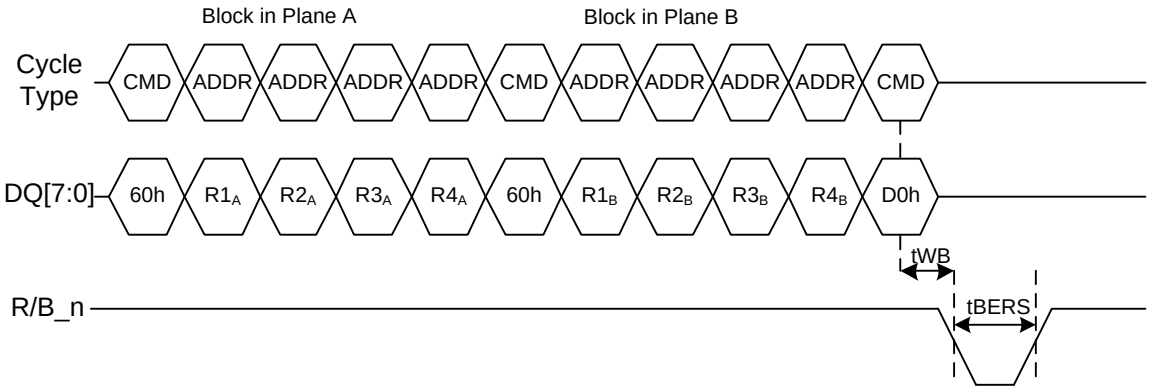
This NAND device supports multi-plane operation. Multi-Plane Block Erase sequence is shown as below.

Figure 90. Multi-Plane Block Erase Sequence 1



The ONFI-JEDEC Joint Taskgroup has defined a modified version of multi-plane block erase, where subsequenct row addresses specifying additional blocks to erase are not separated by D1h commands. This product supports this version.

Figure 91. Multi-Plane Block Erase Sequence 2, ONFI-JEDEC Joint Taskgroup Primary Definition



6.6.2. Erase Suspend (67h)

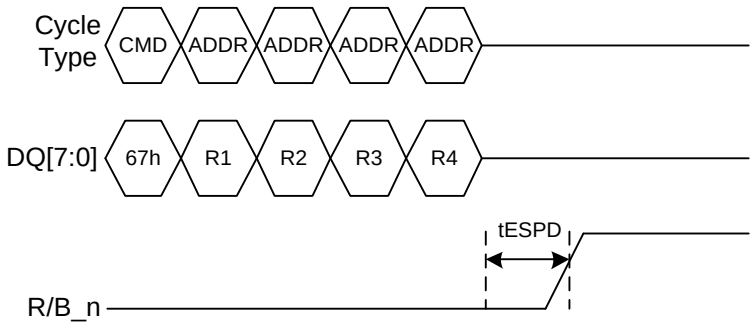
The Erase Suspend command is used to interrupt an Erase operation for a specified LUN with 4 address cycles; the plane and page address are ignored. The command can be issued at any time during an Erase operation. The command is ignored if the device is already in suspending mode or the device is not in erase progress.

Once the command is issued, it is necessary to issue Read Status (70h) command and polling SR[6] to find out when the program controller has paused. Once SR[6] turns from zero to one, then the host should check SR[3]. If SR[3] is one, the erase operation is successfully suspended. If SR[3] is zero, the erase operation is already completed. The suspend latency is defined by tESPD. If any error happens, SR[0] is set to one.

When the specified LUN is in erase suspend mode, for the operations on the same LUN, only the following commands are allowed:

1. Reset Commands (FFh, FAh, FCh) would cancel the suspended erase operation and reset the Status Bits to 'b0. Array data is not guaranteed;
2. Page read operation and Multi-Plane read operation on different blocks on the same LUN is allowed. If reading from the same block in erase suspend mode, the output data is undetermined;
3. All the Status Read commands, ZQ calibration, Mode Switching, Set Feature and Get Feature commands are allowed;
4. If the Multi-Plane erase operation is ongoing, Erase Suspend commands will suspend both planes at the same time;
5. Issuing Erase commands during erase suspend will set SR[0] to one;
6. Program in erase suspend mode is not allowed. SR[0] will be set to one;
7. During erase suspend, it is forbidden to use VSC to change the settings.

Figure 92. Erase Suspend Sequence



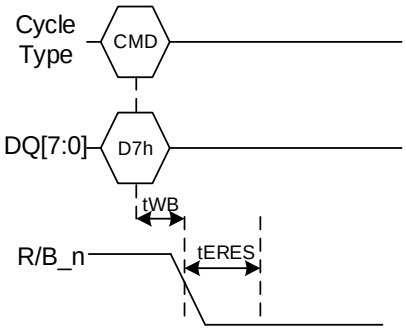
6.6.3. Erase Resume (D7h)

To resume a suspended erase operation for a specified LUN, issue the Erase Resume command. The host needs to select the suspended LUN before issuing the Erase Resume command. This command can be

ignored if the device is not in suspending mode. The resume latency is defined by tERES to improve the effectiveness of erase operation and avoid infinite erase times. Host is allowed to issue the next Erase Suspend command if polling SR[2] to return '0' by issuing Read Status (70h) command.

If the Multi-Plane erase operation is suspended, both planes will be resumed at the same time.

Figure 93. Erase Resume Sequence



6.7. ZQ Calibration Operations

6.7.1. ZQ Calibration Long (F9h)/ZQ Calibration Short (D9h)

ZQ calibration is recommended for NV-DDR2 and NV-DDR3 which the interface over 400MT/s speed.

ZQ Calibration is performed by issuing F9h command for ZQCL (ZQ Calibration Long) and D9h command for ZQCS (ZQ Calibration Short). ZQ Calibration is used to calibrate NAND Ron & ODT values. A longer time is required to calibrate the output driver and ODT circuits at initialization and relatively smaller time to perform periodic calibrations.

ZQCL is used to perform the initial calibration after power-up initialization sequence. The command to enable ZQCL may be issued at any time by the controller depending on the system environment. ZQCL triggers the calibration engine inside the NAND and once calibration is achieved, the calibrated values are transferred from the calibration engine to NAND IO, which updates the output driver and ODT values.

ZQCL is allowed a timing period of tZQCL to perform the full calibration and the transfer of values. ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter tZQCS. One ZQCS command can effectively correct a minimum of 1.5% (ZQ Correction) of RON and Rtt impedance error within tZQCS.

The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.

Other activities, including read status, should not be performed on the NAND channel (i.e. data bus) by the controller during tZQCL or tZQCS. The quiet time on the NAND channel allows accurate calibration of output driver and ODT values. For multi-channel packages, all channels should not have any data transfer during ZQ Calibration even if the devices are not sharing a channel with the LUN performing ZQ Calibration. Once NAND calibration is achieved, the NAND should disable ZQ current consumption path to reduce power. NAND array operations may not occur on the device performing the ZQCS or ZQCL operation. NAND array operations may occur on any devices that share the ZQ resistor with the device performing ZQCS or ZQCL. All devices connected to the DQ bus shall be in high impedance during the calibration procedure. The R/B# signal will be brought low by the device during calibration time, but if other devices are driving a shared R/B_n low then the host is required to wait the maximum tWB+tZQCS before issuing any commands to the data bus.

If a Reset command is issued during ZQ Calibration, the state of the NAND device output driver strength and ODT is not guaranteed and the host shall re-run calibration operation. If a Reset command (FFh, FAh, FCh) is issued during ZQ Calibration Long (ZQCL) operation, the Reset operation is executed and the NAND device will revert to factory settings for output driver strength and ODT values (e.g. as if no ZQ Calibration was performed). If a Reset command (FFh, FAh, FCh) is issued during ZQ Calibration Short (ZQCS) operation, the Reset operation is executed and the NAND device will return to vendor specific settings for

output driver strength and ODT values. When either ZQCL or ZQCS is aborted with a Reset command, the reset time will be less than 10µs (i.e. tRST < 10µs). In systems that share the ZQ resistor between NAND devices, the controller must not allow any overlap of tZQCL or tZQCS between the devices.

Table 80. ZQ Calibration Timing Parameters

Parameter	Description	Typ	Maximum
tZQCL	Normal Operation Long Calibration Time	485ns	TBD
tZQCS	Normal Operation Short Calibration Time	410ns	TBD

Notes: When more than 8 LUNs share a ZQ resistor, tZQCL and tZQCS values may be greater than specified values.

Figure 94. ZQ Calibration Long Sequence

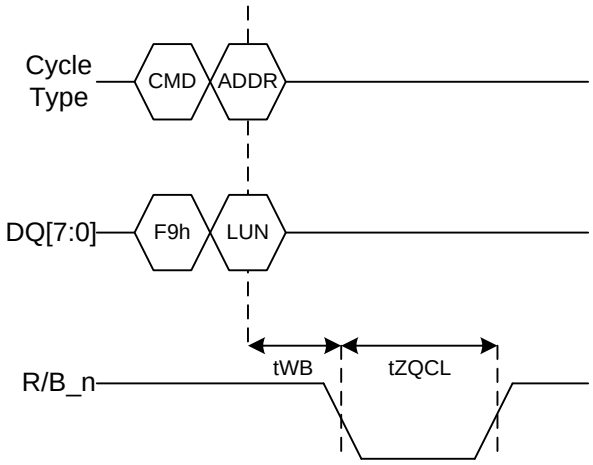
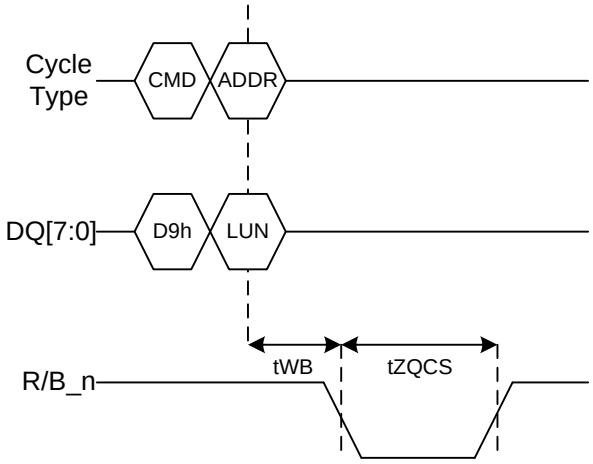


Figure 95. ZQ Calibration Short Sequence



6.7.1.1. ZQ External Resistor Value, Tolerance and Capacitive Loading

In order to use the ZQ Calibration function, a R_{ZQ}=300 Ohms±1% tolerance external resistor must be connected between the ZQ pin and ground. The ZQ resistance is the sum of the trace resistance and the actual resistor resistance. A single resistor can be used for each NAND device or one resistor can be shared between up to the vendor specified number of NAND devices if the ZQ calibration timings for each NAND do not overlap. The C_{Die} component of the ZQ signal will be less than an I/O signal. Depending on the number of die per package the total capacitance ($C_{Package}$+C_{Die}) of the ZQ signal may exceed an I/O signal. For packages with eight or more dies that share a ZQ signal, the total ZQ capacitance will not exceed 15% greater than the number of die times the C_{Die} of an I/O signal [i.e. Total ZQ capacitance<1.15*C_{Die}(I/O)]. The NV-DDR3 driver supports two different Ron values: 35 Ohms and 50 Ohms. Output driver impedance R_{ON} is defined by the value of the external reference resistor R_{ZQ} as follows: $R_{ON}35$=R_{ZQ}/8.5 (nominal 35 Ohms ±15% with nominal R_{ZQ} = 300 Ohms)

6.8. Volume Select Operations

6.8.1. Volume Select (E1h)

The Volume Select command is used to select a particular volume based on the address specified. Volume Select is required to be used when when matrix termination is used.

This command is accepted by all NAND targets that are connected to a particular host target. The command may be executed with any LUN on the volume in any state. The Volume Select command may only be issued as the first command after CE_n is pulled low; CE_n shall be remain high for tCEH in order for the Volume Select command to be properly received by all NAND targets connected to the host target.

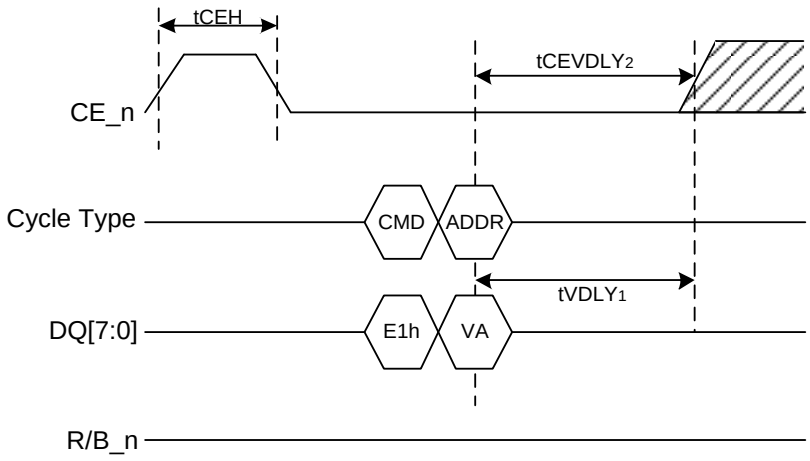
If volumes that share a host target are set to use different data interfaces, then the host shall issue the Volume Select command in the SDR data interface.

When the Volume Select command is issued, all NAND targets that have a Volume address that does not match the address specified shall be deselected to save power (equivalent behavior to CE_n pulled high). If one of the LUNs in an unselected volume is an assigned terminator for the selected volume, then that LUN will enter the sniff state.

If the volume address specified does not correspond to any appointed volume address, then all NAND targets shall be deselected until a subsequent Volume Select command is issued. If the Volume Select command is not the first command issued after CE_n is pulled low, then the NAND Targets revert to their previously selected, deselected or sniff states.

The volume address is retained across all reset commands.

Figure 96. Volume Select Sequence



Notes:

1. The host shall not issue new commands to any LUN on any Volume until after tVDLY. This delay is required to ensure that the appropriate Volume is selected for the next command issued;
2. The host shall not bring CE_n high on any Volume until after tCEVDLY. This delay is required to ensure that the appropriate Volume is selected based on the previously issued Volume Select command.

6.9. ODT Configure Operations

6.9.1. ODT Configure (E2h)

The ODT Configure command is used to configure ODT when using matrix termination. Specifically, ODT Configure specifies whether a particular LUN is a terminator for a volume(s) and the R_{TT} settings. If the LUN is specified as a terminator for one or more volumes, then the LUN shall enable ODT when either data input or data output cycles are executed on the volume(s) for which the LUN acts as a terminator.

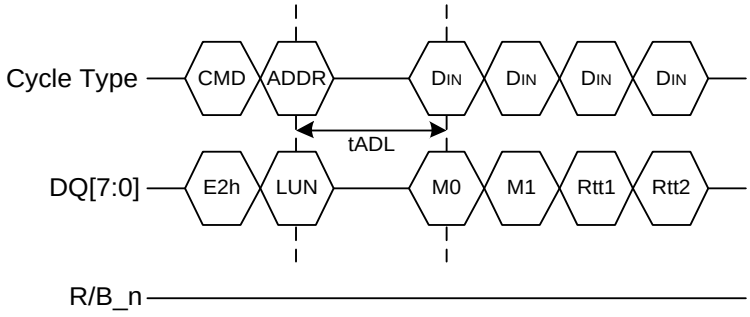
If ODT Configure is used to specify the Rtt settings for any LUN, then it shall be used to specify the R_{TT} settings for LUNs on all volumes. In this case, ODT Configure shall be issued to at least one LUN on each volume. Then, the volume shall begin using the ODT Configuration Matrix for all LUNs on that volume. The default value for the ODT Matrix is 0000h, i.e., termination is disabled.

When issuing ODT Configure in the NV-DDR2 or NV-DDR3 data interface, each data byte is transmitted twice. The device shall only latch one copy of each data byte.

When this command is issued and the NV-DDR2 or NV-DDR3 data interface is enabled, the updated termination settings take effect immediately. The host should take care to modify these settings to avoid any signal integrity issues. If issues occur when the NV-DDR2 interface is enabled, it is recommended to transition to the SDR data interface, make appropriate updates to the termination settings, and then transition back to the NV-DDR2 data interface. If issues occur when NV-DDR3 interface is enabled, it is recommended to transition to a slower timing mode, make appropriate updates to the termination settings, and then transition back to the faster NV-DDR3 timing mode.

The ODT settings are retained across all reset commands, including Reset (FFh).

Figure 97. ODT Configure Timing Sequence



Notes:

1. LUN: LUN that acts as a terminator. This field is formatted in the same manner as the row address byte that contains the LUN address;
2. M0: Lower byte of the ODT configuration matrix;

3. M1: Upper byte of the ODT configuration matrix;
4. Rtt1: Termination settings for DQ[7:0]/DQS;
5. Rtt2: Termination settings for RE_n;
6. R: Reserved (0h).

The table below defines the ODT configuration matrix specified as part of the command. If a bit is set to one, then the LUN shall act as the terminator for the corresponding volume (Vn) where n corresponds to the volume address.

Table 81. ODT Configuration Matrix

Volume Address	7	6	5	4	3	2	1	0
M0	V7	V6	V5	V4	V3	V2	V1	V0
M1	V15	V14	V13	V12	V11	V10	V9	V8

The table below defines the ODT settings specified as part of the command, including the Rtt values for DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c.

Table 82. On-die Termination Settings

R_{TT} Settings	7	6	5	4	3	2	1	0
R_{TT1}	DQ[7:0]/DQS R_{TT} & ODT Enable for Data Output(2)				DQ[7:0]/DQS R_{TT} & ODT Enable for Data Input(1)			
R_{TT2}	Reserved				RE_n R_{TT} & ODT Enable(3)			

Notes:

1. This field controls the ODT settings for the DQ[7:0], DQS_t and DQS_c signals for data input operations.
   The values are:
   0h=ODT disabled
   1h=ODT enabled with R_{TT} of 150 Ohms
   2h=ODT enabled with R_{TT} of 100 Ohms
   3h=ODT enabled with R_{TT} of 75 Ohms
   4h=ODT enabled with R_{TT} of 50 Ohms
   5h=ODT enabled with R_{TT} of 30 Ohms (not supported)
   6h-Fh Reserved
2. This field controls the ODT settings for the DQ[7:0], DQS_t and DQS_c signals for data output operations.
   The values are:
   0h = ODT disabled
   1h = ODT enabled with R_{TT} of 150 Ohms
   2h = ODT enabled with R_{TT} of 100 Ohms
   3h = ODT enabled with R_{TT} of 75 Ohms
   4h = ODT enabled with R_{TT} of 50 Ohms
   5h = ODT enabled with R_{TT} of 30 Ohms (not supported)
   6h-Fh Reserved

3. This field controls the ODT settings for the RE_t and RE_c signals.

   The values are:

   0h = ODT disabled

   1h = ODT enabled with R_{TT} of 150 Ohms

   2h = ODT enabled with R_{TT} of 100 Ohms

   3h = ODT enabled with R_{TT} of 75 Ohms

   4h = ODT enabled with R_{TT} of 50 Ohms

   5h = ODT enabled with R_{TT} of 30 Ohms (not supported)

   6h-Fh Reserved

6.10. Mode Switch Operations

6.10.1. SLC Access (DAh)/ SLC Abort (DFh)

The device can configured to SLC mode by issuing SLC Access command. SLC mode expects to be operated with data which requires frequent update, high-speed and high-reliability. On the other side, TLC mode expects to be operated with data which is large-sized or sequential.

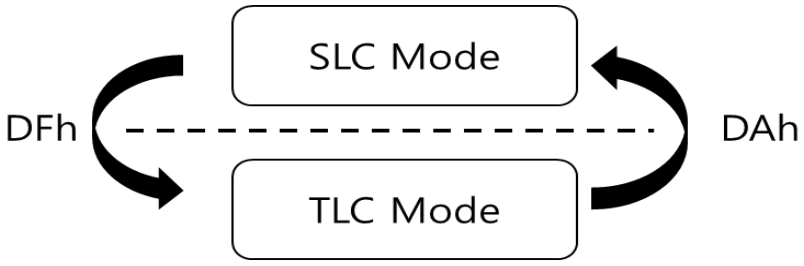
The device is operated with TLC mode at power-up. In order to operate with SLC mode, DAh command must be added in front of normal command. For example, in case of Page Program operation, if the page should be programmed reliably, DAh command must be added in front of 80h. Once device enters into SLC mode, additional DAh command is not needed until the device is switched to TLC mode by SLC Abort (DFh) command. Silimar to Program Operation, DAh command should be added in front of Read or Erase Operation in SLC mode. All commands are supported in SLC mode, except Program Suspend and Resume.

The device will exit SLC mode as well if Reset commands (FFh/FCh/FAh/FDh) are issued.

It is recommended to configure a block to one mode. If a block is used in different modes, such as SLC in one PE cycle and TLC in the next PE cycle, the total endurance cycle should still follow the TLC endurance specification. Before writing in the block in a certain mode, the host needs to erase the block in the same mode. For example, if the block is going to be programmed in SLC mode, the block needs to be erased in SLC mode. The reliability is not guaranteed in mixing modes.

Mode switch is allowed between suspend and resume operation. To ensure that the device is in correct cell mode, the host can issue Get Features (EEh) command or LUN Get Features (D4h) command on feature address C0h.

Figure 98. Mode Switch Flow



Notes:

SLC Access (DAh)/SLC Abort (DFh) is a LUN-level command. After power-up or hard reset, LUN0 will be selected by default if the host doesn't issue Read Status Enhanced command to do LUN selection.

Figure 99. SLC Program Sequence

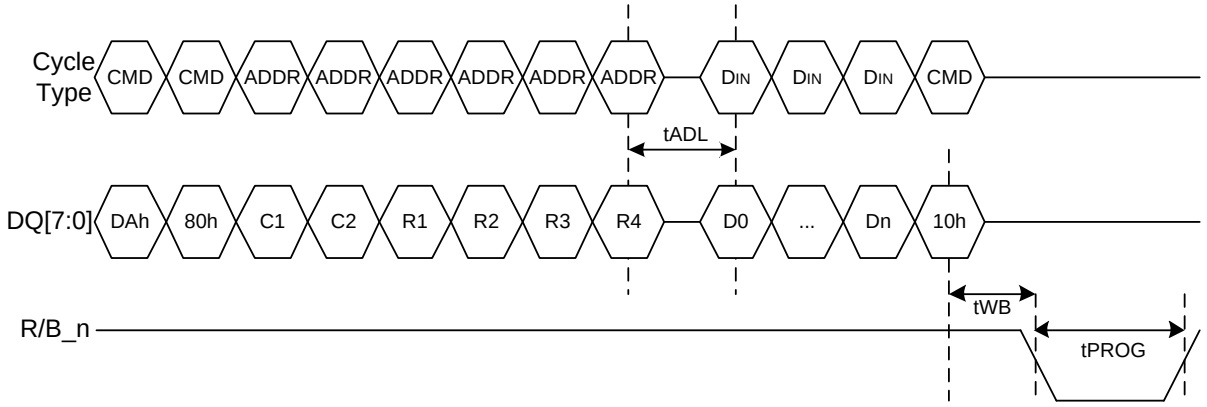


Figure 100. Restoring to TLC Program Sequence

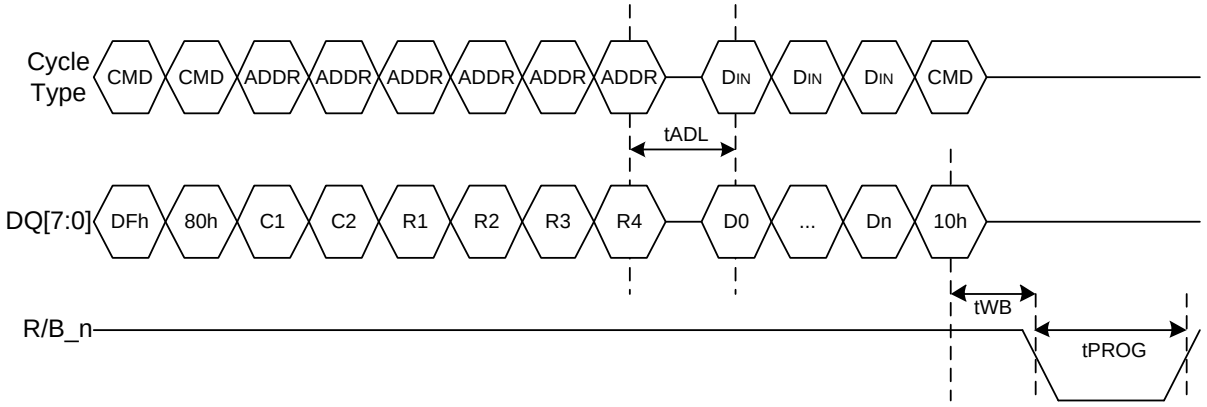


Figure 101. SLC Read Sequence

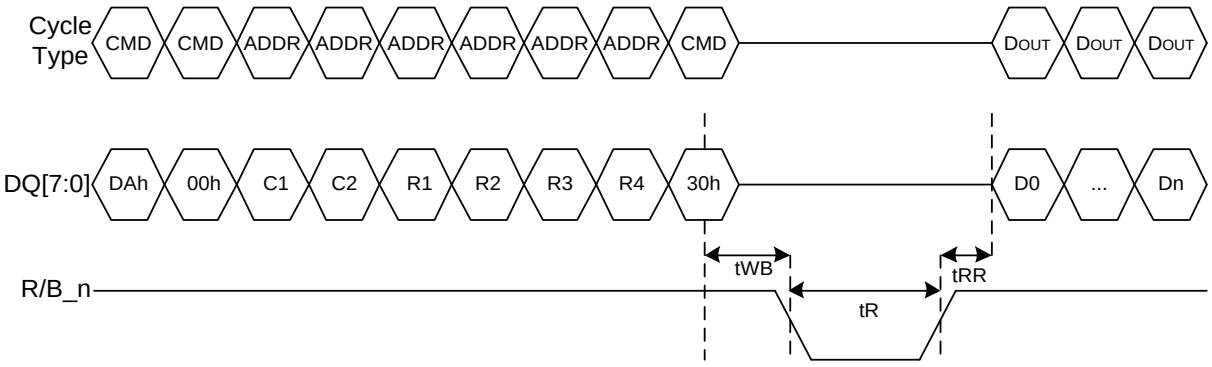
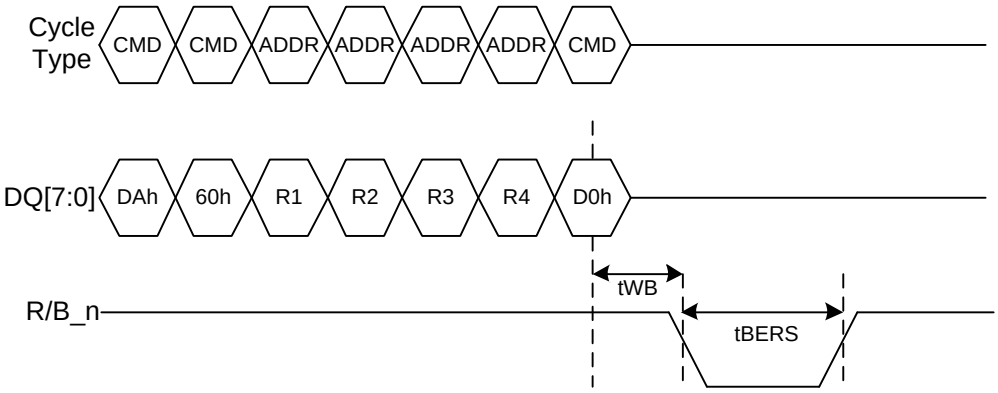


Figure 102. SLC Erase Sequence

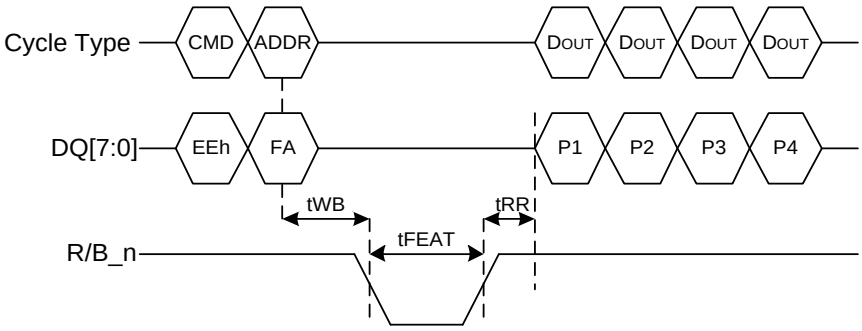


6.11. Feature Operations

6.11.1. Get Features (EEh)

The Get Features command is used to determine the current settings for a particular feature. This function shall return the current settings for the feature (including modifications that may have been previously made with the Set Features command). Parameters are always transferred on the lower 8-bits of the data bus. After reading the first byte of data, the host shall complete reading all desired data before issuing another command (including Read Status or Read Status Enhanced). When issuing Get Features in the NV-DDR2 or NV-DDR3 data interface, each data byte is received twice. The host shall only latch one copy of each data byte. If Read Status or Read Status Enhanced is used to monitor when the tFEAT time is up, the host shall issue a command value of 00h to begin transfer of the feature data starting with parameter P1.

Figure 103. Get Features Sequence



Notes:

1. FA: Feature address identifying feature to return parameters for;
2. P1-P4: Current settings/parameters for the feature identified by argument P1;
3. P1: Sub feature parameter 1 setting;
4. P2: Sub feature parameter 2 setting;
5. P3: Sub feature parameter 3 setting;
6. P4: Sub feature parameter 4 setting.

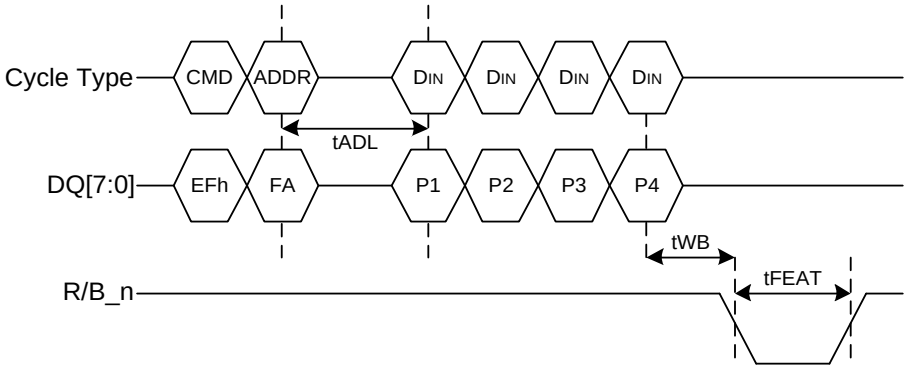
6.11.2. Set Features (EFh)

The Set Features command modifies the settings of a particular feature. For example, this function can be used to enable a feature that is disabled at power-on. Parameters are always transferred on the lower 8-bits of the data bus.

When issuing Set Features in the source synchronous data interface, each data byte is transmitted twice. The device shall only latch one copy of each data byte.

Set Features is used to change the timing mode, data interface type and some operation's behavior. When changing the timing mode, the device is busy for tITC, not tFEAT. During the tITC time, the host shall not poll for status.

Figure 104. Set Features Sequence



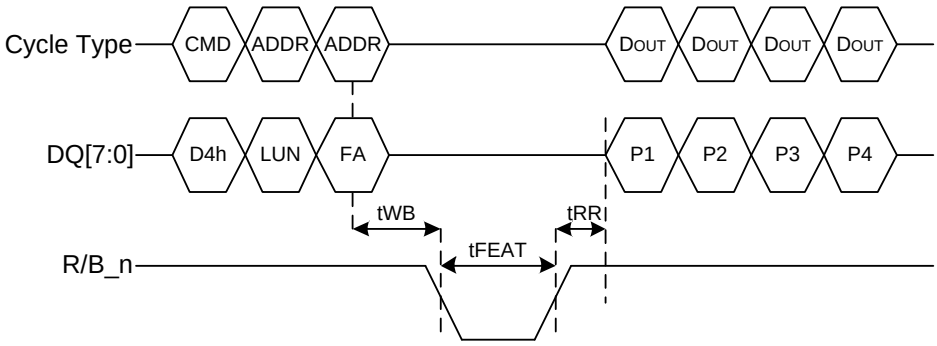
Notes:

1. FA: Feature address identifying feature to modify settings for;
2. P1-P4: Parameters identifying new settings for the feature specified;
3. P1: Sub feature parameter 1;
4. P2: Sub feature parameter 2;
5. P3: Sub feature parameter 3;
6. P4: Sub feature parameter 4.

6.11.3. LUN Get Features (D4h)

LUN Get Features (D4h) command can be used to read Get Feature information of a special LUN. LUN address input by the host is needed.

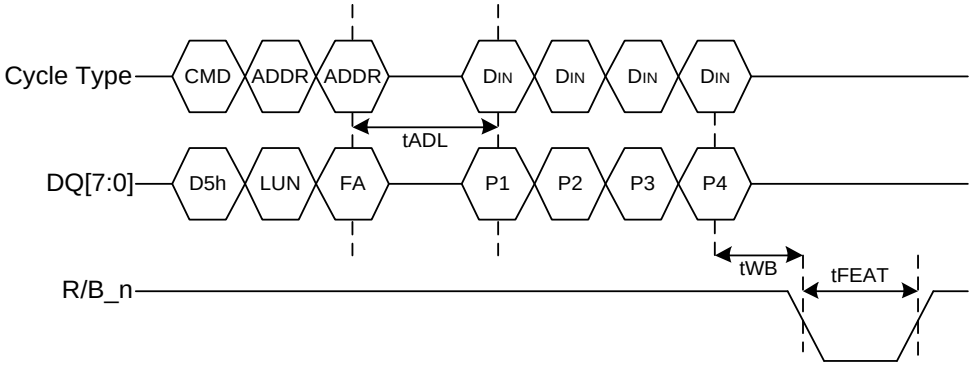
Figure 105. LUN Get Features Sequence



6.11.4. LUN Set Features (D5h)

LUN Set Features command can be used to set feature information of a special LUN. LUN address input by the host is needed.

Figure 106. LUN Set Features Sequence



6.11.5. Feature Definitions

Table 83. Basic Features Address

Feature Address	Description
01h	Timing Mode
02h	NV-DDR2/NV-DDR3 Configuration
10h	Output Drive Strength
30h	External Vpp Configuration
58h	Volume Configuration

6.11.5.1. Timing Mode (01h)

When the SDR or NV-DDR2 data interface is enabled, the Data Interface setting and Timing Mode Number are not retained across Reset (FFh); after a Reset (FFh) the Data Interface shall be SDR and Timing Mode Number 0. All other settings for the timing mode are retained across Reset (FFh), Synchronous Reset (FCh), and Reset LUN (FAh) commands. If the Reset (FFh) command is issued when the Data Interface is configured as NV-DDR2, then the host shall use the SDR data interface in Timing Mode 0 until a new data interface and/or timing mode is selected with Set Features. The host shall only set a timing mode that is explicitly shown as supported in the Read Parameter Page.

To transition from NV-DDR2 data interface to the SDR data interface, the host should use the Reset (FFh) command instead of the Set Features command.

When V_{CCQ}=1.2V, the NV-DDR3 interface is enabled by default. Switching from the NV-DDR3 interface to the SDR or NV-DDR2 interfaces is not allowed. If sub feature parameter P1 the Data Interface bits [4:5] are changed, the device will remain in NV-DDR3 interface. If the Reset (FFh) command is issued when the Data Interface is NV-DDR3, the host shall continue to use the NV-DDR3 data interface. It is recommended that after the host issues Reset (FFh), Timing Mode 0 be used until the host reconfigures the device to support faster Timing Modes.

Table 84. Timing Mode Feature Enable Address: 01h

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	R	PC	Data Interface		Timing Mode Number			
P2	Reserved (0)							
P3	Reserved (0)							
P4	Reserved (0)							

Notes:

1. Timing Mode Number:
   Set to the numerical value of the maximum timing mode in use by the host. Default power-on value is 0h.
2. Data Interface:
   00b = SDR (default power-on value);

10b = NV-DDR2;

01b and 11b = Reserved ("Data Interface" is not supported for NV-DDR3).

3. PC:

   The Program Clear bit controls the program page buffer clear enhancement which defines the behavior of clearing the page buffer when a Program (80h) command is received. If cleared to zero, then the page buffer(s) for each LUN that is part of the target is cleared after the Program (80h) command is received. If set to one, only the page buffer for the LUN and interleave address selected with the Program (80h) command are cleared. The tADL time for Program commands is as reported in the parameter page.

4. Reserved/R:

   Reserved values shall be cleared to zero by the host. Targets shall not be sensitive to the values of reserved fields.

6.11.5.2. NV-DDR2/NV-DDR3 Configuration (02h)

This setting shall be supported if the target supports the NV-DDR2 or NV-DDR3 data interface. This setting controls differential signaling, basic ODT configuration, and warmup cycles for data input and output. For the NV-DDR2 interface, these settings are not retained across Reset (FFh) and the power-on values are reverted. For the NV-DDR3 data interface, these settings are retained Reset (FFh). For both the NV-DDR2 and NV-DDR3 interfaces, these settings are retained across Synchronous Reset (FCh) and Reset LUN (FAh) commands. The power-on default is 0h for all fields.

The NV-DDR2 data interface shall be enabled in the Timing Mode feature for these settings to take effect. It is recommended that this feature be configured prior to enabling the NV-DDR2 data interface.

When this feature is changed and the NV-DDR2 or NV-DDR3 data interface is enabled, then the updated settings take effect immediately. The host should take care when modifying these settings while NV-DDR2 or NV-DDR3 is enabled to avoid any signal integrity issues. If issues occur while NV-DDR2 is enabled, then it is recommended to transition to the SDR data interface, make the appropriate updates to this feature, and then transition back to the NV-DDR2 data interface. If issues occur while NV-DDR3 is enabled, then it is recommended to transition to Timing Mode 0, make appropriate updates to this feature, and then transition back to the desired Timing Mode. If these settings are modified, the host should take care to ensure that appropriate settings are applied in a manner that avoids signal integrity issues.

Table 85. NV-DDR2/NV-DDR3 Configuration Feature Enable Address: 02h

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	DQ/DQS/RE_n ODT Enable				R	CMPR	CMPD	VEN
P2	Warmup DQS cycles for Data Input				Warmup RE_n and DQS cycles for Data Output			
P3	Reserved							
P4	Reserved							

Notes:

1. VEN:

   1b = external V_{REFQ} is used as a reference for the input and I/O signals;

0b = internal V_{REFQ} is used as an input reference for the input and I/O signals;

CE_n and WP_n are CMOS signals. Implementations may use CMOS or SSTL_18 (NV-DDR2) or NV-DDR3 input levels for WE_n, ALE, and CLE. For all other signals, including DQ[7:0], DQS_t, and RE_t, SSTL_18 (NV-DDR2) or NV-DDR3 input levels are used regardless of V_{REFQ} configuration. If VEN=0, then $V_{CCQ}/2$ (not V_{REFQ}) is used as reference. RE_t, DQS_t only use V_{REFQ} when CMPD, CMPR are cleared to zero.

2. CMPD:

   If set to one, then the complementary DQS (DQS_c) signal is enabled. If cleared to zero, then the complementary DQS (DQS_c) signal is not used.

3. CMPR:

   If set to one, then the complementary RE_n (RE_c) signal is enabled. If cleared to zero, then the complementary RE_n (RE_c) signal is not used.

4. DQ/DQS/RE_n ODT Enable:

   This field controls the ODT settings for the DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c signals. The values are:

   0h = ODT disabled

   1h = ODT enabled with Rtt of 150 Ohms

   2h = ODT enabled with Rtt of 100 Ohms

   3h = ODT enabled with Rtt of 75 Ohms

   4h = ODT enabled with Rtt of 50 Ohms

   5h = ODT enabled with Rtt of 30 Ohms (Optional)

   Rtt settings may be specified separately for DQ[7:0]/DQS and the RE_n signals. The DQ[7:0]/DQS may be specified separately for data input versus data output operation. Refer to the definition of the ODT Configure command. If values are specified with the ODT Configure command, then this field is not used. Get Features returns the previous value set in this field, regardless of the Rtt settings specified using ODT Configure.

5. Warmup RE_n and DQS cycles for Data Output:

   This field indicates the number of warmup cycles of RE_n and DQS that are provided for data output. These are the number of initial “dummy” RE_t/RE_c cycles at the start of data output operations. There are corresponding “dummy” DQS_t/DQS_c cycles to the “dummy” RE_t/RE_c cycles that the host shall ignore. The values are:

   0h = 0 cycles, feature disabled

   1h = 1 warmup cycle

   2h = 2 warmup cycles

   3h = 4 warmup cycles

   4h-Fh = Reserved

6. Warmup DQS cycles for Data Input:

   This field indicates the number of warmup cycles of DQS that are provided for data input. These are the number of initial “dummy” DQS_t/DQS_c cycles at the start of data input operations. The values are:

   0h = 0 cycles, feature disabled

   1h = 1 warmup cycle

   2h = 2 warmup cycles

   3h = 4 warmup cycles

   4h-Fh = Reserved

7. Reserved:
   Reserved values shall be cleared to zero by the host. Targets shall not be sensitive to the value of reserved fields.

6.11.5.3. Output Drive Strength (10h)

The I/O drive strength setting shall be retained across Reset (FFh), Synchronous Reset (FCh), and Reset LUN (FAh) commands. The power-on default drive strength value is the 35 Ohms (10b) setting.

Table 86. Output Drive Strength Feature Enable Address: 10h

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	Reserved (0)						Drive Strength	
P2	Reserved (0)							
P3	Reserved (0)							
P4	Reserved (0)							

Notes:

1. Drive strength:
   01b = 25 Ohms (Not supported for NV-DDR3)
   10b = 35 Ohms (power-on default)
   11b = 50 Ohms
2. Reserved:
   Reserved values shall be cleared to zero by the host. Targets shall not be sensitive to the value of reserved fields.

6.11.5.4. External V_{PP} Configuration (30h)

This setting shall be supported if the target supports external V_{PP} as specified in the parameter page. This setting controls whether external Vpp is enabled. This setting is retained across Reset (FFh), Synchronous Reset (FCh) and Reset LUN (FAh) commands. The power-on default is 0h for all fields. The Hard Reset (FDh) command will disable the VPP feature and clear the VPP feature address back to its default value for the target LUN.

V_{PP} must be valid prior to Set Features that enables V_{PP}.

Table 87. External V_{PP} Configuration Feature Enable Address: 30h

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	Reserved (0)							Vpp
P2	Reserved (0)							
P3	Reserved (0)							
P4	Reserved (0)							

Notes:

1. V_{PP}:
   If 0b = External, Vpp is disabled;
   If 1b = External, Vpp is enabled;
2. Reserved:
   Reserved values shall be cleared to zero by the host. Targets shall not be sensitive to the value of reserved fields.

6.11.5.5. Volume Configuration (58h)

This setting is used to configure the Volume Address and shall be supported for NAND Targets that indicate support for Volume Addressing in the parameter page. The Volume is deselected until a Volume Select command is issued to select an associated Volume.

The host shall only set this feature once per power cycle for each Volume. The address specified is then used in Select Volume commands for accessing this NAND Target. This setting is retained across Reset (FFh), Synchronous Reset (FCh), and Reset LUN (FAh) commands. There is no default power-on value.

Table 88. Volume Configuration Feature Enable Address: 58h

Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	Reserved (0)				Volume Address			
P2	Reserved (0)							
P3	Reserved (0)							
P4	Reserved (0)							

Notes:

1. Volume Address:
   Assign volume address.
2. Reserved:
   Reserved values shall be cleared to zero by the host. Targets shall not be sensitive to the value of reserved fields.

Revision History

Rev	Date	Changes
0.1	2019/03	Initial release.
0.2	2019/10	Updated typical parameters for ES version. Updated parameter page data for ES version. Removed CE reduction feature and related content. Changed Eni/Eno pad to NU. Removed Eni/Eno related content. Changed typical VCC voltage to 2.5V. Changed operating temperature definition as case temperature. Changed operating temperature to 0~70° C, same as industrial common spec. Added cache operation in command sets. Updated block number in “Logical Memory Organization” figure.