NAND Flash Memory - Fortis Flash

MT29F256G08CBHBB, MT29F512G08CEHBB, MT29F1T08CMHBB
MT29F2T08CUHBB, MT29F4T08CTHBB

Features

- Open NAND Flash Interface (ONFI) 4.0-compliant[1]
- JEDEC NAND Flash Interoperability (JESD230B) compliant[2]
- Multiple-level cell (MLC)
- Organization
  - Page size x8: 18,592 bytes (16,384 + 2208 bytes)
  - Block size: 1024 pages, (16,384K + 2208K bytes)
  - Plane size: 4 planes x 548 blocks per plane
  - Device size: 256Gb: 2192 blocks; 512Gb: 4384 blocks; 1Tb: 8768 blocks; 2Tb: 17,536 blocks; 4Tb: 35,072 blocks
- NV-DDR3 I/O performance[5]
  - Up to NV-DDR3 timing mode 9
  - Clock rate: 3ns (NV-DDR3)
  - Read/write throughput per pin: 667 MT/s
- NV-DDR2 I/O performance[5]
  - Up to NV-DDR2 timing mode 8
  - Clock rate: 3.75ns (NV-DDR2)
  - Read/write throughput per pin: 533 MT/s
- NV-DDR I/O performance [5]
  - Up to NV-DDR timing mode 5
  - Clock rate: 10ns (NV-DDR)
  - Read/write throughput per pin: 200 MT/s
- Asynchronous I/O performance [5]
  - Up to asynchronous timing mode 5
  - ^{t}RC/^{t}WC: 20ns (MIN)
  - Read/write throughput per pin: 50 MT/s
- Array performance
  - Single-Plane EXPRESS READ operation time without/with V_{PP} 64/61µs (TYP) [3]
  - Single-Plane READ PAGE operation time without/with V_{PP} 66/63µs (TYP)[3]
  - Multi-Plane READ PAGE operation time without/with V_{PP} 77/63µs (TYP) [3]
  - Program page without/with V_{PP}: 1300µs/1225µs (TYP)
  - Erase block: 15ms (TYP)
- Operating Voltage Range
  - V_{CC}: 2.7–3.6V
  - V_{CCQ}: 1.7–1.95V; 1.14–1.26V
- Command set: ONFI NAND Flash Protocol
- Advanced Command Set
  - Program cache
  - Read cache sequential
  - Read cache random
  - One-time programmable (OTP) mode
  - Multi-plane commands
  - Multi-LUN operations
  - Read Unique ID
  - Copyback
  - SLC Mode[6]
  - Read Retry[7]
  - ZQ Calibration
- First block (block address 00h) is valid when shipped from factory. For minimum required ECC, see Error Management (page 187).[7]
- RESET (FFh) required as first command after power-on
- Operation status byte provides software method for detecting
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Data strobe (DQS) signals provide a hardware method for synchronizing data DQ in the NV-DDR/NV-DDR2/NV-DDR3 interface
- Copyback operations supported within the plane from which data is read
- On-die Termination (ODT) [4]
- Quality and reliability[7]
  - Testing methodology: JESD47
  - Data retention: See qualification report – May vary for targeted application
  - Endurance: 3000 PROGRAM/ERASE cycles
- Operating temperature:
  - Commercial: 0°C to +70°C
  - Industrial (IT): -40°C to +85°C
- Package
  - 132-ball BGA

Notes:
1. The ONFI 4.0 specification is available at www.onfi.org.
2. The JEDEC specification is available at www.jedec.org/standards-documents.
3. Contact factory for technical details regarding Randomization. Array read times listed are without internal randomization.

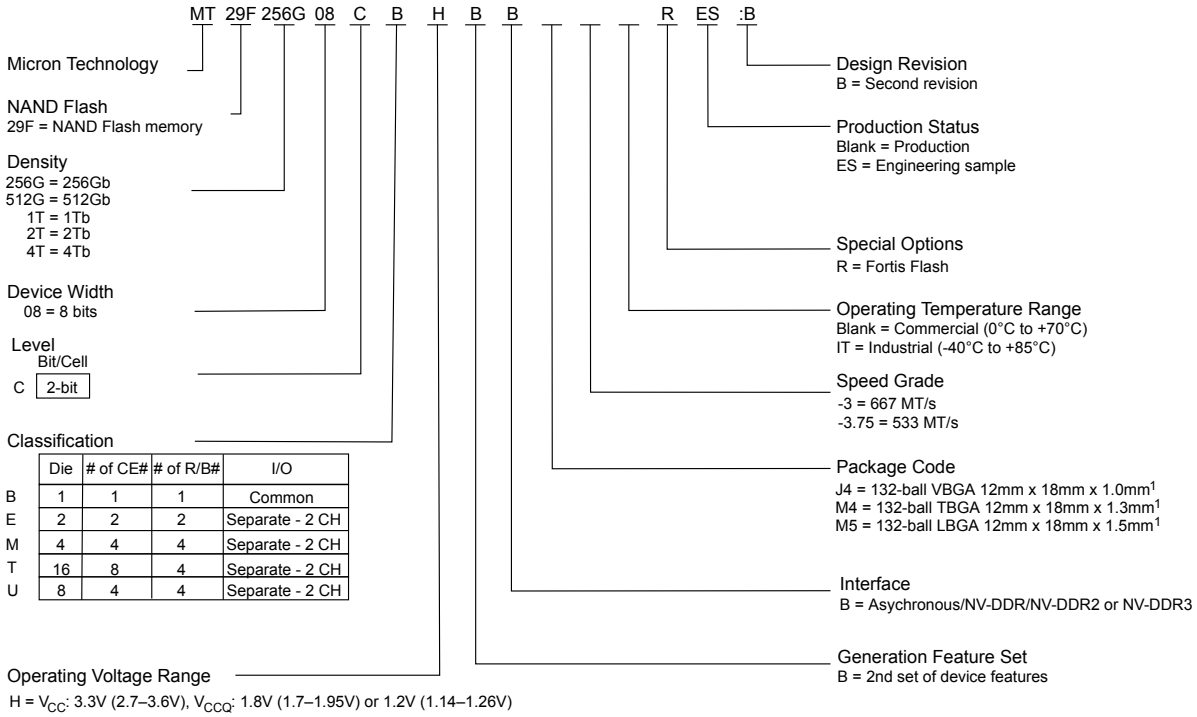
Release: 11/30/15

4. ODT functionality is supported only in NV-DDR2 or NV-DDR3.
5. Asynchronous, NV-DDR, and NV-DDR2 functionality is only available within the 1.8V V_{CCQ} supply range. NV-DDR3 functionality is only available within the 1.2V V_{CCQ} supply range.
6. Contact factory for technical details regarding SLC mode.
7. Read Retry operations are required to achieve specified endurance and for general array data integrity.

Part Numbering Information

Micron NAND Flash devices are available in different configurations and densities. Verify valid part numbers by using Micron's part catalog search at www.micron.com. To compare features and specifications by device type, visit www.micron.com/products. Contact the factory for devices not found.

Figure 1: Part Numbering



	Die	# of CE#	# of R/B#	I/O
B	1	1	1	Common
E	2	2	2	Separate - 2 CH
M	4	4	4	Separate - 2 CH
T	16	8	4	Separate - 2 CH
U	8	4	4	Separate - 2 CH

Note: 1. Pb-free package.

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General Description

Micron NAND Flash devices include an asynchronous data interface for I/O operations. These devices use a highly multiplexed 8-bit bus (DQx) to transfer commands, address, and data. There are five control signals used to implement the asynchronous data interface: CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection (WP#) and monitor device status (R/B#).

Some versions of this Micron NAND Flash device additionally includes a NV-DDR, NV-DDR2, and/or a NV-DDR3 data interface for high-performance I/O operations. When the NV-DDR interface is active, WE# becomes CLK and RE# becomes W/R#. Data transfers include a bidirectional data strobe (DQS).

This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign.

A target is the unit of memory accessed by a chip enable signal. A target contains one or more NAND Flash die. A NAND Flash die is the minimum unit that can independently execute commands and report status. A NAND Flash die, in the ONFI specification, is referred to as a logical unit (LUN). For further details, see Device and Array Organization.

Asynchronous, NV-DDR, NV-DDR2, NV-DDR3 Signal Descriptions

Table 1: Asynchronous, NV-DDR, NV-DDR2, and NV-DDR3 Signal Definitions

Asynchronous Signal[1]	NV-DDR Signal[1]	NV-DDR2 / NV-DDR3 Signal[1]	Type	Description[2]
ALE	ALE	ALE	Input	**Address latch enable:** Loads an address from DQx into the address register.
CE#	CE#	CE#	Input	**Chip enable:** Enables or disables one or more die (LUNs) in a target.
CLE	CLE	CLE	Input	**Command latch enable:** Loads a command from DQx into the command register.
DQx	DQx	DQx	I/O	**Data inputs/outputs:** The bidirectional I/Os transfer address, data, and command information.
–	DQS	DQS, DQS_t	I/O	**Data strobe:** Provides a synchronous reference for data input and output.
–	–	DQS_c	I/O	**Data strobe compliment:** Provides a complementary signal to the data strobe signal optionally used in the NV-DDR2 or NV-DDR3 interface for synchronous reference for data input and output.
ENi	ENi	ENi	Input	**Enumerate input**: Input to a NAND device (if first NAND device on the daisy chain have as NC) from ENo of a previous NAND device to support CE# pin reduction functionality.
ENo	ENo	ENo	Output	**Enumerate output**: Output from a NAND device to the ENi of the next NAND device in the daisy chain to support CE# pin reduction functionality.

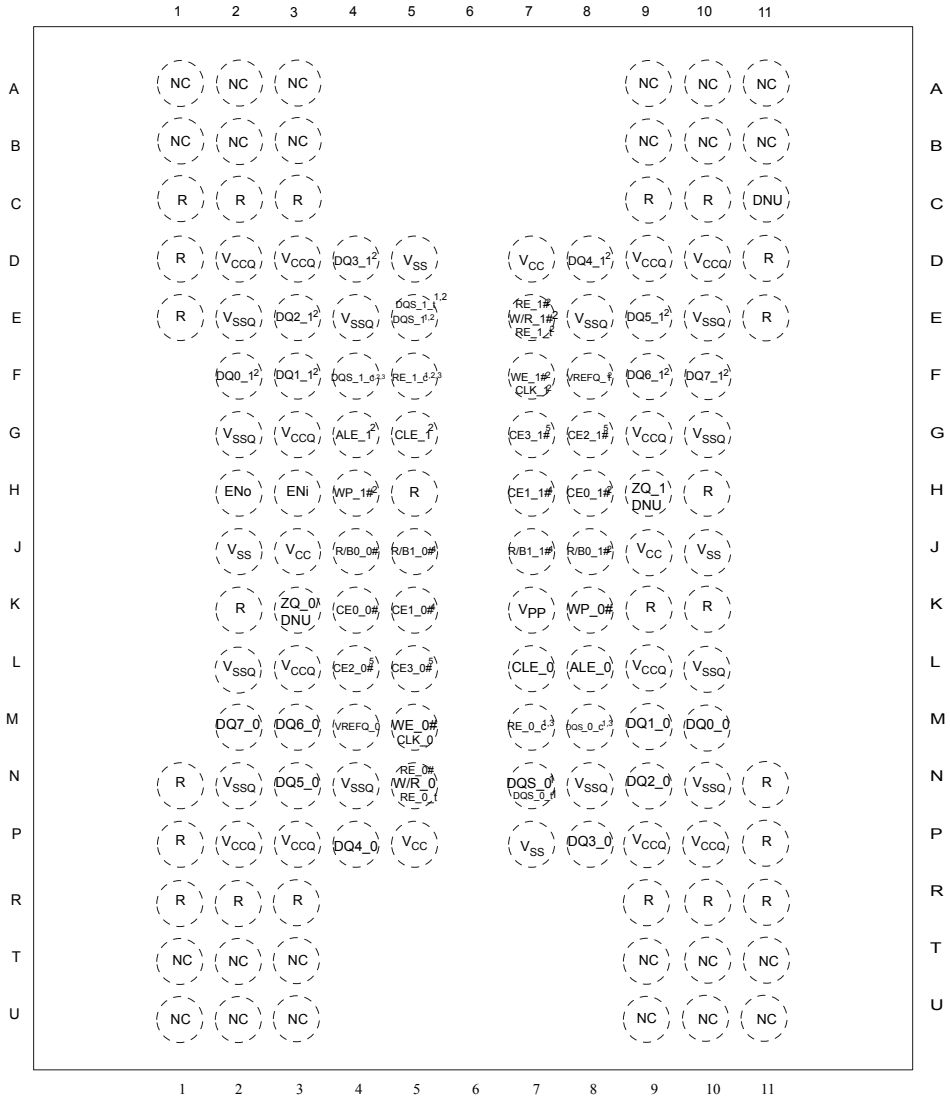
Table 1: Asynchronous, NV-DDR, NV-DDR2, and NV-DDR3 Signal Definitions (Continued)

Asynchronous Signal[1]	NV-DDR Signal[1]	NV-DDR2 / NV-DDR3 Signal[1]	Type	Description[2]
RE#	W/R#	RE#, RE_t	Input	**Read enable and write/read:** RE# transfers serial data from the NAND Flash to the host system when the asynchronous interface is active. When the NV-DDR interface is active, W/R# controls the direction of DQx and DQS.
–	–	RE_c	Input	**Read enable complement:** Provides a complementary signal to the read enable signal optionally used in the NV-DDR2 or NV-DDR3 interface for synchronous reference for data output.
WE#	CLK	WE#	Input	**Write enable and clock:** WE# transfers commands, addresses when the asynchronous, NV-DDR2, and NV-DDR3 interfaces are active, and serial data from the host system to the NAND Flash when the asynchronous interface is active. When the NV-DDR interface is active, CLK latches command and address cycles.
WP#	WP#	WP#	Input	**Write protect:** Enables or disables array PROGRAM and ERASE operations.
R/B#	R/B#	R/B#	Output	**Ready/busy:** An open-drain, active-low output that requires an external pull-up resistor. This signal indicates target array activity.
V_{CC}	V_{CC}	V_{CC}	Supply	**V_{CC}:** Core power supply
V_{CCQ}	V_{CCQ}	V_{CCQ}	Supply	**V_{CCQ}:** I/O power supply
V_{PP}	V_{PP}	V_{PP}	Supply	**V_{PP}:** The V_{PP} signal is an optional external high voltage power supply to the device. This high voltage power supply may be used to enhance operations (e.g., improved power efficiency).
V_{SS}	V_{SS}	V_{SS}	Supply	**V_{SS}:** Core ground connection
V_{SSQ}	V_{SSQ}	V_{SSQ}	Supply	**V_{SSQ}:** I/O ground connection
–	–	V_{REFQ}	Supply	**V_{REFQ}**: Reference voltage used with NV-DDR2 and NV-DDR3 interfaces
ZQ	ZQ	ZQ	–	**Reference pin for ZQ calibration**: This is used on ZQ calibration. The ZQ signal shall be connected to Vss through R_{ZQ} resistor.
NC	NC	NC	–	**No connect:** NCs are not internally connected. They can be driven or left unconnected.
DNU	DNU	DNU	–	**Do not use:** DNUs must be left unconnected.
RFU	RFU	RFU	–	**Reserved for future use:** RFUs must be left unconnected.

Notes:
1. See Device and Array Organization for detailed signal connections.
2. See sections Bus Operation - Asynchronous Interface, Bus Operation - NV-DDR Interface, Bus Operations - NV-DDR2 Interface, and Bus Operations - NV-DDR3 Interface for detailed Asynchronous, NV-DDR, NV-DDR2, and NV-DDR3 interface signal descriptions.

Signal Assignments

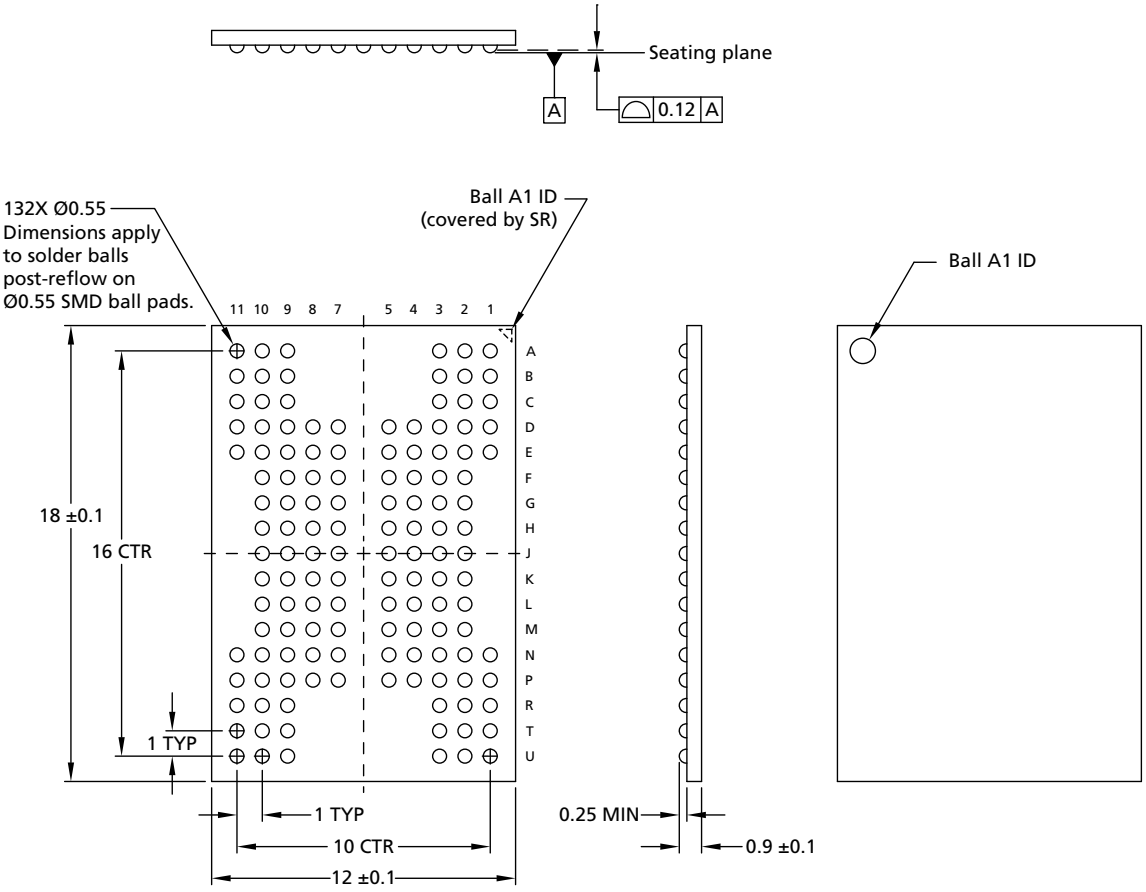
Figure 2: 132-ball BGA (Ball-Down, Top View)



Notes:
1. N/A: This signal is tri-stated when the asynchronous interface is active.
2. These signals are available on dual, quad, octal or higher die stacked die packages. They are NC for other configurations.
3. These signals are available when differential signaling is enabled.
4. These signals are available on quad die four CE# or octal die packages. They are NC for other configurations.
5. These signals are available on 16 LUN stacked packages. They are NC for other configurations.

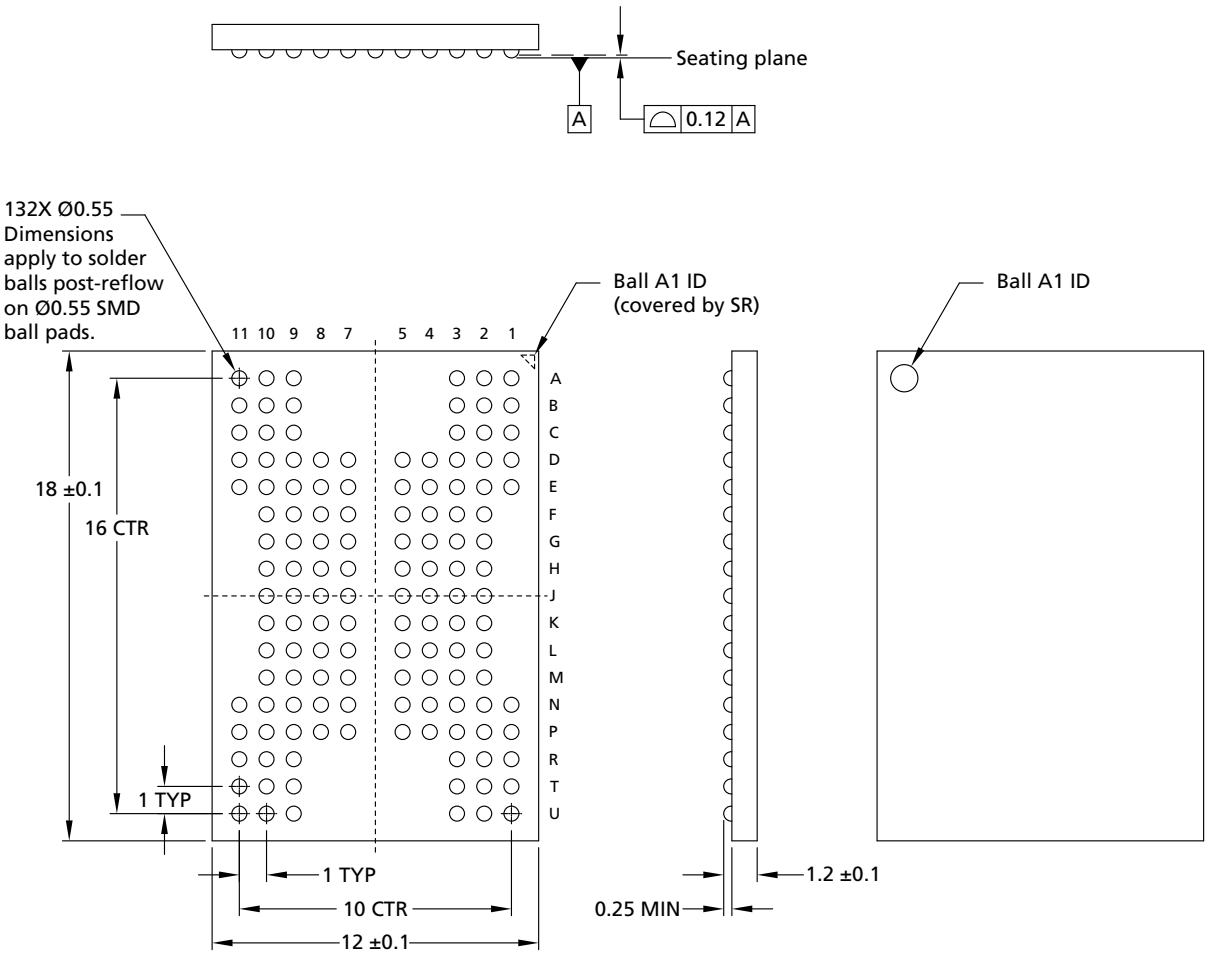
Package Dimensions

Figure 3: 132-Ball VBGA – 12mm x 18mm (Package Code: J4)



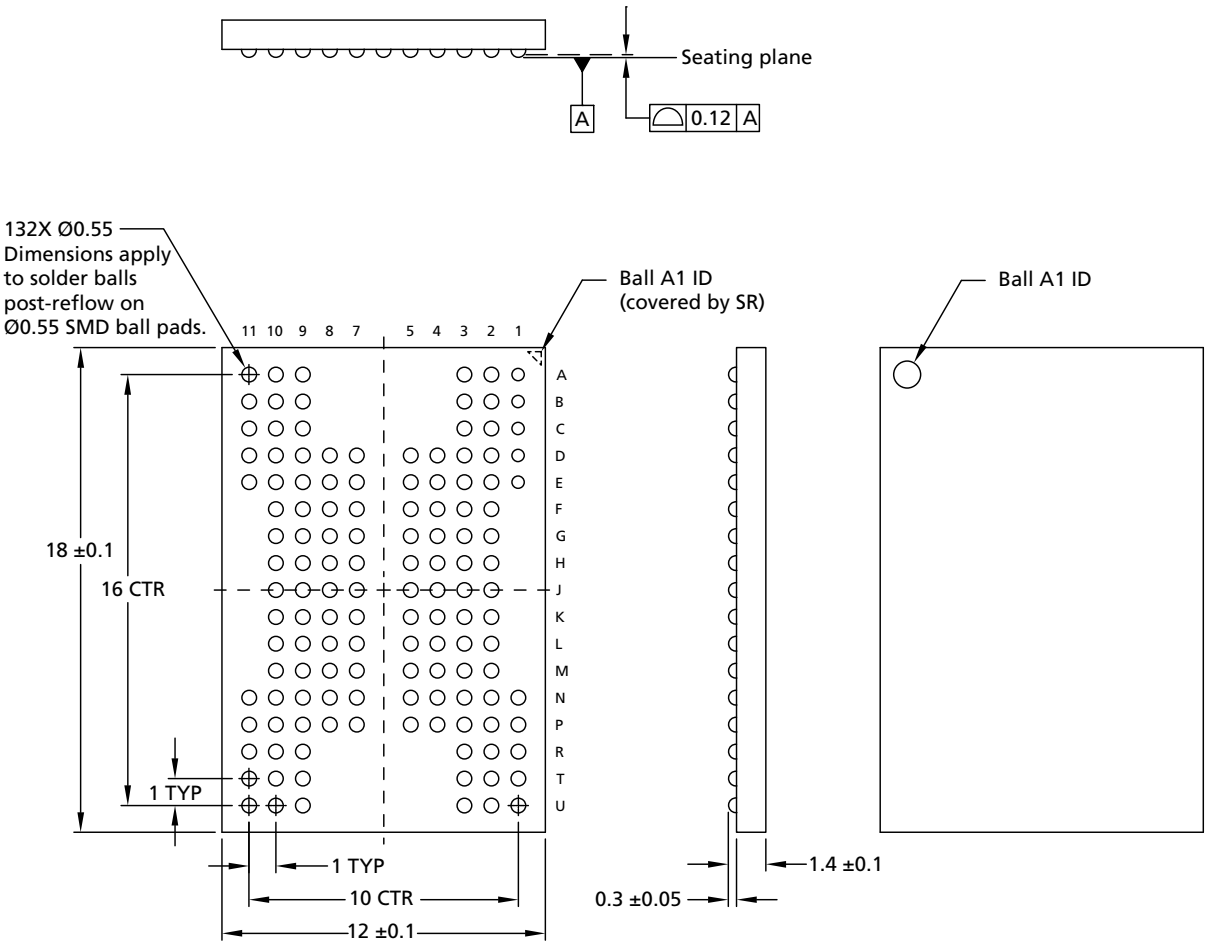
Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC405 (95.5% Sn, 4% Ag, 0.5% Cu).

Figure 4: 132-Ball TBGA – 12mm x 18mm (Package Code: M4)



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC405 (95.5% Sn, 4% Ag, 0.5% Cu).

Figure 5: 132-Ball LBGA – 12mm x 18mm (Package Code: M5)



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC405 (95.5% Sn, 4% Ag, 0.5% Cu).

Architecture

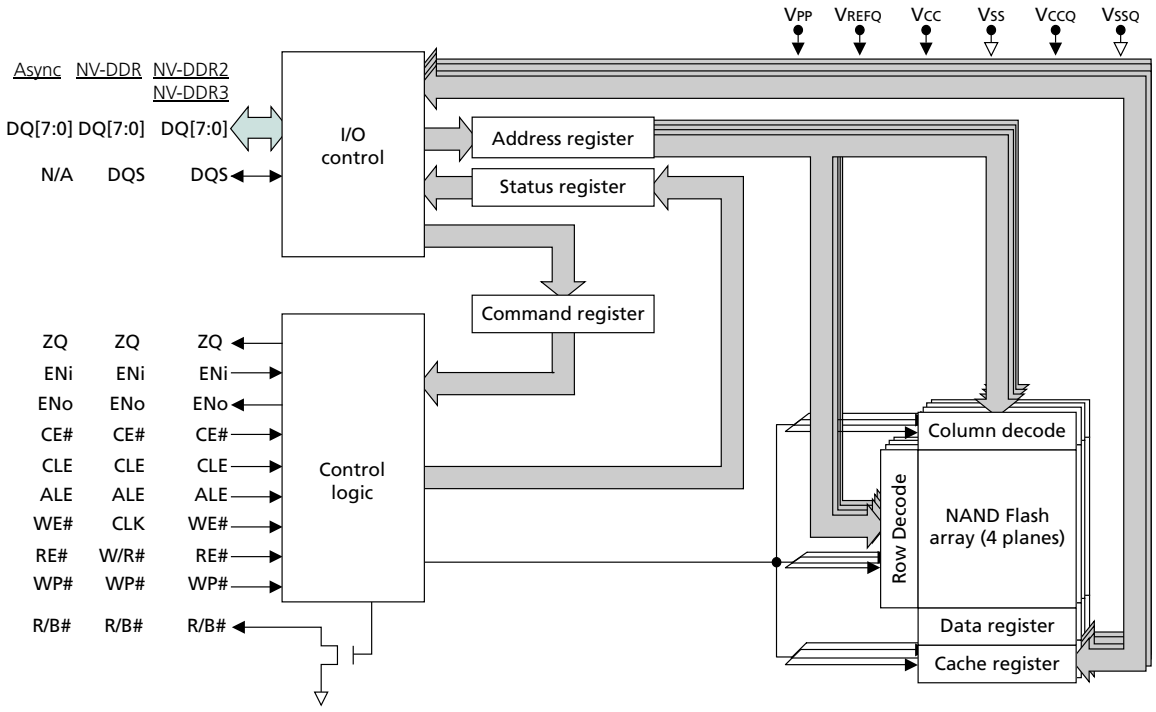
These devices use NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins and received by I/O control circuits. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations. The addresses are latched by an address register and sent to a row decoder to select a row address, or to a column decoder to select a column address.

Data is transferred to or from the NAND Flash memory array, byte by byte, through a data register and a cache register.

The NAND Flash memory array is programmed and read using page-based operations and is erased using block-based operations. During normal page operations, the data and cache registers act as a single register. During cache operations, the data and cache registers operate independently to increase data throughput.

The status register reports the status of die (LUN) operations.

Figure 6: NAND Flash Die (LUN) Functional Block Diagram



Notes:
1. N/A: This signal is tri-stated when the asynchronous interface is active.
2. Some devices may not include the NV-DDR, NV-DDR2, or NV-DDR3 interface.
3. Some devices do not include the V_{REFQ} or V_{PP} signal.

Device and Array Organization

Figure 7: Device Organization for Single-Die Package (132-ball BGA)

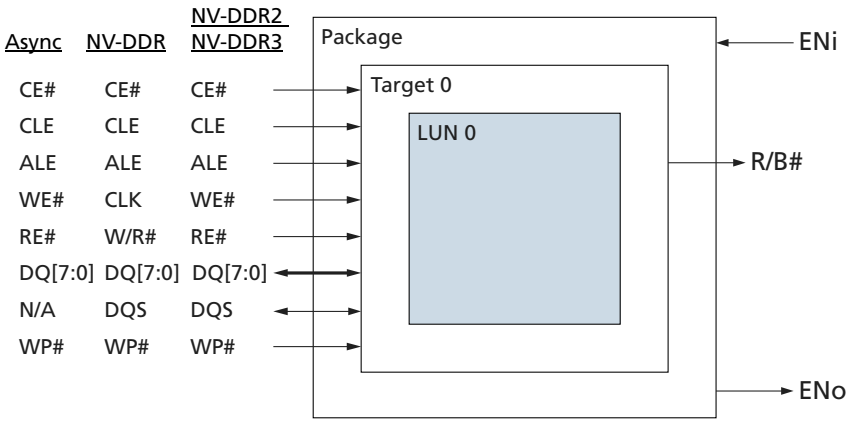


Figure 8: Device Organization for Two-Die Package (132-ball BGA)

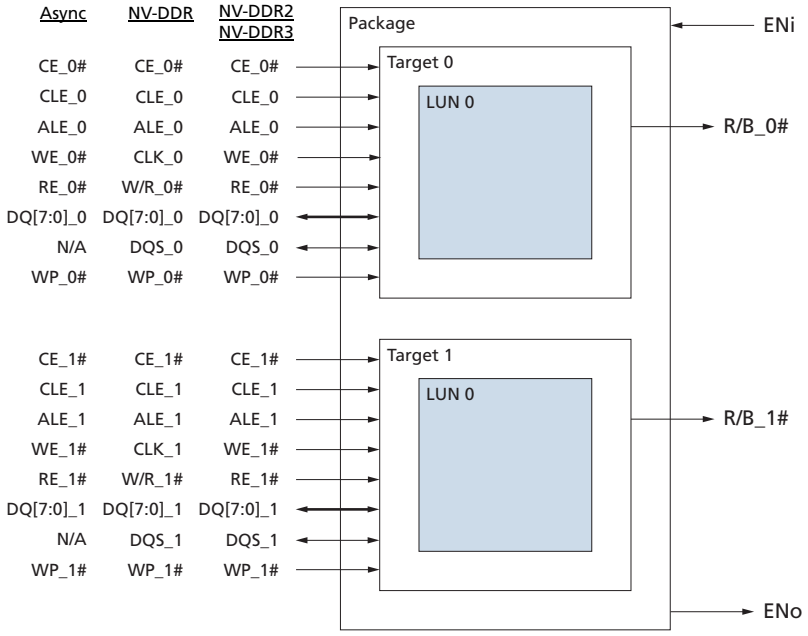


Figure 9: Device Organization for Four-Die Package with four CE# (132-ball BGA)

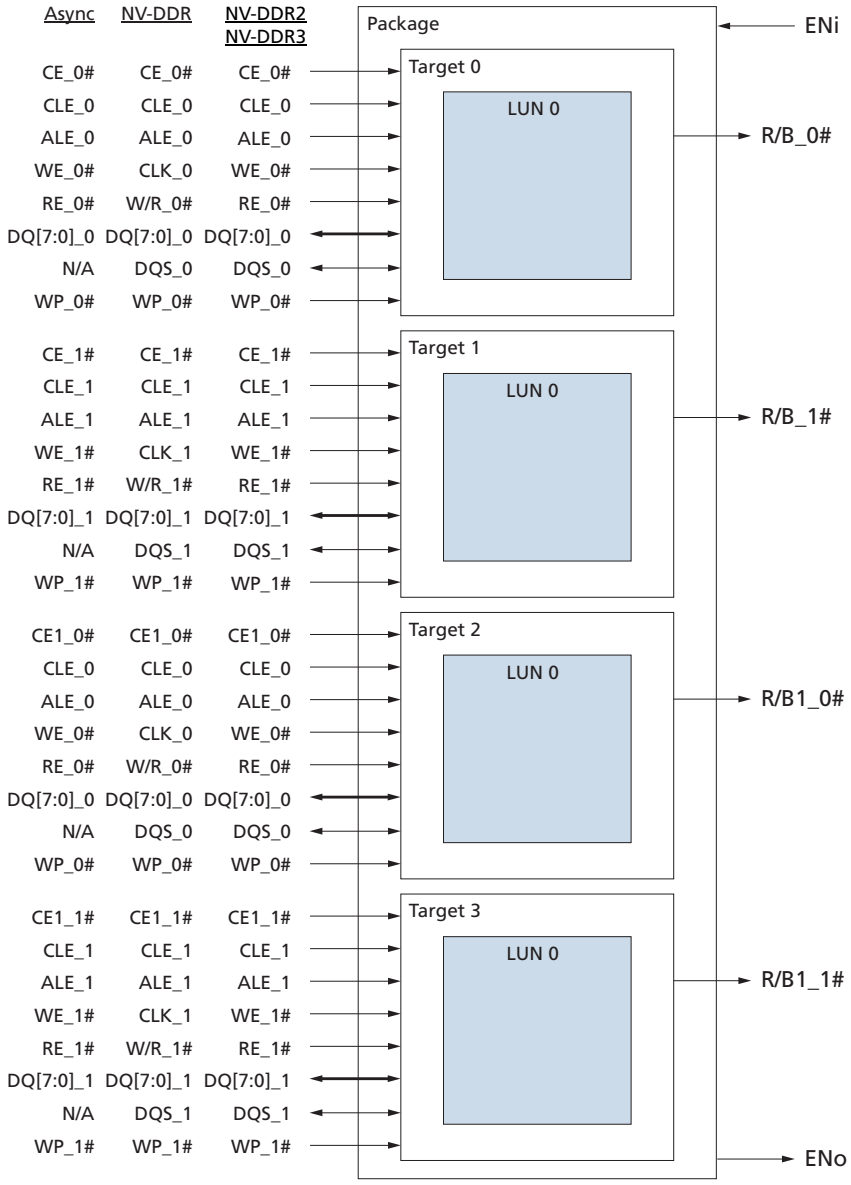


Figure 10: Device Organization for Eight-Die Package with four CE# (132-ball)

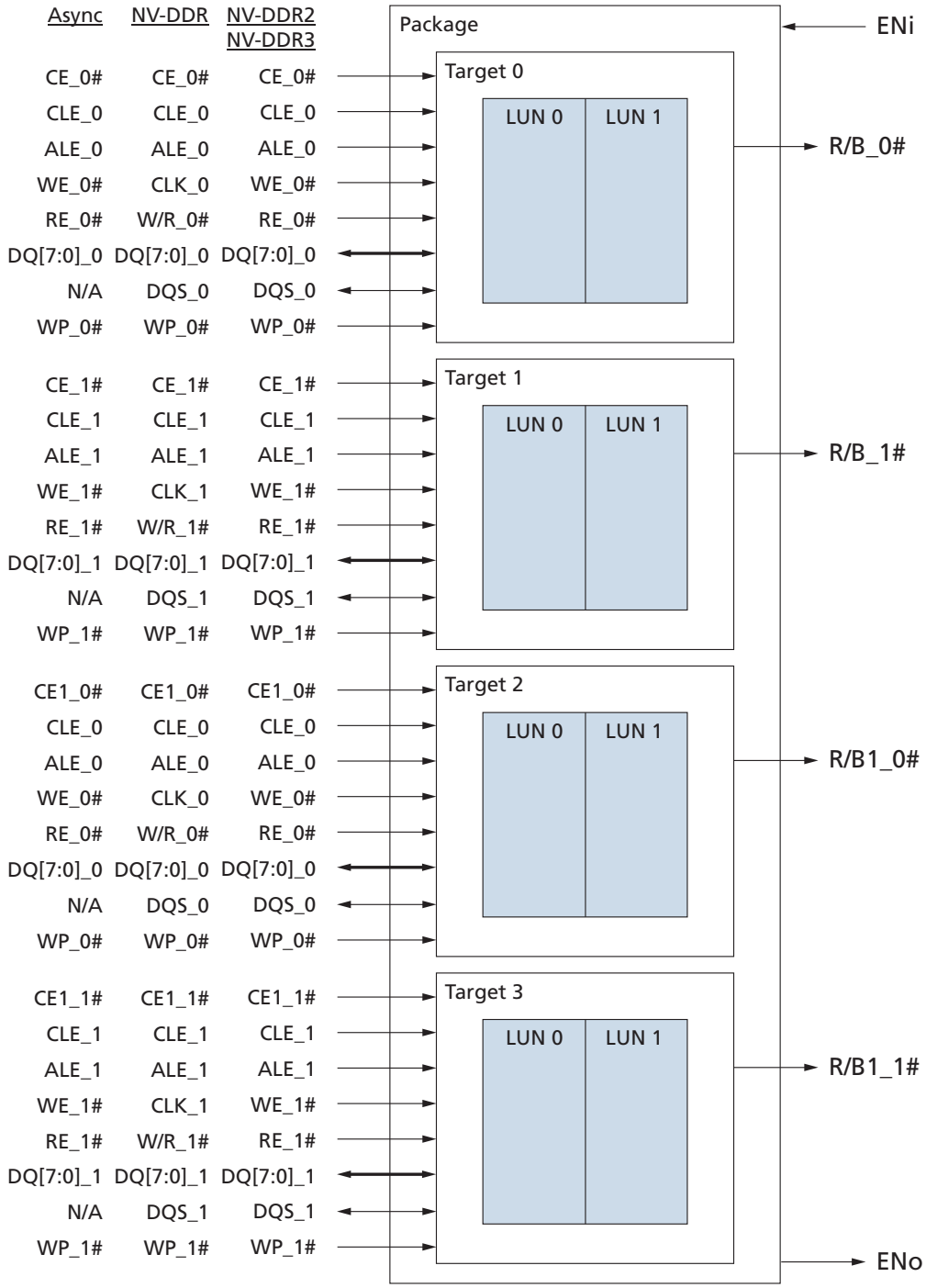


Figure 11: Device Organization for Sixteen-Die Package with eight CE# (132-ball BGA)

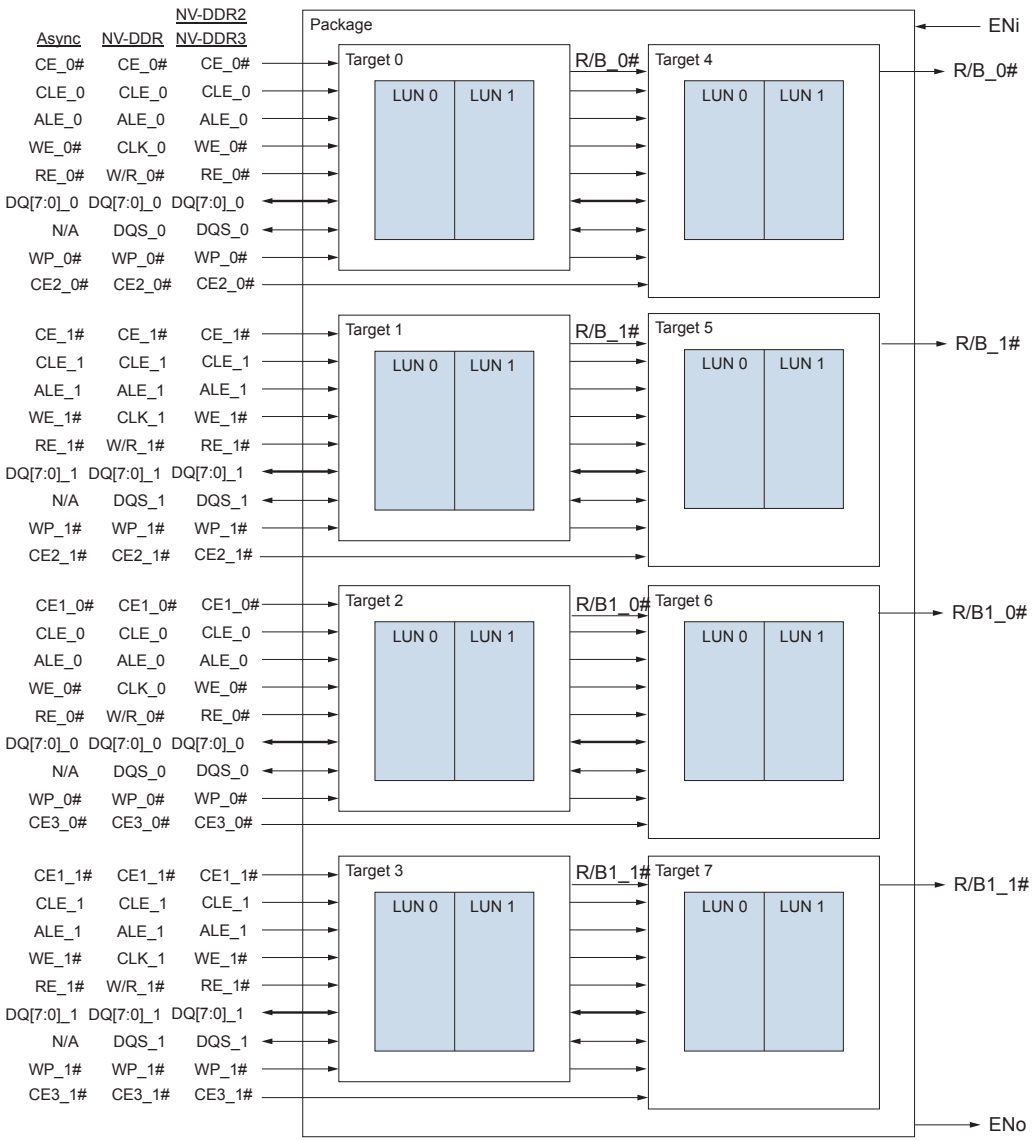


Figure 12: Array Organization per Logical Unit (LUN)

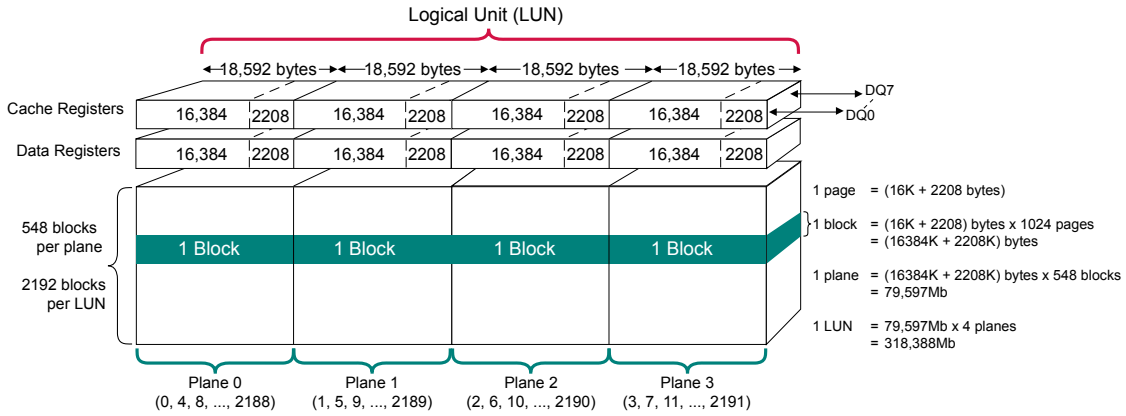


Table 2: Array Addressing for Logical Unit (LUN)

Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0[2]
Second	LOW	CA14[3]	CA13	CA12	CA11	CA10	CA9	CA8
Third	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11[4]	BA10[4]	PA9	PA8
Fifth	LOW	LA0[5]	BA21	BA20	BA19	BA18	BA17	BA16

Notes:

1. CAx = column address, PAx = page address, BAx = block address, LAx = LUN address; the page address, block address, and LUN address are collectively called the row address. Consequently, the first and second cycles containing the column addresses are known as C1 and C2, and the third, fourth, and fifth cycles containing the row addresses cycles are known as R1, R2, and R3 respectively.
2. When using the NV-DDR/NV-DDR2/NV-DDR3 interface, CA0 is forced to 0 internally; one data cycle always returns one even byte and one odd byte.
3. CA[14:0] address column addresses 0 through 18,591 (16,384 + 2208) (489Fh), therefore column addresses 18,592 (48A0h) through 32,767 (8FFFh) are invalid, out of bounds, do not exist in the device, and cannot be addressed.
4. BA[11] and BA[10] are the plane-select bits:
   Plane 0: BA[11] = 0, BA[10] = 0
   Plane 1: BA[11] = 0, BA[10] = 1
   Plane 2: BA[11] = 1, BA[10] = 0
   Plane 3: BA[11] = 1, BA[10] = 1
5. LA0 is the LUN-select bits. They are present only when two LUNs are shared on the target; otherwise, it should be held LOW.
   LUN 0: LA0 = 0
   LUN 1: LA0 = 1
6. For single LUN Targets block addresses 2192 through 4095 are invalid, out of bounds, do not exist in the device, and cannot be addressed.
   For two LUN Targets block addresses 2192 through 4095 and 6288 through 8191 are invalid, out of bounds, do not exist in the device, and cannot be addressed.

Bus Operation – Asynchronous Interface

The asynchronous interface is active when the NAND Flash device powers on within the 1.8V V_{CCQ} operational range. The I/O bus, DQ[7:0], is multiplexed sharing data I/O, addresses, and commands. The DQS signal, if present, is tri-stated when the asynchronous interface is active. If the NAND Flash device powers on within the 1.2V V_{CCQ} operational range, the NV-DDR3 interface is active, refer to the Bus Operations – NV-DDR3 Interface section for details.

Asynchronous interface bus modes are summarized below.

Table 3: Asynchronous Interface Mode Selection

Mode	CE#	CLE	ALE	WE#	RE#	DQS	DQx	WP#	Notes
Standby	H	X	X	X	X	X	X	0V/V_{CCQ}[2]	2
Bus idle	L	X	X	H	H	X	X	X	
Command input	L	H	L	↑	H	X	input	H	
Address input	L	L	H	↑	H	X	input	H	
Data input	L	L	L	↑	H	X	input	H	
Data output	L	L	L	H	↓	X	output	X	
Write protect	X	X	X	X	X	X	X	L	

Notes:
1. DQS is tri-stated when the asynchronous interface is active.
2. WP# should be biased to CMOS LOW or HIGH for standby.
3. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.

Asynchronous Enable/Standby

A chip enable (CE#) signal is used to enable or disable a target. When CE# is driven LOW, all of the signals for that target are enabled. With CE# LOW, the target can accept commands, addresses, and data I/O. There may be more than one target in a NAND Flash package. Each target is controlled by its own chip enable; the first target (Target 0) is controlled by CE#; the second target (if present) is controlled by CE2#, etc.

A target is disabled when CE# is driven HIGH, even when the target is busy. When disabled, all of the target's signals are disabled except CE#, WP#, and R/B#. This functionality is also known as CE# "Don't Care". While the target is disabled, other devices can utilize the disabled NAND signals that are shared with the NAND Flash.

A target enters low-power standby when it is disabled and is not busy. If the target is busy when it is disabled, the target enters standby after all of the die (LUNs) complete their operations. Standby helps reduce power consumption.

Asynchronous Bus Idle

A target's bus is idle when CE# is LOW, WE# is HIGH, and RE# is HIGH.

During bus idle, all of the signals are enabled except DQS, which is not used when the asynchronous interface is active. No commands, addresses, and data are latched into the target; no data is output.

Asynchronous Pausing Data Input/Output

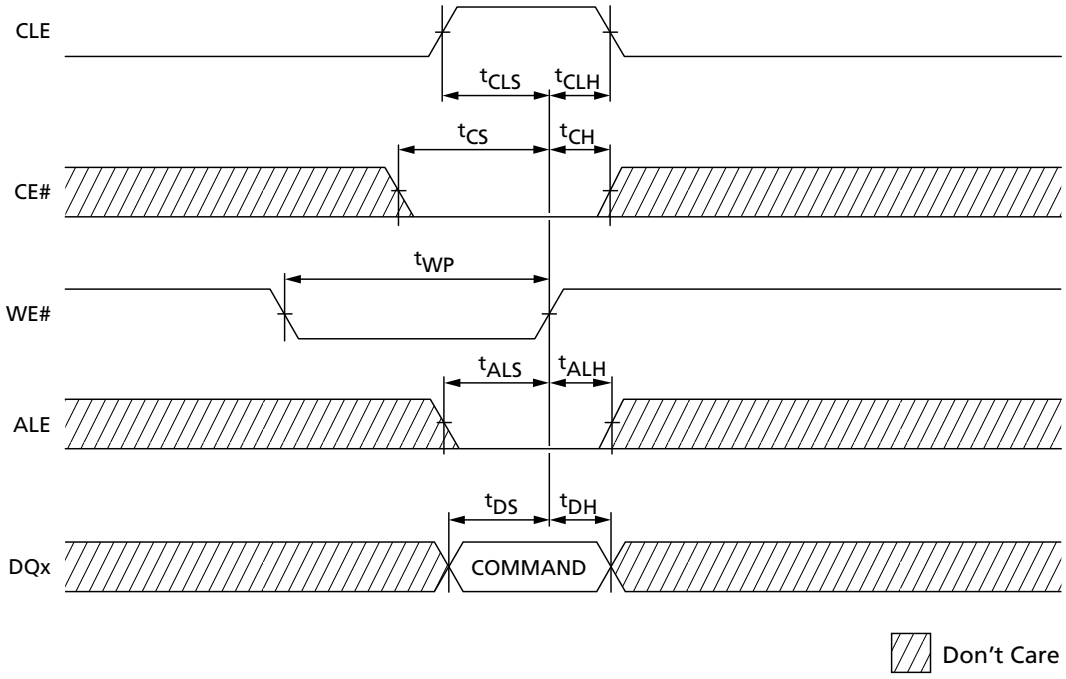
Pausing data input or data output is done by keeping WE# or RE# HIGH, respectively.

Asynchronous Commands

An asynchronous command is written from DQ[7:0] to the command register on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is HIGH, and RE# is HIGH.

Commands are typically ignored by die (LUNs) that are busy (RDY = 0); however, some commands, including READ STATUS (70h) and READ STATUS ENHANCED (78h), are accepted by die (LUNs) even when they are busy.

Figure 13: Asynchronous Command Latch Cycle



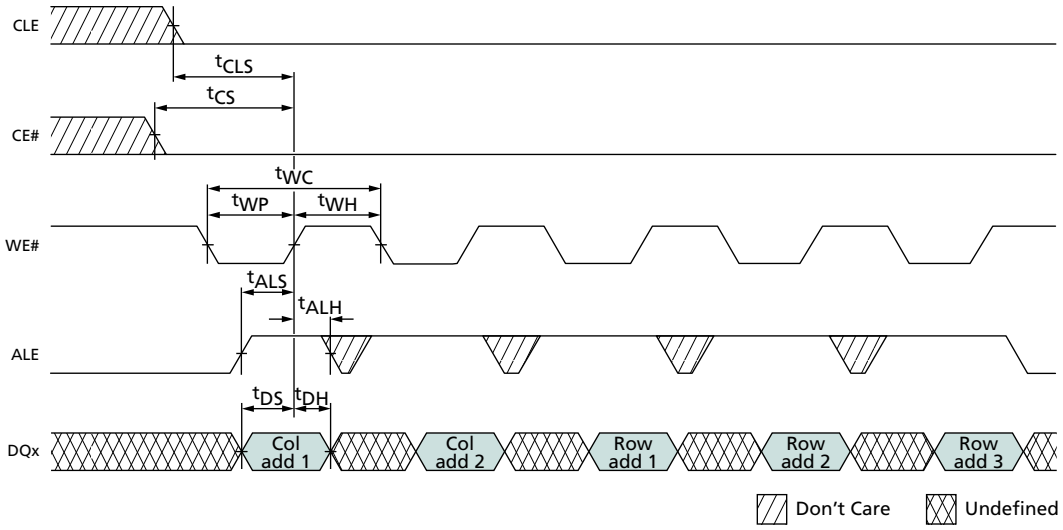
Asynchronous Addresses

An asynchronous address is written from DQ[7:0] to the address register on the rising edge of WE# when CE# is LOW, ALE is HIGH, CLE is LOW, and RE# is HIGH.

Bits that are not part of the address space must be LOW (see Device and Array Organization). The number of cycles required for each command varies. Refer to the command descriptions to determine addressing requirements (see Command Definitions).

Addresses are typically ignored by die (LUNs) that are busy (RDY = 0); however, some addresses are accepted by die (LUNs) even when they are busy; for example, address cycles that follow the READ STATUS ENHANCED (78h) command.

Figure 14: Asynchronous Address Latch Cycle

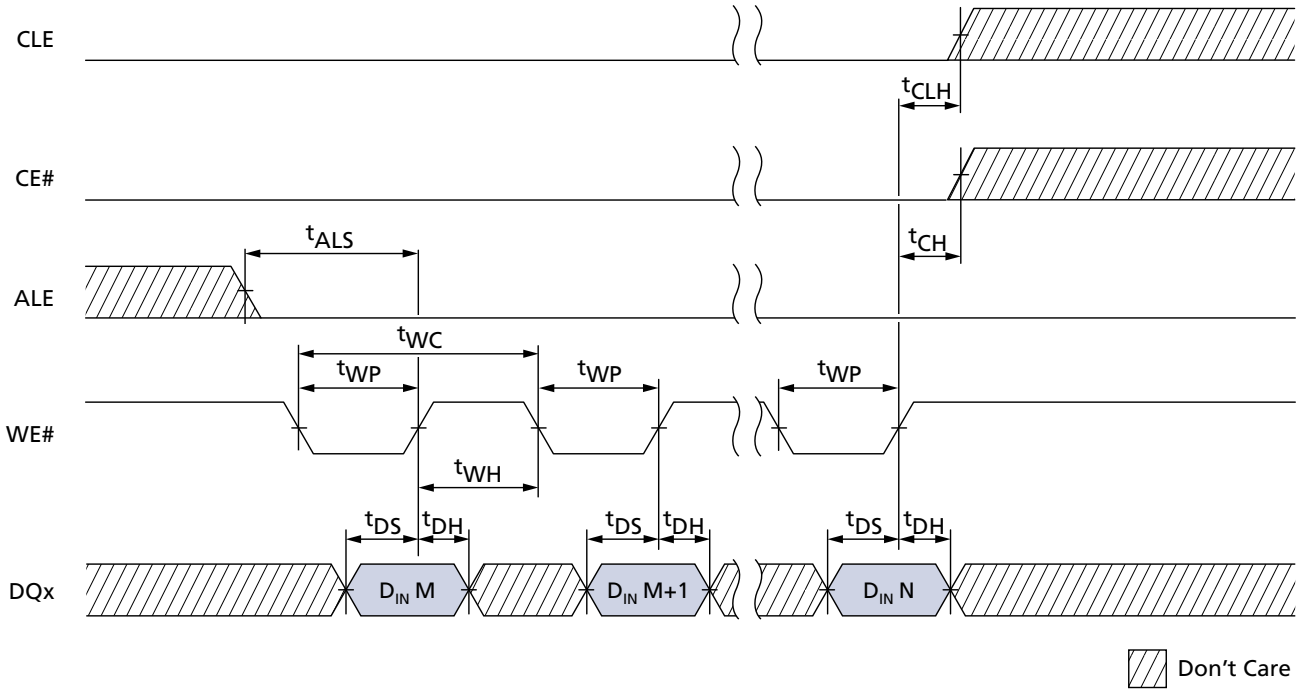


Asynchronous Data Input

Data is written from DQ[7:0] to the cache register of the selected die (LUN) on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is LOW, and RE# is HIGH.

Data input is ignored by die (LUNs) that are not selected or are busy (RDY = 0).

Figure 15: Asynchronous Data Input Cycles



Asynchronous Data Output

Data can be output from a die (LUN) if it is in a READY state. Data output is supported following a READ operation from the NAND Flash array. Data is output from the cache register of the selected die (LUN) to DQ[7:0] on the falling edge of RE# when CE# is LOW, ALE is LOW, CLE is LOW, and WE# is HIGH.

If the host controller is using a ^{t}RC of 30ns or greater, the host can latch the data on the rising edge of RE# (see Figure 16 for proper timing). If the host controller is using a ^{t}RC of less than 30ns, the host can latch the data on the next falling edge of RE# (see Figure 17 (page 32) for extended data output (EDO) timing).

Using the READ STATUS ENHANCED (78h) command prevents data contention following an interleaved die (multi-LUN) operation. After issuing the READ STATUS ENHANCED (78h) command, to enable data output, issue the READ MODE (00h) command.

Data output requests are typically ignored by a die (LUN) that is busy (RDY = 0); however, it is possible to output data from the status register even when a die (LUN) is busy by first issuing the READ STATUS (70h) or READ STATUS ENHANCED (78h) command.

Figure 16: Asynchronous Data Output Cycles

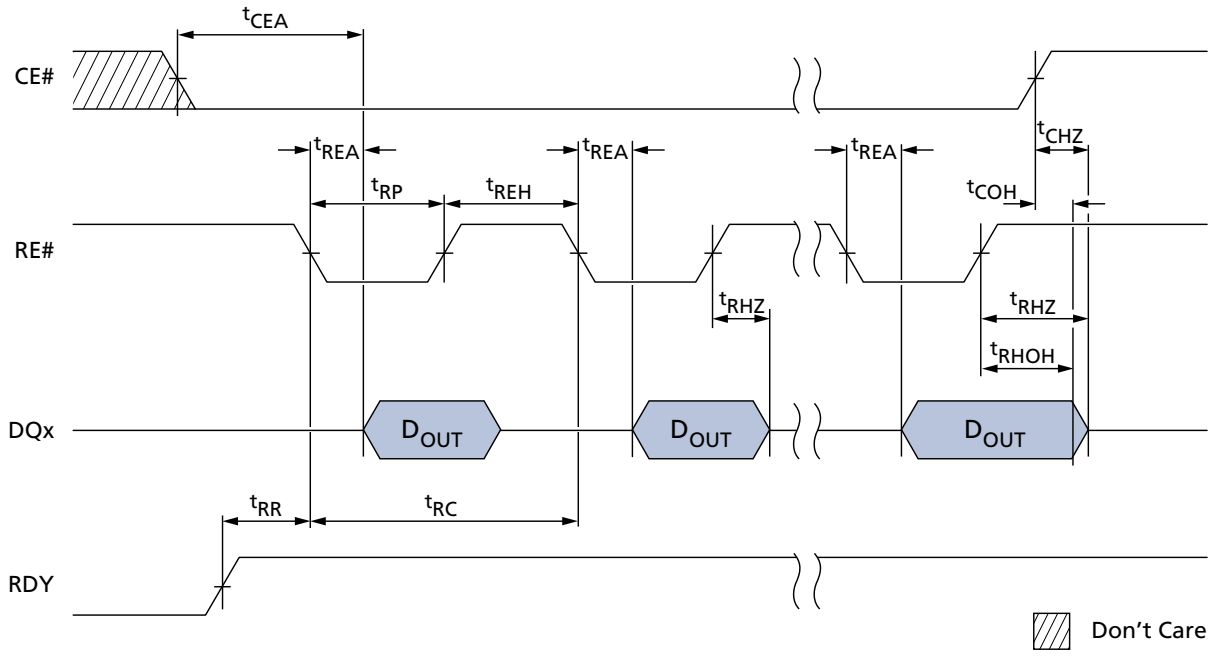
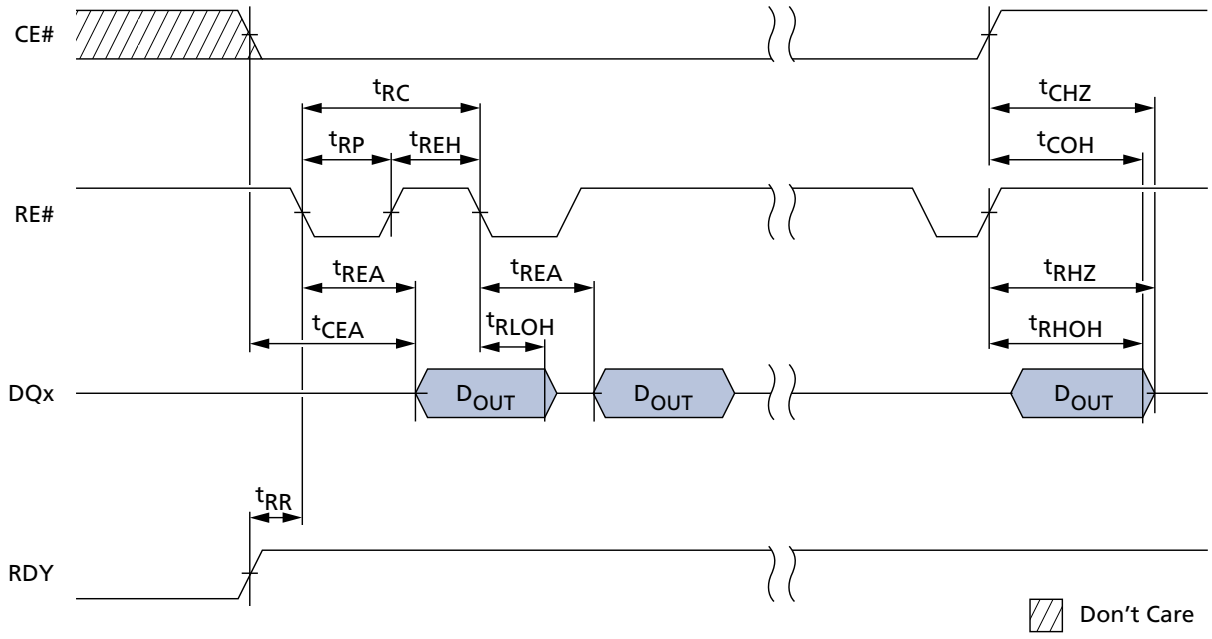


Figure 17: Asynchronous Data Output Cycles (EDO Mode)



Write Protect

The write protect# (WP#) signal enables or disables PROGRAM and ERASE operations to a target. When WP# is LOW, PROGRAM and ERASE operations are disabled. When WP# is HIGH, PROGRAM and ERASE operations are enabled.

It is recommended that the host drive WP# LOW during power-on until Vcc and Vccq are stable to prevent inadvertent PROGRAM and ERASE operations (see Device Initialization section for additional details).

WP# must be transitioned only when the target is not busy and prior to beginning a command sequence. After a command sequence is complete and the target is ready, WP# can be transitioned. After WP# is transitioned, the host must wait ^{t}WW before issuing a new command.

The WP# signal is always an active input, even when CE# is HIGH. This signal should not be multiplexed with other signals.

Ready/Busy#

The ready/busy# (R/B#) signal provides a hardware method of indicating whether a target is ready or busy. A target is busy when one or more of its die (LUNs) are busy (RDY = 0). A target is ready when all of its die (LUNs) are ready (RDY = 1). Because each die (LUN) contains a status register, it is possible to determine the independent status of each die (LUN) by polling its status register instead of using the R/B# signal (see Status Operations section for details regarding die (LUN) status).

This signal requires a pull-up resistor, Rp, for proper operation. R/B# is HIGH when the target is ready, and transitions LOW when the target is busy. The signal's open-drain

driver enables multiple R/B# outputs to be OR-tied. Typically, R/B# is connected to an interrupt pin on the system controller (see Figure 18 (page 33)).

It is not permitted to drive or have the NAND R/B# signal HIGH while the NAND V_{CCQ} voltage is below V_{CCQ} Min.

The combination of Rp and capacitive loading of the R/B# circuit determines the rise time of the R/B# signal. The actual value used for Rp depends on the system timing requirements. Large values of R_P cause R/B# to be delayed significantly. Between the 10- to 90-percent points on the R/B# waveform, the rise time is approximately two time constants (TC).

$$TC = R \times C$$

Where R = Rp (resistance of pull-up resistor), and C = total capacitive load.

The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# signal and the total load capacitance. Approximate Rp values using a circuit load of 100pF are provided in Figure 19 (page 34).

The minimum value for Rp is determined by the output drive capability of the R/B# signal, the output voltage swing, and V_{CCQ}.

$$Rp = \frac{Vccq\ (MAX) - Vol\ (MAX)}{IOL + \Sigma il}$$

Where Σil is the sum of the input currents of all devices tied to the R/B# pin.

Figure 18: READ/BUSY# Open Drain

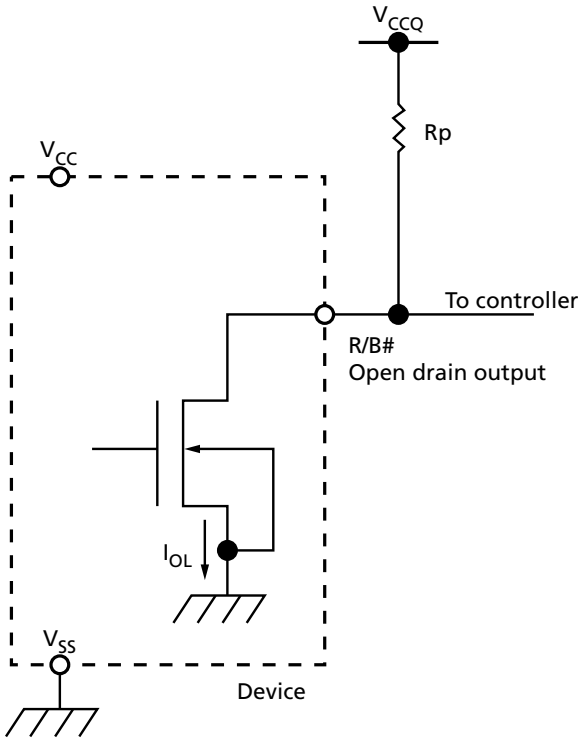
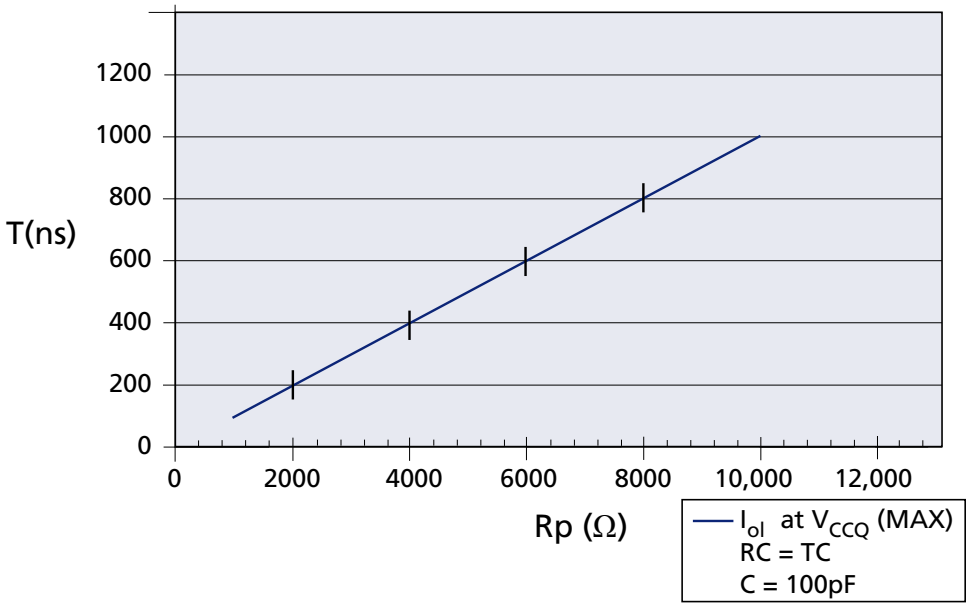


Figure 19: TC vs Rp



Bus Operation – NV-DDR Interface

The NAND Flash command protocol for both the asynchronous and NV-DDR interfaces is identical. However, there are some differences between the asynchronous and NV-DDR interfaces when issuing command, address, and data I/O cycles using the NAND Flash signals.

When the NV-DDR interface is activated on a target (see Activating Interfaces), the target is capable of high-speed NV-DDR data transfers. Existing signals are redefined for high-speed NV-DDR I/O. The WE# signal becomes CLK. DQS is enabled. The RE# signal becomes W/R#. CLK provides a clock reference to the NAND Flash device.

DQS is a bidirectional data strobe. During data output, DQS is driven by the NAND Flash device. During data input, DQS is controlled by the host controller while inputting data on DQ[7:0].

The direction of DQS and DQ[7:0] is controlled by the W/R# signal. When the W/R# signal is latched HIGH, the controller is driving the DQ bus and DQS. When the W/R# is latched LOW, the NAND Flash is driving the DQ bus and DQS.

Transition from the NV-DDR interface to the NV-DDR2 interface is not permitted.

The NV-DDR interface bus modes are summarized below.

Table 4: NV-DDR Interface Mode Selection

Mode	CE#	CLE	ALE	CLK	W/R#	DQS	DQ[7:0]	WP#	Notes
Standby	H	X	X	X	X	X	X	0V/V_{CCQ}	1, 2
Bus idle	L	L	L	↑	H	X	X	X	
Bus driving	L	L	L	↑	L	output	output	X	
Command input	L	H	L	↑	H	X	input	H	3
Address input	L	L	H	↑	H	X	input	H	3
Data input	L	H	H	↑↓	H	↑↓	input	H	4
Data output	L	H	H	↑↓	L	See Note 5	output	X	5
Write protect	X	X	X	X	X	X	X	L	
Undefined	L	L	H	↑	L	output	output	X	
Undefined	L	H	L	↑	L	output	output	X	

Notes:
1. CLK can be stopped when the target is disabled, even when R/B# is LOW.
2. WP# should be biased to CMOS LOW or HIGH for standby.
3. Commands and addresses are latched on the rising edge of CLK.
4. During data input to the device, DQS is the "clock" that latches the data in the cache register.

5. During data output from the NAND Flash device, DQS is an output generated from CLK after ^{t}DQSCK delay.
6. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.

NV-DDR Enable/Standby

In addition to the description found in Asynchronous Enable/Standby, the following requirements also apply when the NV-DDR interface is active.

Before enabling a target, CLK must be running and ALE and CLE must be LOW. When CE# is driven LOW, all of the signals for the selected target are enabled. The target is not enabled until ^{t}CS completes; the target's bus is then idle.

Prior to disabling a target, the target's bus must be idle. A target is disabled when CE# is driven HIGH, even when it is busy. All of the target's signals are disabled except CE#, WP#, and R/B#. After the target is disabled, CLK can be stopped.

A target enters low-power standby when it is disabled and is not busy. If the target is busy when it is disabled, the target enters standby after all of the die (LUNs) complete their operations.

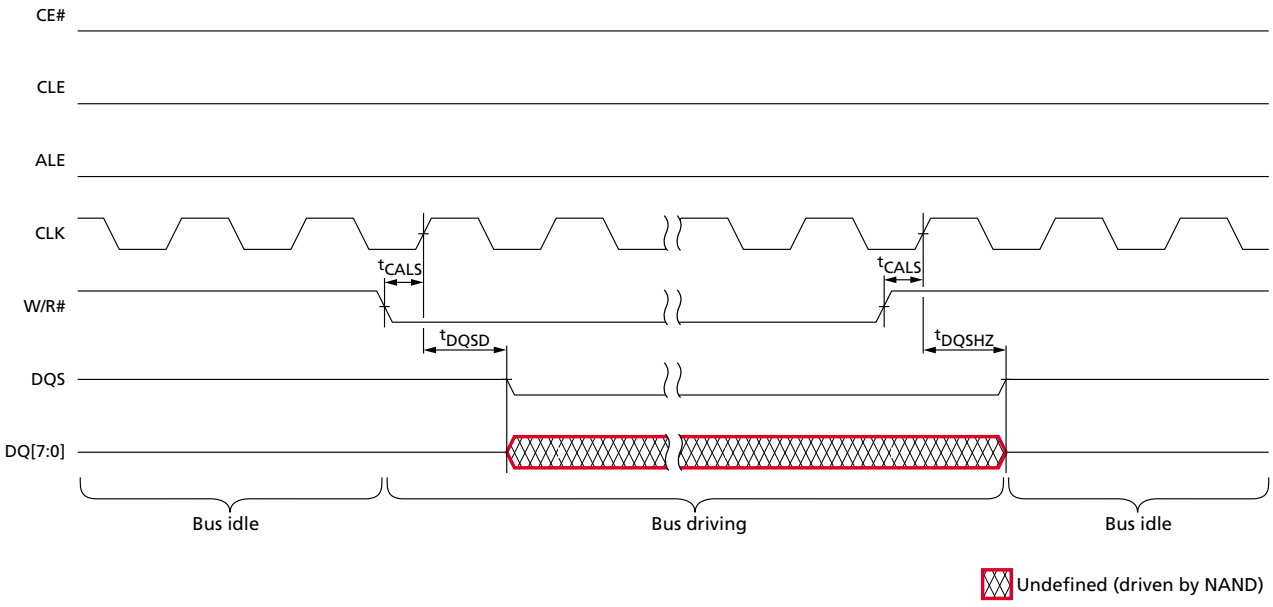
NV-DDR Bus Idle/Driving

A target's bus is idle or driving when CLK is running, CE# is LOW, ALE is LOW, and CLE is LOW.

The bus is idle when W/R# transitions HIGH and is latched by CLK. During the bus idle mode, all signals are enabled; DQS and DQ[7:0] are inputs. No commands, addresses, or data are latched into the target; no data is output. When entering the bus idle mode, the host must wait a minimum of ^{t}CAD before changing the bus mode. In the bus idle mode, the only valid bus modes supported are: bus driving, command, address, and NV-DDR data input.

The bus is driving when W/R# transitions LOW and is latched by CLK. During the bus driving mode, all signals are enabled; DQS is LOW and DQ[7:0] is driven LOW or HIGH, but no valid data is output. Following the bus driving mode, the only valid bus modes supported are bus idle and NV-DDR data output.

Figure 20: NV-DDR Bus Idle/Driving Behavior



Note: 1. Only the selected die (LUN) drives DQS and DQ[7:0]. During an interleaved die (multi-LUN) operation, the host must use the READ STATUS ENHANCED (78h) or FIXED ADDRESS READ STATUS ENHANCED (71h) to prevent data output contention.

NV-DDR Pausing Data Input/Output

Pausing data input or data output is done by setting ALE and CLE to LOW. The host may continue data transfer by setting ALE and CLE to HIGH after the applicable ^{t}CAD time has passed.

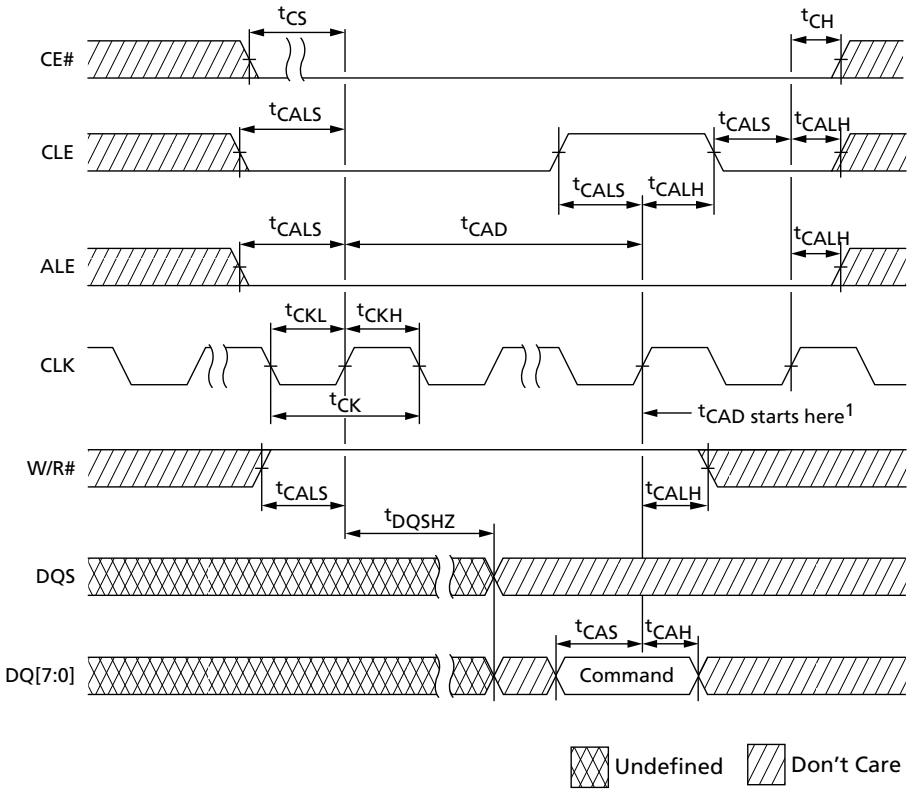
NV-DDR Commands

A command is written from DQ[7:0] to the command register on the rising edge of CLK when CE# is LOW, ALE is LOW, CLE is HIGH, and W/R# is HIGH.

After a command is latched—and prior to issuing the next command, address, or data I/O—the bus must go to bus idle mode on the next rising edge of CLK, except when the clock period, ^{t}CK, is greater than ^{t}CAD.

Commands are typically ignored by die (LUNs) that are busy (RDY = 0); however, some commands, such as READ STATUS (70h), READ STATUS ENHANCED (78h), and FIXED ADDRESS READ STATUS ENHANCED (71h), are accepted by die (LUNs) even when they are busy.

Figure 21: NV-DDR Command Cycle



Note: 1. When CE# remains LOW, tCAD begins at the rising edge of the clock from which the command cycle is latched for subsequent command, address, data input, or data output cycle(s).

NV-DDR Addresses

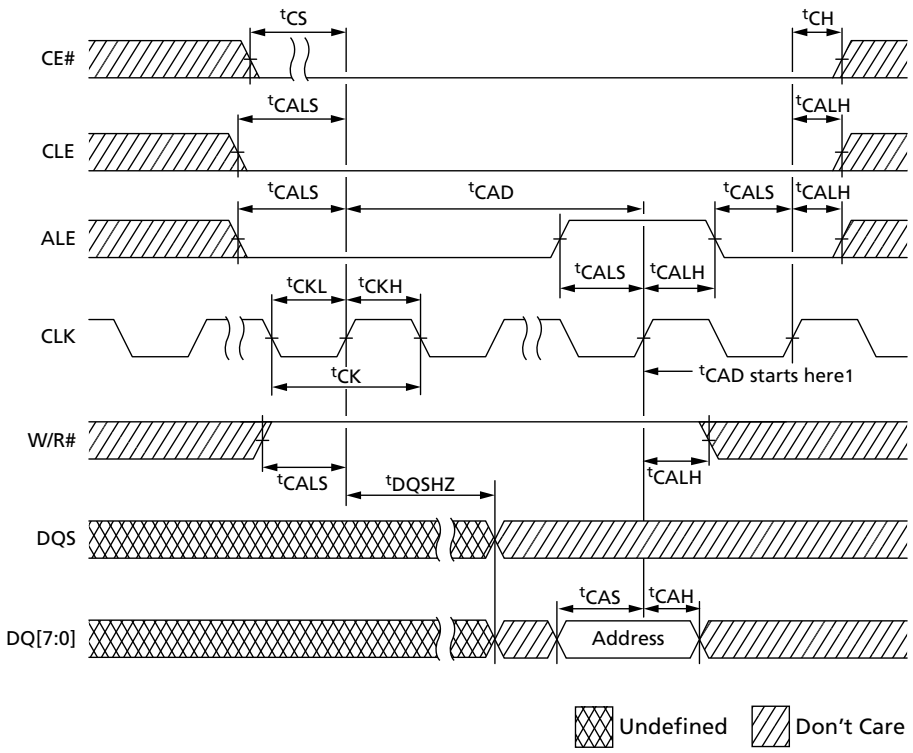
A NV-DDR address is written from DQ[7:0] to the address register on the rising edge of CLK when CE# is LOW, ALE is HIGH, CLE is LOW, and W/R# is HIGH.

After an address is latched—and prior to issuing the next command, address, or data I/O—the bus must go to bus idle mode on the next rising edge of CLK, except when the clock period, tCK, is greater than tCAD.

Bits not part of the address space must be LOW (see Device and Array Organization). The number of address cycles required for each command varies. Refer to the command descriptions to determine addressing requirements.

Addresses are typically ignored by die (LUNs) that are busy (RDY = 0); however, some addresses such as address cycles that follow the READ STATUS ENHANCED (78h) or FIXED ADDRESS READ STATUS ENHANCED (71h) commands, are accepted by die (LUNs) even when they are busy.

Figure 22: NV-DDR Address Cycle



Note: 1. When CE# remains LOW, tCAD begins at the rising edge of the clock from which the command cycle is latched for subsequent command, address, data input, or data output cycle(s).

NV-DDR DDR Data Input

To enter the NV-DDR data input mode, the following conditions must be met:

- CLK is running
- CE# is LOW
- W/R# is HIGH
- tCAD is met
- DQS is LOW
- ALE and CLE are HIGH on the rising edge of CLK

Upon entering the NV-DDR data input mode after tDQSS, data is written from DQ[7:0] to the cache register on each and every rising and falling edge of DQS (center-aligned) when CLK is running and the DQS to CLK skew meets tDSH and tDSS, CE# is LOW, W/R# is HIGH, and ALE and CLE are HIGH on the rising edge of CLK.

To exit NV-DDR data input mode, the following conditions must be met:

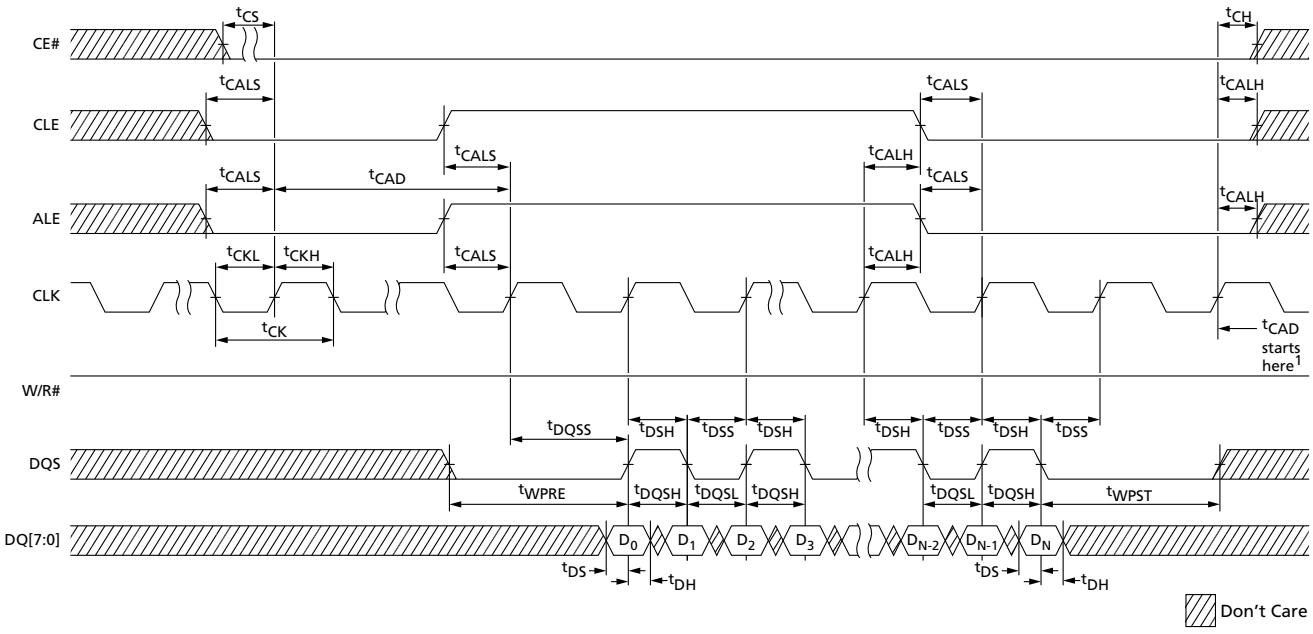
- CLK is running and the DQS to CLK skew meets tDSH and tDSS
- CE# is LOW
- W/R# is HIGH
- ALE and CLE are latched LOW on the rising edge of CLK

- The final two data bytes of the data input sequence are written to DQ[7:0] to the cache register on the rising and falling edges of DQS after the last cycle in the data input sequence in which ALE and CLE are latched HIGH.
- DQS is held LOW for tWPST (after the final falling edge of DQS)

Following tWPST, the bus enters bus idle mode and tCAD begins on the next rising edge of CLK. After tCAD starts, the host can disable the target if desired.

Data input is ignored by die (LUNs) that are not selected or are busy.

Figure 23: NV-DDR Data Input Cycles



Notes:
1. When CE# remains LOW, tCAD begins at the first rising edge of the clock after tWPST completes.
2. tDSH (MIN) generally occurs during tDQSS (MIN).
3. tDSS (MIN) generally occurs during tDQSS (MAX).

NV-DDR Data Output

Data can be output from a die (LUN) if it is ready. Data output is supported following a READ operation from the NAND Flash array.

To enter the NV-DDR data output mode, the following conditions must be met:

- CLK is running
- CE# is LOW
- The host has released the DQ[7:0] bus and DQS
- W/R# is latched LOW on the rising edge of CLK to enable the selected die (LUN) to take ownership of the DQ[7:0] bus and DQS within tWRCK
- tCAD is met
- ALE and CLE are HIGH on the rising edge of CLK

Upon entering the NV-DDR data output mode, DQS will toggle HIGH and LOW with a delay of ^{t}DQSCK from the respective rising and falling edges of CLK. DQ[7:0] will output data edge-aligned to the rising and falling edges of DQS, with the first transition delayed by no more than ^{t}AC.

NV-DDR data output mode continues as long as CLK is running, CE# is LOW, W/R# is LOW, and ALE and CLE are HIGH on the rising edge of CLK.

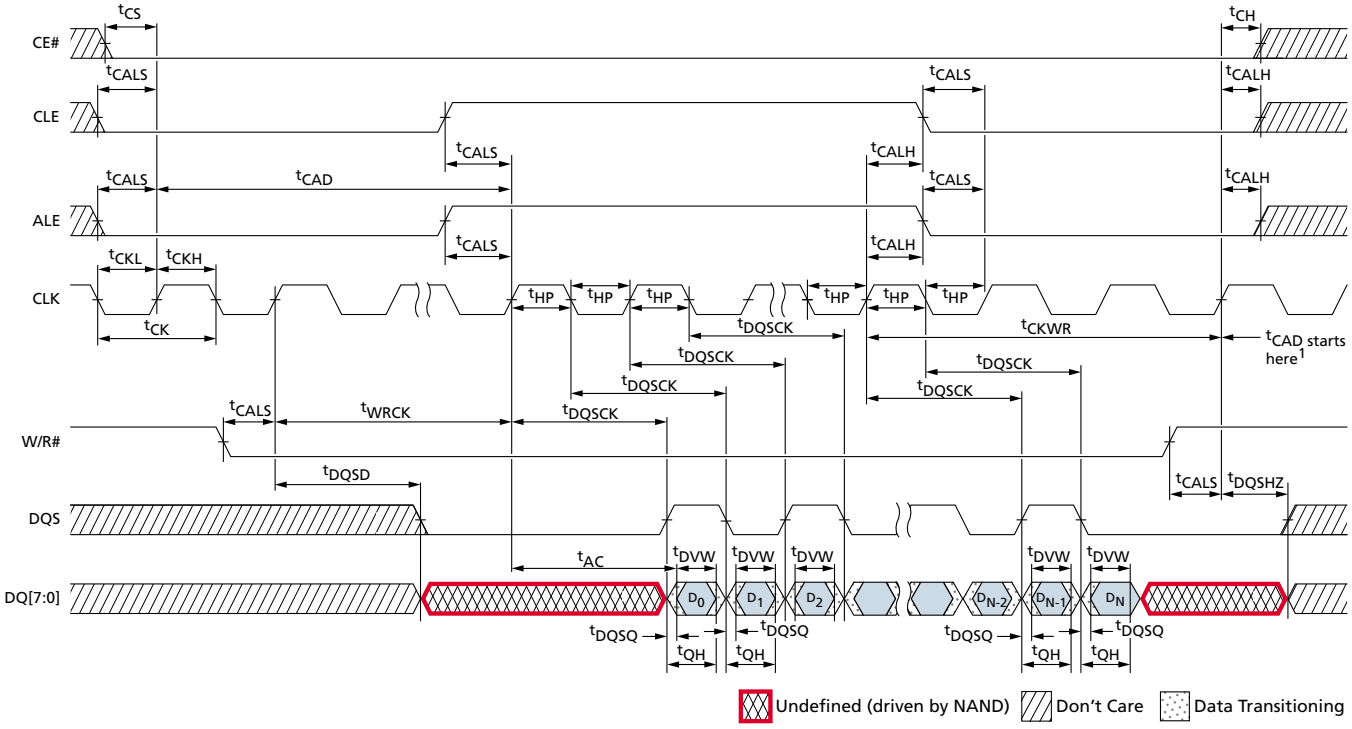
To exit NV-DDR data output mode, the following conditions must be met:

- CLK is running
- CE# is LOW
- W/R# is LOW
- ALE and CLE are latched LOW on the rising edge of CLK

The final two data bytes are output on DQ[7:0] on the final rising and falling edges of DQS. The final rising and falling edges of DQS occur ^{t}DQSCK after the last cycle in the data output sequence in which ALE and CLE are latched HIGH. After ^{t}CKWR, the bus enters bus idle mode and ^{t}CAD begins on the next rising edge of CLK. Once ^{t}CAD starts the host can disable the target if desired.

Data output requests are typically ignored by a die (LUN) that is busy (RDY = 0); however, it is possible to output data from the status register even when a die (LUN) is busy by issuing the READ STATUS (70h), READ STATUS ENHANCED (78h), or FIXED ADDRESS READ STATUS ENHANCED (71h) command.

Figure 24: NV-DDR Data Output Cycles



Notes:
1. When CE# remains LOW, tCAD begins at the rising edge of the clock after tCKWR for subsequent command or data output cycle(s).
2. See Figure 21 (page 38) for details of W/R# behavior.
3. tAC is the DQ output window relative to CLK and is the long-term component of DQ skew.
4. For W/R# transitioning HIGH, DQ[7:0] and DQS go to tri-state.
5. For W/R# transitioning LOW, DQ[7:0] drives current state and DQS goes LOW.
6. After final data output, DQ[7:0] is driven until W/R# goes HIGH, but is not valid.

Write Protect

See Write Protect under Bus Operations - Asynchronous Interface.

Ready/Busy#

See Ready/Busy# under Bus Operations - Asynchronous Interface.

Bus Operation – NV-DDR2 Interface

When the NV-DDR2 interface is activated on a target (see Activating Interfaces), the target is capable of high-speed DDR data transfers and the DQS signal is enabled. DQS is a bidirectional data strobe. During data output, DQS is driven by the NAND Flash device. During data input, DQS is controlled by the host controller while inputting data on DQ[7:0].

For operations in NV-DDR2 mode, the NV-DDR2 interface must be selected (see Activating Interfaces (page 72)). The capabilities that NV-DDR2 operations offers beyond NV-DDR operations include:

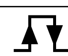
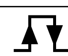
- Supported only at 1.8V V_{CCQ}
- Support for speeds beyond 200MT/s
- Support for differential signaling for the RE# and/or DQS signals (RE_c, DQS_c)
- Support for Warmup Cycles
- Support for On-die Termination (ODT)
- Support for V_{REFQ}

Use of differential signaling and external V_{REFQ} are optional, but are required to guarantee specified AC timings for speeds faster than 200MT/s. If not using the differential signaling, statements about those signal types can be ignored.

Transition from the NV-DDR2 interface to the NV-DDR interface is not permitted.

The NV-DDR2 interface bus modes are summarized below:

Table 5: NV-DDR2 Interface Mode Selection

Mode	CE#	CLE	ALE	RE# (RE_t)	DQS (DQS_t)	DQ[7:0][1]	WE#	WP#	Notes
Standby	H	X	X	X	X	X	X	0V/V_{CCQ}	1, 2
Idle	L	L	L	H	H	X	H	X	6
Command input	L	H	L	H	X	input		H	3
Address input	L	L	H	H	X [4]	input		H	3
Data input	L	L	L	H		input	H	H	2, 3
Data output	L	L	L			output	H	X	2, 3, 5
Write protect	X	X	X	X	X	X	X	L	

Notes:
1. The current state of the device is data input, data output, or neither based on the commands issued.
2. There are two data input/output cycles from the rising edge of DQS/RE# to the next rising edge of DQS/RE#.
3. ODT may be enabled as part of the data input and data output cycles.
4. When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

5. At the beginning of a data output burst, DQS shall be held HIGH for ^{t}DQSRH after RE# transitions LOW to begin data output. ^{t}DQSRH is only required if Matrix ODT is enabled.
6. WE# is set HIGH during the Idle state.
7. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.

Differential Signaling

An enabler for higher speed operation is differential signaling for the RE# and DQS signals. A complementary RE# and complementary DQS signal may be optionally used to create differential signal pairs (RE_t/RE_c and DQS_t/DQS_c). When using differential signaling, RE# is referred to as RE_t and DQS is referred to as DQS_t, i.e., the "true" versions of the signals. Differential signaling may be used to improve signal integrity through enhanced noise immunity. Differential signaling shall only be enabled for use when the NV-DDR2 data interface is selected.

A device may support differential RE# and/or differential DQS signaling. The support for differential RE# and/or DQS is reported in the parameter page. Complementary RE# (i.e., RE_c) and complementary DQS (i.e., DQS_c) signals are individually configured/enabled. By default, differential signaling is disabled. The host may configure the device to use differential signaling using the NV-DDR2 Configuration feature address.

Differential signaling is not enabled by default. It is recommended that if differential signaling is used by a host system that is it enabled at the same time as the interface utilizing the differential signaling is enabled.

To begin using differential signaling, the host shall issue a SET FEATURES (EFh) command to the Timing Mode feature address that sets the Data Interface from asynchronous to NV-DDR2 operation. Then issue a SET FEATURES (EFh) command to the NV-DDR2 Configuration feature address to activate differential RE# and/or differential DQS signaling. The differential signaling is then enabled after CE# is brought HIGH.

To change from differential signaling to single-ended signaling, the host shall configure the device using the NV-DDR2 Configuration feature address to disable differential signaling. The differential signaling is disabled after CE# is brought HIGH.

A RESET (FFh) command will disable differential signaling. The SYNCHRONOUS RESET (FCh) and RESET LUN (FAh) commands have no effect on differential signaling.

Warmup Cycles

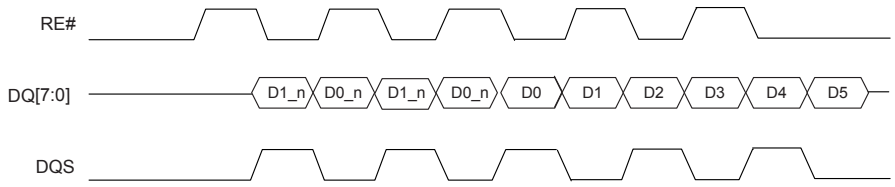
In order to support higher speed operation, warmup cycles for data output and data input may be provided. Warmup cycles shall only be enabled for use when the NV-DDR2 data interface is selected.

Warmup cycles for data output provides extra RE# and corresponding DQS transitions at the beginning of a data output burst. These extra RE#/DQS transitions do not have any data associated with them. The number of extra cycles is configured via the NV-DDR2 configuration feature address.

Warmup cycles for data input provides extra DQS transitions at the beginning of a data input burst. These extra DQS transitions do not have any data associated with them. The number of extra cycles is configured via the NV-DDR2 Configuration feature address. The number of cycles specified includes a full data input cycle (both rising and falling edge for DQS).

Warmup cycles are optional for both data output and data input, and if used, do not need to be configured to the same value. Warmup cycles apply to all commands. Warm-up cycles are initiated at the start of each data burst when warmup cycles are enabled for that data transfer type. If the host pauses and then resumes a data transfer without exiting and re-entering the data burst, then the host shall not issue additional warmup cycles. Exiting and re-entering the data burst shall be performed by bringing ALE, CLE, or CE# HIGH without latching with WE#. In the case of not re-issuing warmup cycles, the host should take care to avoid signal integrity issues due to pausing the data transfer and resuming without warmup cycles.

Figure 25: Warmup Cycles for data output (2 warmup cycles)



On-die Termination (ODT)

On-die termination may be required at higher speeds depending on system topology. On-die termination applies to the DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c signals. On-die termination is an optional capability that may be employed to meet higher speeds in particular topologies. On-die termination can improve signal quality by reducing signal reflection through internal termination resistance adjustment. If power needs to be optimized in a particular condition, then on-die termination may be disabled and the topology may be run at a slower timing mode. On-die termination shall only be enabled for use in the NV-DDR2 data interface.

On-die termination settings are configured during device initialization. The host may configure the ODT in a self-termination only configuration, or matrix termination which enables a combination of Target and non-Target termination to be specified.

For the more flexible matrix termination the host configures a matrix that defines the LUN(s) that terminate for a particular Volume. This matrix is configured using the ODT CONFIGURE (E2h) command. After the on-die termination matrix is defined, ODT is enabled and disabled based on the type of cycle (on for data input and output cycles, off for command, and address cycles). On-die termination applies for data input and output cycles for all command types, including both single data rate (SDR) and double data rate (DDR) transfers.

Volume addressing is required for use of non-Target on-die termination (ODT) functionality. See Configuration Operations for how to appoint Volume addresses. Once volume addresses have been appointed they can be selected with the VOLUME SELECT (E1h) command. For Target only termination, no ODT termination matrix is required.

The on-die termination configuration matrix and control mechanism utilize Volume addresses. Volume addressing is a required capability to utilize non-Target on-die termination.

The on-die termination settings are retained across RESET (FAh, FCh, FFh) commands, but are not retained across HARD RESET (FDh) commands for the target LUN.

When on-die termination is enabled via the NV-DDR2 Configuration feature address, the default is Target termination. For non-Target termination or termination topologies that use multiple terminators, the Volume address mechanism shall be used and the on-die termination configuration matrix shall be specified using the ODT CONFIGURE (E2h) command. As part of the ODT CONFIGURE (E2h) command, R_{TT} settings may be specified on a per LUN basis with individual values for:

- RE#
- DQ[7:0] and DQS for data output
- DQ[7:0] and DQS for data input

Table 6: On-die Termination DC Electrical Characteristics without ZQ Calibration

Mode	Symbol	Min	Typ	Max	Units	Notes
R_{TT} effective impedance value for 50 Ohm setting	$R_{TT2(EFF)}$	32.5	50	67.5	Ohms	1
R_{TT} effective impedance value for 75 Ohm setting	$R_{TT3(EFF)}$	48.7	75	101.3	Ohms	1
R_{TT} effective impedance value for 100 Ohm setting	$R_{TT4(EFF)}$	65	100	135	Ohms	1
R_{TT} effective impedance value for 150 Ohm setting	$R_{TT5(EFF)}$	97.5	150	202.5	Ohms	1
Deviation of VM with respect to V_{CCQ} / 2	ΔVM	-7	-	7	Percent	2

Notes:
1. $R_{TT2\ (EFF)}$, $R_{TT3\ (EFF)}$, $R_{TT4\ (EFF)}$, and $R_{TT5\ (EFF)}$ are determined by separately applying $V_{IH(AC)}$ and $V_{IL(AC)}$ to the signal being tested, and then measuring current $I(V_{IH[AC]})$ and $I(V_{IL[AC]})$, respectively. $R_{TT(EFF)} = (V_{IH[AC]} - V_{IL[AC]}) / (I(V_{IH[AC]}) - I(V_{IL[AC]})$
2. Measure voltage (VM) at the tested signal with no load. $\Delta VM = [(2 \times VM) / V_{CCQ} - 1] \times 100$.

Table 7: On-die Termination DC Electrical Characteristics with ZQ Calibration

Mode	Symbol	Min	Typ	Max	Units	Notes
R_{TT} effective impedance value	$R_{TT(EFF)}$	See on page				on page

Table 7: On-die Termination DC Electrical Characteristics with ZQ Calibration (Continued)

Mode	Symbol	Min	Typ	Max	Units	Notes
Deviation of VM with respect to V_{CCQ} / 2	ΔVM	-7	-	7	Percent	on page

Notes:
1. $R_{TT\ (EFF)}$ is determined by separately applying $V_{IH(AC)}$ and $V_{IL(AC)}$ to the signal being tested, and then measuring current $I(V_{IH[AC]})$ and $I(V_{IL[AC]})$, respectively. $R_{TT(EFF)} = (V_{IH[AC]} - V_{IL[AC]}) / (I(V_{IH[AC]}) - I(V_{IL[AC]})$
2. Measure voltage (VM) at the tested signal with no load. $\Delta VM = [(2 \times VM) / V_{CCQ} - 1] \times 100$.

Table 8: $R_{TT(EFF)}$ Impedance Values with ZQ Calibration

R_{TT}	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
50 Ohms	Rpd	$V_{CCQ} \times 0.2$	0.57	1	1.15	RZQ/3
		$V_{CCQ} \times 0.5$	0.85	1	1.15	RZQ/3
		$V_{CCQ} \times 0.8$	0.85	1	1.47	RZQ/3
	Rpu	$V_{CCQ} \times 0.2$	0.85	1	1.47	RZQ/3
		$V_{CCQ} \times 0.5$	0.85	1	1.15	RZQ/3
		$V_{CCQ} \times 0.8$	0.57	1	1.15	RZQ/3
50 Ohms		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.85	1	1.67	RZQ/6
75 Ohms	Rpd	$V_{CCQ} \times 0.2$	0.57	1	1.15	RZQ/2
		$V_{CCQ} \times 0.5$	0.85	1	1.15	RZQ/2
		$V_{CCQ} \times 0.8$	0.85	1	1.47	RZQ/2
	Rpu	$V_{CCQ} \times 0.2$	0.85	1	1.47	RZQ/2
		$V_{CCQ} \times 0.5$	0.85	1	1.15	RZQ/2
		$V_{CCQ} \times 0.8$	0.57	1	1.15	RZQ/2
75 Ohms		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.85	1	1.67	RZQ/4
100 Ohms	Rpd	$V_{CCQ} \times 0.2$	0.57	1	1.15	RZQ/1.5
		$V_{CCQ} \times 0.5$	0.85	1	1.15	RZQ/1.5
		$V_{CCQ} \times 0.8$	0.85	1	1.47	RZQ/1.5
	Rpu	$V_{CCQ} \times 0.2$	0.85	1	1.47	RZQ/1.5
		$V_{CCQ} \times 0.5$	0.85	1	1.15	RZQ/1.5
		$V_{CCQ} \times 0.8$	0.57	1	1.15	RZQ/1.5
100 Ohms		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.85	1	1.67	RZQ/3
150 Ohms	Rpd	$V_{CCQ} \times 0.2$	0.57	1	1.15	RZQ/1
		$V_{CCQ} \times 0.5$	0.85	1	1.15	RZQ/1
		$V_{CCQ} \times 0.8$	0.85	1	1.47	RZQ/1
	Rpu	$V_{CCQ} \times 0.2$	0.85	1	1.47	RZQ/1
		$V_{CCQ} \times 0.5$	0.85	1	1.15	RZQ/1
		$V_{CCQ} \times 0.8$	0.57	1	1.15	RZQ/1

Table 8: $R_{TT(EFF)}$ Impedance Values with ZQ Calibration (Continued)

R_{TT}	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
150 Ohms		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.85	1	1.67	RZQ/2

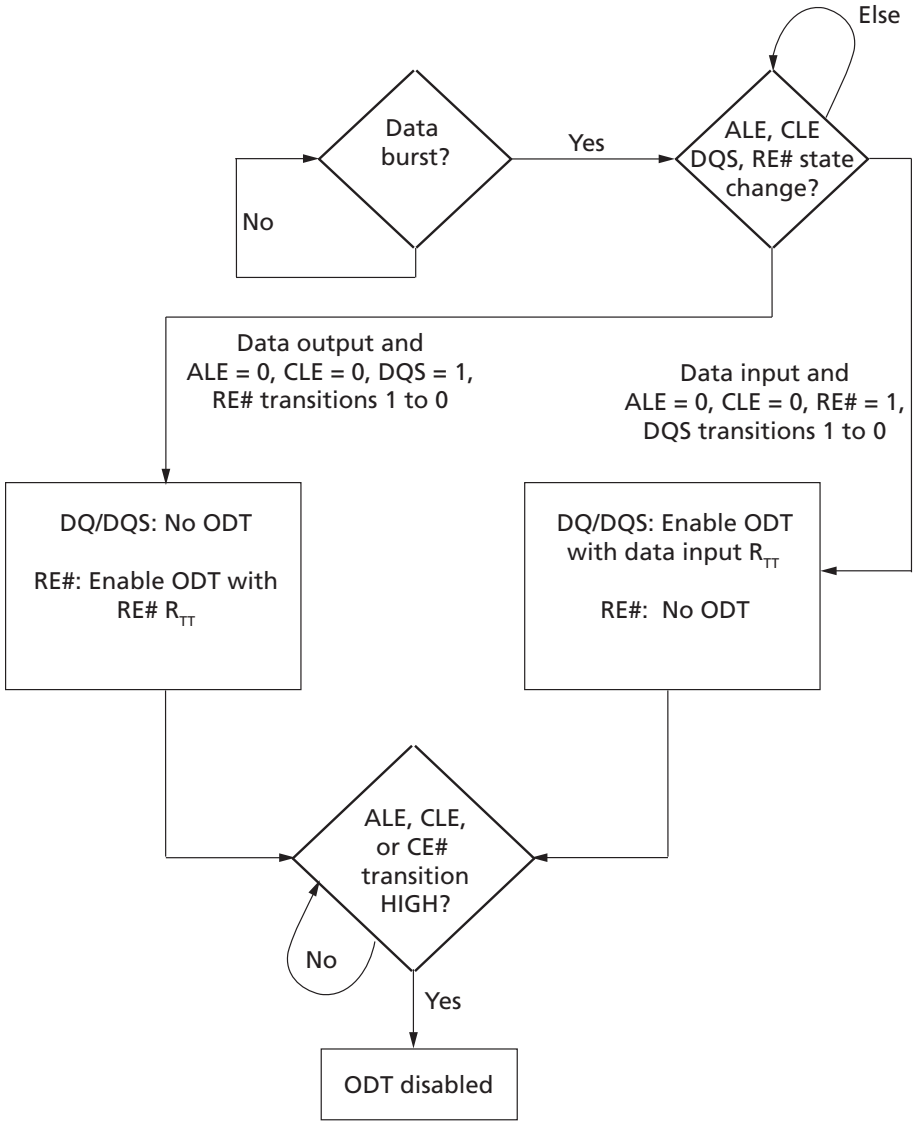
Notes:
1. Tolerance limits assume R_{ZQ} of 300 ohms +/- 1% and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage.
2. Refer to Output Driver Sensitivity if either the temperature or the voltage changes after calibration.
3. The minimum values are derated by 6% when the device operates between -40°C and 0°C.

Self-termination On-die Termination (ODT)

When self-termination is enabled, the LUN that is executing the command provides on-die termination. Figure 26 (page 49) defines the self-termination only ODT enable and disable requirements for the LUN that is executing the command when ODT is selected for use via SET FEATURES (EFh) command. If the ODT CONFIGURE (E2h) command is issued to a LUN on a Target, then the ODT mechanism used for that Target changes to matrix termination.

Self-termination is applied to DQS and DQ[7:0] signals during data input operations and RE# during data output operations.

Figure 26: Self-termination only ODT behavioral flow



Matrix Termination

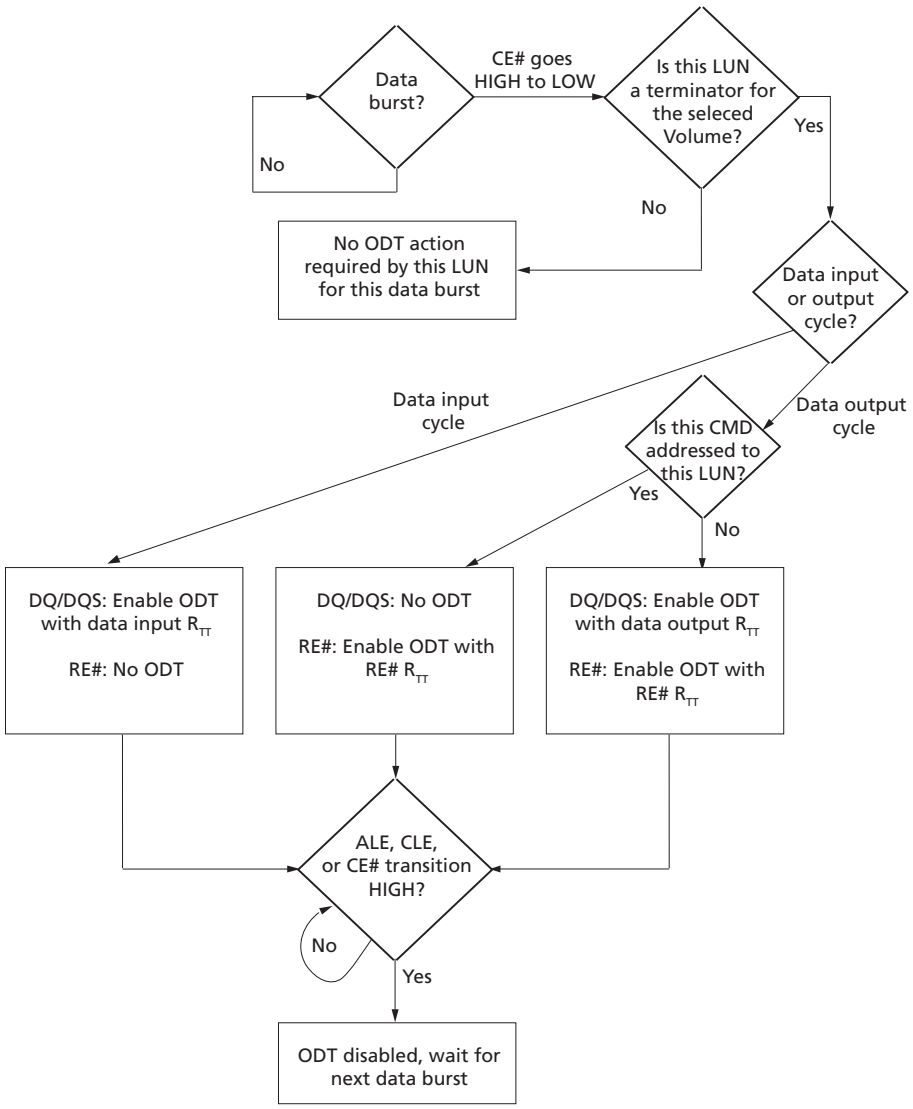
A LUN that is configured to act as a terminator using the configuration matrix (that is specified with the ODT CONFIGURE (E2h) command) may be located on the selected Volume as the Volume it is terminating for (Target termination) or a unselected Volume (non-Target termination). Based on the ODT configuration and the Volume a command is addressed to, LUNs enter different states which determine their ODT behavior; those states are listed in Table 9.

Table 9: LUN state for Matrix Termination

LUN is on selected Volume?	Terminator for selected Volume?	LUN state	ODT actions defined
Yes	N/A	Selected	Figure 27
No	Yes	Sniff	Figure 28
No	No	Deselected	No ODT actions

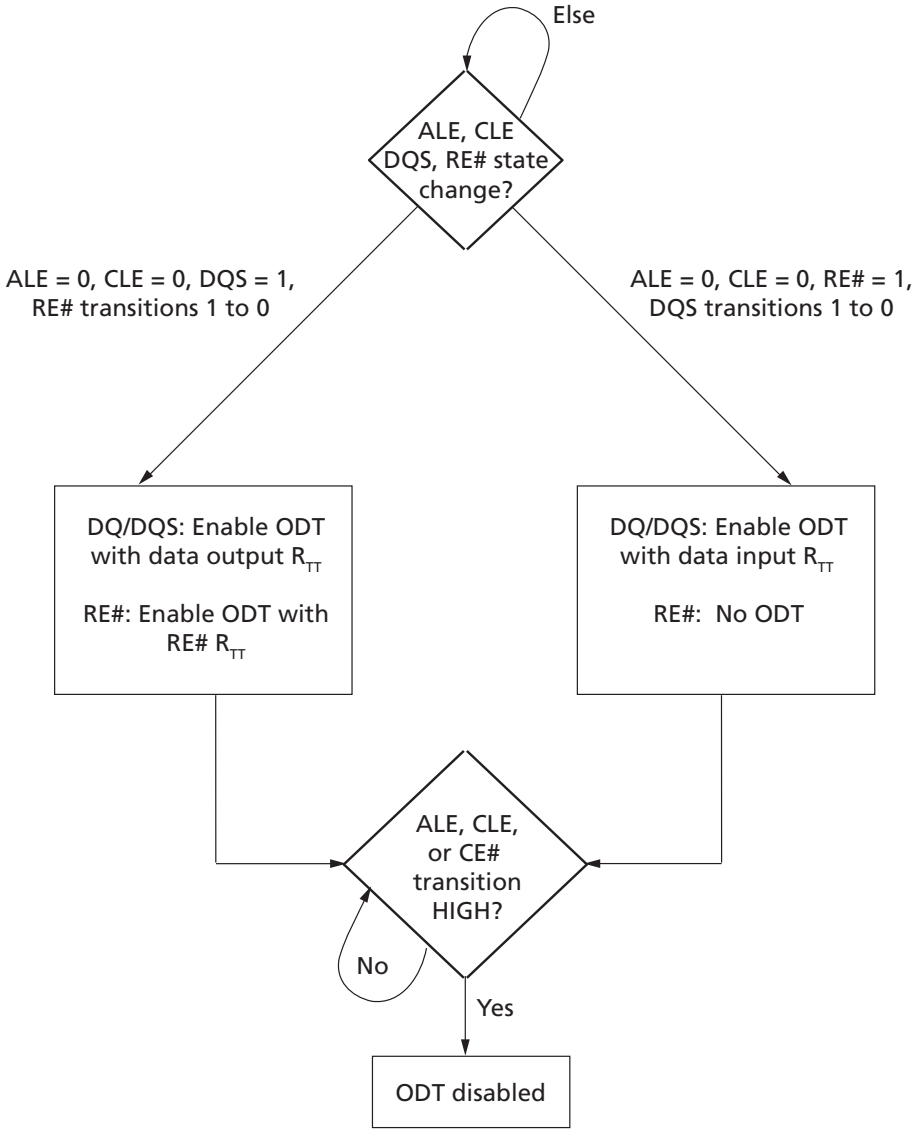
The LUN that a command is addressed to for execution may provide termination. Other LUNs on the selected Volume that are not responsible for execution of the command may also provide termination. Figure 27 (page 51) defines the ODT actions required for LUNs of each of these types on the selected Volume. LUNs on the selected Volume remain in an active state, and thus are aware of state information like whether there is a data burst currently and the type of cycle; these LUNs do not rely only on ALE, CLE, DQS and RE# signals.

Figure 27: ODT actions for LUNs on selected Volume



The ODT configuration matrix also offers the flexibility of having LUNs on an unselected Volume provide termination for the selected Volume. When a LUN is placed in the Sniff state, it checks the ALE, CLE, DQS and RE# signals to determine when to enable or disable ODT. Figure 28 (page 52) defines the ODT actions for LUNs in the Sniff state on an unselected Volume.

Figure 28: ODT actions for LUNs in Sniff state on unselected Volume



Matrix Termination Examples

This section describes two examples of on-die termination configurations using matrix termination. In both examples, each Volume consists of two LUNs, referred to as H0N*n*-LUN0 and H0N*n*-LUN1. The following Volume addresses were appointed at initialization.

Table 10: Volume appointment for Matrix Termination example

Volume	Appointed Volume Address
H0N0	0
H0N1	1
H0N2	2

Table 10: Volume appointment for Matrix Termination example (Continued)

Volume	Appointed Volume Address
H0N3	3

For optimal signal integrity and power consumption, the host may configure termination in a variety of ways. The host may configure a LUN to self terminate, perform non-Target termination for another Volume, or not perform any termination function. Using matrix termination, the termination R_{TT} values may be set differently for each LUN configured as a terminator, including the ability to specify different settings for data output operation and data input operation. The first example shows that a controller may configure the ODT matrix to perform stronger non-Target ODT for data output operations and weaker Target ODT for data input operations.

Table 11: Non-Target ODT for Data Output, Target ODT for Data Input settings configuration example

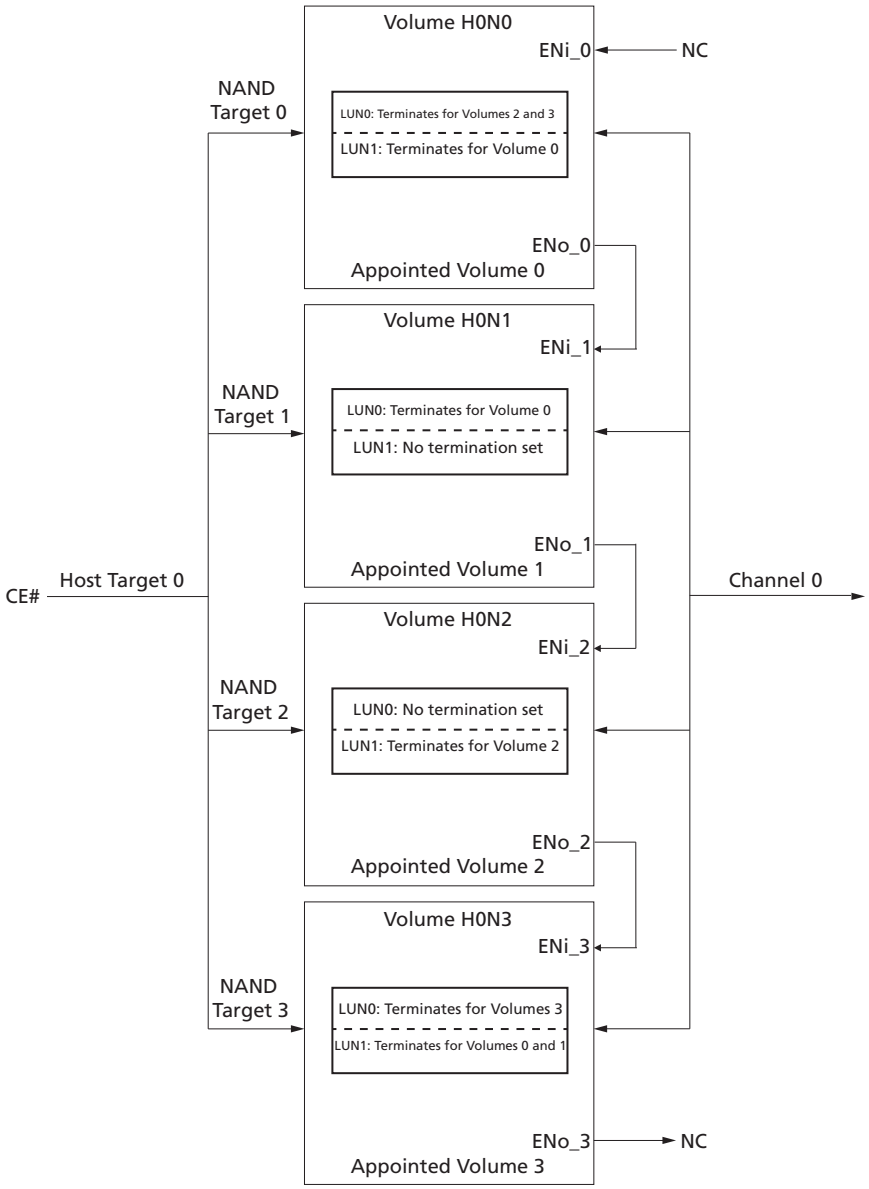
	Input values for ODT CONFIGURE (E2h)				
LUN	Byte M0	Byte M1	Byte R_{TT1}	Byte R_{TT2}	Notes
H0N0-LUN0	0Ch	00h	40h	00h	Terminates for Volumes 2 and 3 (non-Target) for data output with an R_{TT} value of 50 Ohms for DQ[7:0]/DQS
H0N0-LUN1	01h	00h	02h	03h	Terminates for Volume 0 (Target) for data input with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE#
H0N1-LUN0	02h	00h	02h	03h	Terminates for Volume 1 (Target) for data input with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE#
H0N1-LUN1	00h	00h	00h	00h	Does not act as terminator
H0N2-LUN0	00h	00h	00h	00h	Does not act as terminator
H0N2-LUN1	04h	00h	02h	03h	Terminates for Volume 2 (Target) for data input with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE#
H0N3-LUN0	08h	00h	02h	03h	Terminates for Volume 3 (Target) for data input with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE#

Table 11: Non-Target ODT for Data Output, Target ODT for Data Input settings configuration example (Continued)

	Input values for ODT CONFIGURE (E2h)				
LUN	Byte M0	Byte M1	Byte R_{TT1}	Byte R_{TT2}	Notes
H0N3-LUN1	03h	00h	40h	00h	Terminates for Volumes 0 and 1 (non-Target) for data output with an R_{TT} value 50 Ohms for DQ[7:0]/DQS

Note: 1. See ODT CONFIGURE (E2h) (page 130) for details on input values for ODT CONFIGURE (E2h).

Figure 29: Non-Target ODT for Data Output, Target ODT for Data Input configuration example



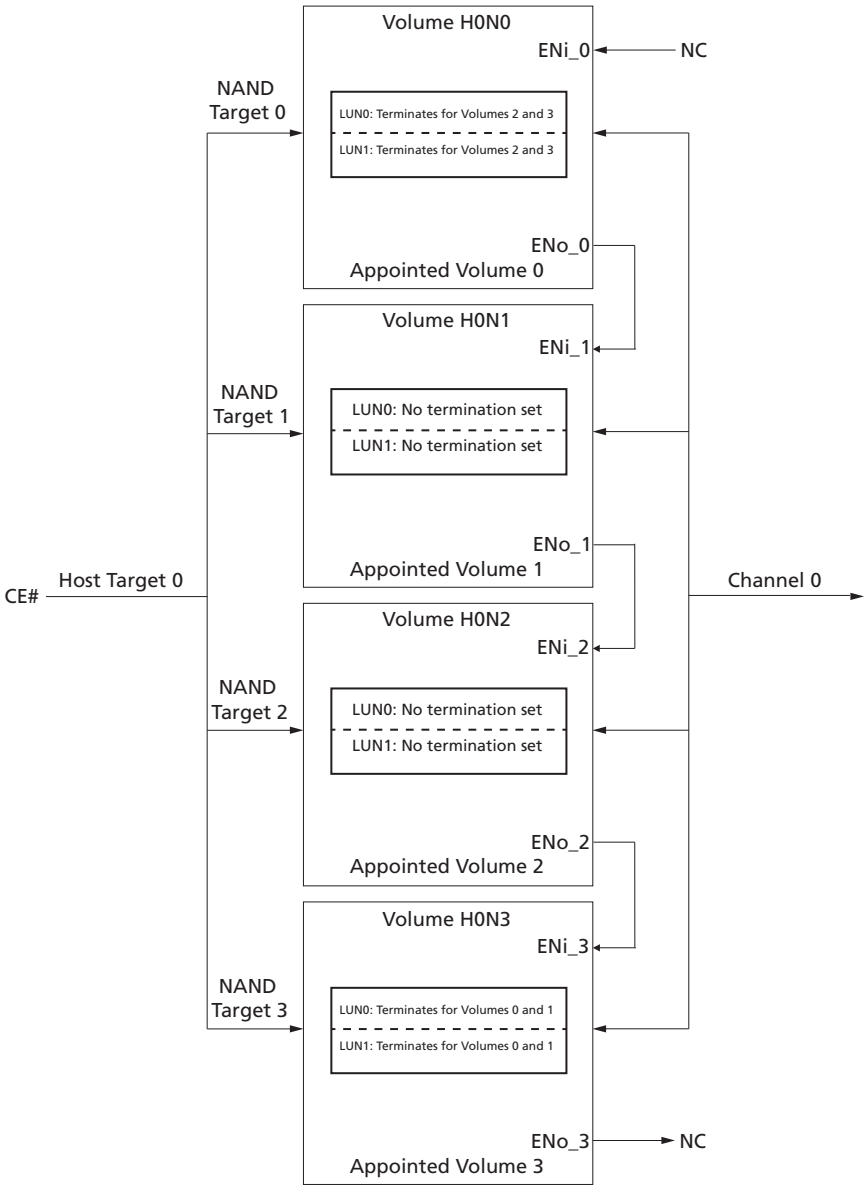
The second example uses parallel non-Target termination to achieve a stronger effective R_{TT} value for both data output and data input operations. For data output, two 50 Ohm terminators are used in parallel to achieve an effective 25 Ohms non-Target termination value. For data input, two 100 Ohm terminators are used in parallel to achieve an effective 50 Ohms non-Target termination value. This type of ODT matrix allows for stronger termination than may be available through a single device. It also allows for intermediate R_{TT} values with the use of different R_{TT} values for parallel LUNs. For example, if one terminator was configured for 75 Ohms and another terminator was configured for 100 Ohms for the same Volume then an effective R_{TT} value of 43 Ohms is achieved. In this example, parallel termination is used for data input and data output for

DQ[7:0]/DQS, however, RE# is non-Target terminated with 100 Ohms using a single LUN.

Table 12: Parallel Non-Target ODT settings configuration example

	Input values for ODT CONFIGURE (E2h)				
LUN	Byte M0	Byte M1	Byte R_{TT1}	Byte R_{TT2}	Notes
H0N0-LUN0	0Ch	00h	42h	00h	Terminates for Volumes 2 and 3 (non-Target) for data output with an R_{TT} value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 2 and 3 (non-Target) for data input with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS.
H0N0-LUN1	0Ch	00h	42h	01h	Terminates for Volumes 2 and 3 (non-Target) for data output with an R_{TT} value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 0 and 1 (non-Target) for data input with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS. Terminates for Volumes 2 and 3 (non-Target) with an R_{TT} value of 150 Ohms for RE#.
H0N1-LUN0	00h	00h	00h	00h	Does not act as terminator
H0N1-LUN1	00h	00h	00h	00h	Does not act as terminator
H0N2-LUN0	00h	00h	00h	00h	Does not act as terminator
H0N2-LUN1	00h	00h	00h	00h	Does not act as terminator
H0N3-LUN0	03h	00h	42h	01h	Terminates for Volumes 0 and 1 (non-Target) for data output with an R_{TT} value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 0 and 1 (non-Target) for data input with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS. Terminates for Volumes 0 and 1 (non-Target) with an R_{TT} value of 150 Ohms for RE#.
H0N3-LUN1	03h	00h	42h	00h	Terminates for Volumes 0 and 1 (non-Target) for data output with an R_{TT} value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 0 and 1 (non-Target) for data input with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS.

Figure 30: Parallel Non-Target ODT configuration example



NV-DDR2 Standby

Prior to disabling a target, the target's bus must be idle. A target is disabled when CE# is driven HIGH, even when it is busy. All of the target's signals are disabled except CE#, WP#, and R/B#.

A target enters low-power standby when it is disabled and is not busy. If the target is busy when it is disabled, the target enters standby after all of the die (LUNs) complete their operations.

NV-DDR2 Idle

A target's bus is idle when CE# is LOW, ALE is LOW, CLE is LOW, RE# is HIGH, and DQS is HIGH and no internal LUN operations are ongoing or data being inputted or outputted from the target. DQS is driven HIGH to prevent the device from enabling ODT. If ODT is disabled, then DQS is a don't care during Idle states.

During the bus idle mode, all signals are enabled. No commands, addresses, or data are latched into the target; no data is output.

NV-DDR2 Pausing Data Input/Output

Pausing data input or data output may be done by placing the bus in an Idle state. The pausing of data output may also be done by pausing RE# and holding the signal(s) static HIGH or LOW until the data burst is resumed. The pausing of data input may also be done by pausing DQS and holding the signal(s) static HIGH or LOW until the data burst is resumed. WE# shall be held HIGH during data input and output burst pause time. ODT (if enabled) stays ON the entire pause time and warmup cycles (if enabled) are not re-issued when re-starting a data burst from pause. The host will be required to exit the data burst if it wishes to disable ODT or re-issue warmup cycles when re-starting. If the host wishes to end the data burst, after exiting the data burst, a new command is issued.

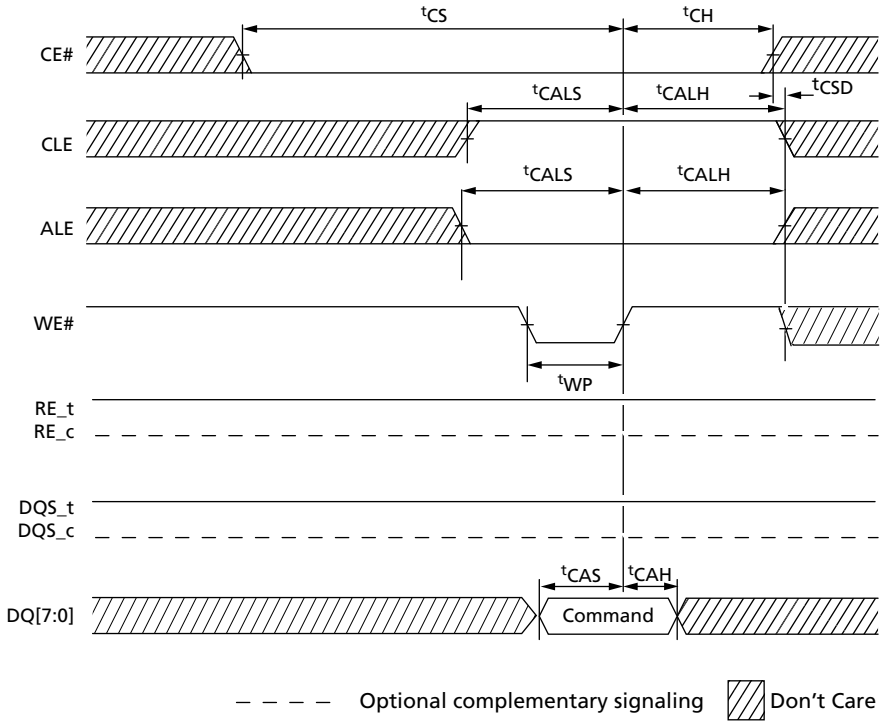
During the bus idle mode, all signals are enabled. No commands, addresses, or data are latched into the target; no data is output.

NV-DDR2 Commands

A command is written from DQ[7:0] to the command register on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is HIGH, and RE# is HIGH.

Commands are typically ignored by die (LUNs) that are busy (RDY = 0); however, some commands, such as READ STATUS (70h) and READ STATUS ENHANCED (78h), are accepted by die (LUNs), even when they are busy.

Figure 31: NV-DDR2 Command Cycle



Note: 1. DQS is "don't care" during active command cycle (CLE is high).

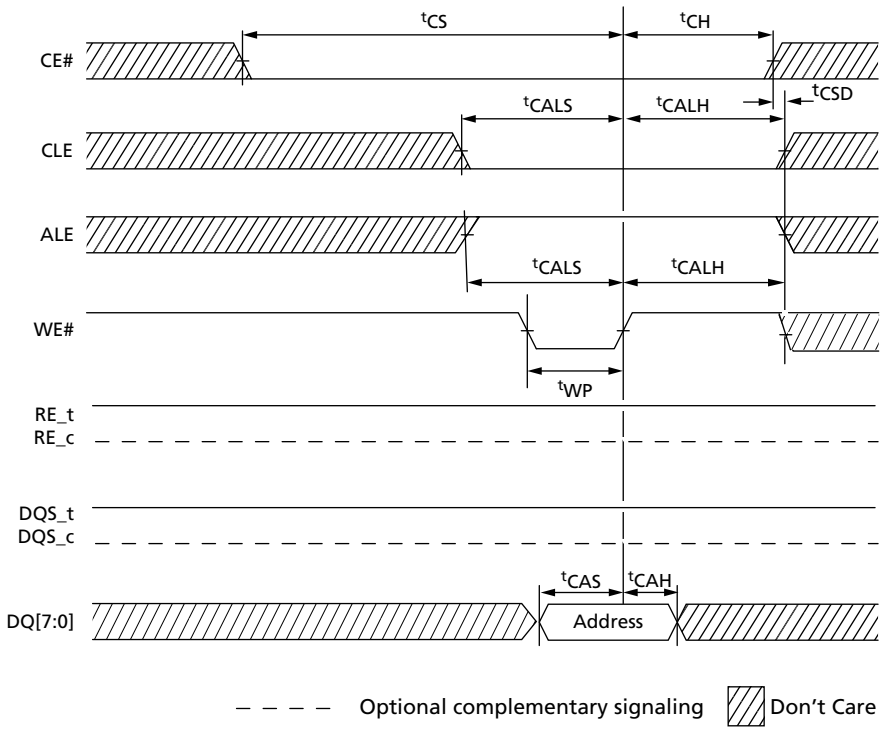
NV-DDR2 Addresses

A NV-DDR2 address is written from DQ[7:0] to the address register on the rising edge of WE# when CE# is LOW, ALE is HIGH, CLE is LOW, and RE# is HIGH.

Bits not part of the address space must be LOW (see Device and Array Organization). The number of address cycles required for each command varies. Refer to the command descriptions to determine addressing requirements.

Addresses are typically ignored by die (LUNs) that are busy (RDY = 0); however, some addresses such as address cycles that follow the READ STATUS ENHANCED (78h) command, are accepted by die (LUNs), even when they are busy.

Figure 32: NV-DDR2 Addresses Cycle



Note: 1. DQS is "don't care" during active address cycle (ALE is high).

NV-DDR2 Data Input

To enter the NV-DDR2 data input mode, the following conditions must be met:

- CE# is LOW
- ALE and CLE are LOW
- RE# is HIGH
- tWPRE is met
- DQS is LOW

Upon entering the NV-DDR2 data input mode after tWPRE, data is written from DQ[7:0] to the cache register on each and every rising and falling edge of DQS (center-aligned) when CE# is LOW, RE# is HIGH, and ALE and CLE are LOW.

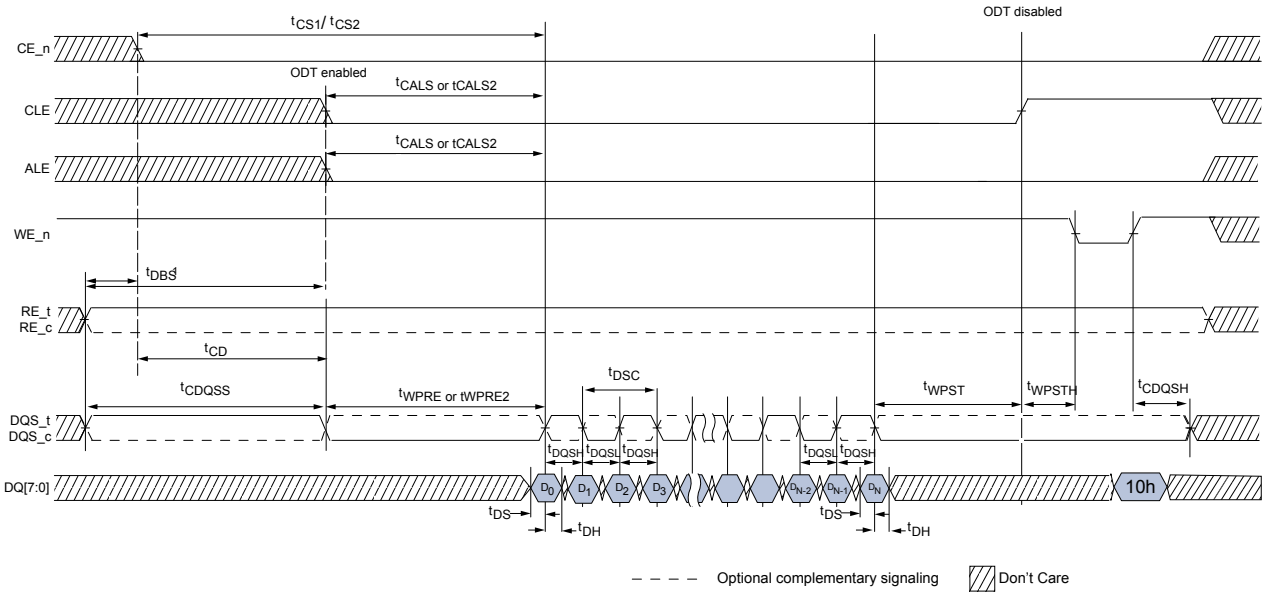
To exit NV-DDR2 data input mode, the following conditions must be met:

- CE# is LOW
- ALE and CLE are LOW
- RE# is HIGH
- The final two data bytes of the data input sequence are written to DQ[7:0] to the cache register on the rising and falling edges of DQS after the last cycle in the data input sequence
- DQS is held LOW for tWPST (after the final falling edge of DQS)

Following tWPST, CE#, CLE, or ALE should be brought HIGH to exit the data burst.

Data input is ignored by die (LUNs) that are not selected or are busy.

Figure 33: NV-DDR2 Data Input Cycles



Note: 1. ODT may not be required to be used for data input. If ODT is selected for use via SET FEATURES (EFh), then ODT is enabled and disabled during the points indicated.

NV-DDR2 Data Output

Data can be output from a die (LUN) if it is ready. Data output is supported following a READ operation from the NAND Flash array.

To enter the NV-DDR2 data output mode, the following conditions must be met:

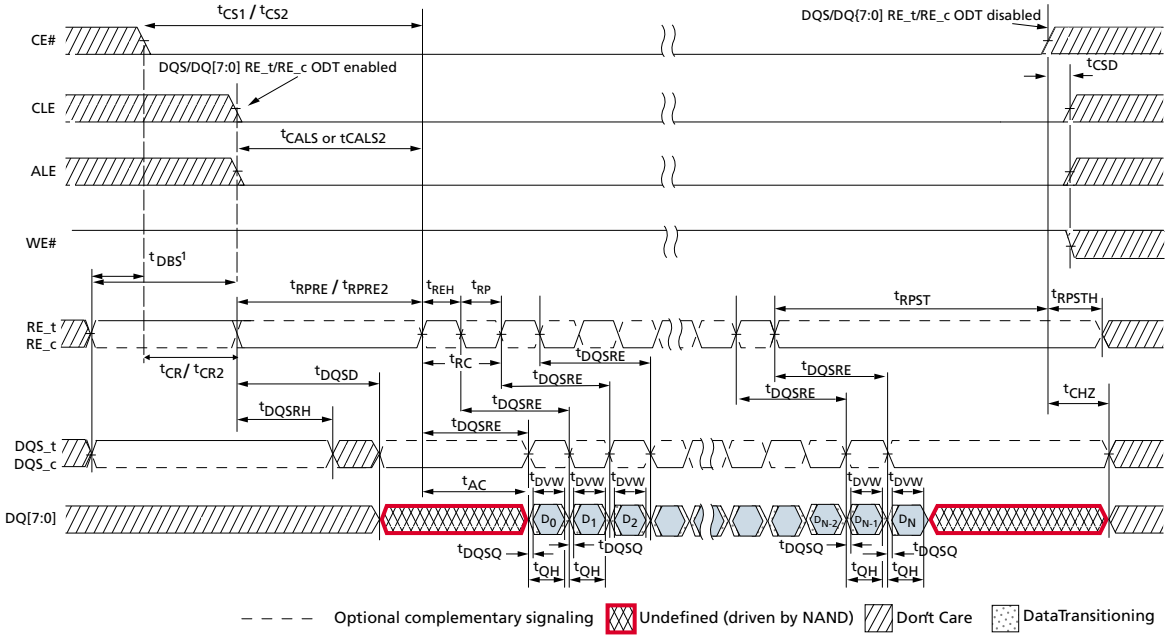
- CE# is LOW
- The host has released the DQ[7:0] bus and DQS
- ALE and CLE are LOW
- tRPRE is met

Upon entering the NV-DDR2 data output mode, DQS will toggle HIGH and LOW with a delay of tDQSRE from the respective rising and falling edges of RE#. DQ[7:0] will output data edge-aligned to the rising and falling edges of DQS, with the first transition delayed by no more than tAC.

The final two data bytes are output on DQ[7:0] on the final rising and falling edges of DQS. The final rising and falling edges of DQS occur tDQSRE after the last cycle in the data output sequence. The host must hold RE# for tRPST after the last RE# falling edge for data output.

Data output requests are typically ignored by a die (LUN) that is busy (RDY = 0); however, it is possible to output data from the status register even when a die (LUN) is busy by issuing the READ STATUS (70h) or READ STATUS ENHANCED (78h) command.

Figure 34: NV-DDR2 Data Output Cycles



Notes:
1. ODT may not be required to be used for data output. If ODT is selected for use via SET FEATURES (EFh), then ODT is enabled and disabled during the points indicated.
2. ^{t}DQSRH is only required if Matrix ODT is enabled.

Write Protect

See Write Protect under Bus Operations - Asynchronous Interface.

Ready/Busy#

See Ready/Busy# under Bus Operations - Asynchronous Interface.

Bus Operation – NV-DDR3 Interface

When the NV-DDR3 interface is activated on a device (see Activating Interfaces), the device is capable of high-speed DDR data transfers. and the DQS signal is enabled. DQS is a bidirectional data strobe. During data output, DQS is driven by the NAND Flash device. During data input, DQS is controlled by the host controller while inputting data on DQ[7:0].

For operations in the NV-DDR3 interface, the NAND device must be powered-on with V_{CCQ} in the 1.2V operational range (see Activating Interfaces (page 72)). The capabilities that NV-DDR3 operations offers beyond NV-DDR2 operations include:

- Supported only at 1.2V V_{CCQ}
- Support for speeds beyond 533MT/s

Use of differential signaling, external V_{REFQ}, and ZQ calibration is optional for interface speeds 200MT/s or slower. Differential signaling and external V_{REFQ} are optional for NV-DDR3 interface speeds faster than 200MT/s but required to guarantee specified AC timings. If a host does not use differential signaling and external V_{REFQ} at speeds faster than 200MT/s, specified AC timings are not guaranteed. If not using the differential signaling, statements about those signal types can be ignored. ZQ calibration is optional for NV-DDR3 interface speeds faster than 533MT/s but required to guarantee specified AC timings. If a host does not use ZQ calibration at speeds faster than 533MT/s, specified AC timings are not guaranteed.

Transition from the NV-DDR3 interface to the Asynchronous, NV-DDR, or NV-DDR2 interface is not permitted.

The NV-DDR3 interface bus modes operate identically to the NV-DDR2 interface. See Bus Operation – NV-DDR2 Interface for details on those modes of operation.

On-die Termination (ODT)

In addition to the description for On-die Termination (ODT) found in the Bus Operation – NV-DDR2 Interface, the following applies for ODT in the NV-DDR3 interface.

On-die termination is enabled when ALE, CLE and CE# transition from HIGH to LOW. On-die termination is disabled when ALE, CLE or CE# transitions from LOW to HIGH.

The on-die termination settings are retained across RESET (FAh, FCh, FFh) commands, but are not retained across HARD RESET (FDh) commands for the target LUN.

Table 13: On-die Termination DC Electrical Characteristics without ZQ Calibration

Mode	Symbol	Min	Typ	Max	Units	Notes
R_{TT} effective impedance value for 50 Ohm setting	$R_{TT1(EFF)}$	32.5	50	80	Ohms	1
R_{TT} effective impedance value for 75 Ohm setting	$R_{TT2(EFF)}$	48.5	75	120	Ohms	1

Table 13: On-die Termination DC Electrical Characteristics without ZQ Calibration (Continued)

Mode	Symbol	Min	Typ	Max	Units	Notes
R_{TT} effective impedance value for 100 Ohm setting	$R_{TT3(EFF)}$	65	100	160	Ohms	1
R_{TT} effective impedance value for 150 Ohm setting	$R_{TT4(EFF)}$	97.5	150	240	Ohms	1
Deviation of VM with respect to V_{CCQ} / 2	ΔVM	-7	-	7	Percent	2

Notes:
1. $R_{TT1\ (EFF)}$, $R_{TT2\ (EFF)}$, $R_{TT3\ (EFF)}$, and $R_{TT4\ (EFF)}$ are determined by separately applying $V_{IH(AC)}$ and $V_{IL(AC)}$ to the signal being tested, and then measuring current $I(V_{IH[AC]})$ and $I(V_{IL[AC]})$, respectively. $R_{TT(EFF)} = (V_{IH[AC]} - V_{IL[AC]}) / (I(V_{IH[AC]}) - I(V_{IL[AC]})$
2. Measure voltage (VM) at the tested signal with no load. $\Delta VM = [(2 \times VM) / V_{CCQ} - 1] \times 100$.

Table 14: On-die Termination DC Electrical Characteristics with ZQ Calibration

Mode	Symbol	Min	Typ	Max	Units	Notes
R_{TT} effective impedance value	$R_{TT(EFF)}$	See Table 15 (page 64)				1
Deviation of VM with respect to V_{CCQ} / 2	ΔVM	-7	-	7	Percent	2

Notes:
1. $R_{TT\ (EFF)}$ is determined by separately applying $V_{IH(AC)}$ and $V_{IL(AC)}$ to the signal being tested, and then measuring current $I(V_{IH[AC]})$ and $I(V_{IL[AC]})$, respectively. $R_{TT(EFF)} = (V_{IH[AC]} - V_{IL[AC]}) / (I(V_{IH[AC]}) - I(V_{IL[AC]})$
2. Measure voltage (VM) at the tested signal with no load. $\Delta VM = [(2 \times VM) / V_{CCQ} - 1] \times 100$.

Table 15: $R_{TT(EFF)}$ Impedance Values with ZQ Calibration

R_{TT}	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
50 Ohms	Rpd	$V_{CCQ} \times 0.2$	0.57	1	1.15	RZQ/3
		$V_{CCQ} \times 0.5$	0.85	1	1.15	RZQ/3
		$V_{CCQ} \times 0.8$	0.85	1	1.47	RZQ/3
	Rpu	$V_{CCQ} \times 0.2$	0.85	1	1.47	RZQ/3
		$V_{CCQ} \times 0.5$	0.85	1	1.15	RZQ/3
		$V_{CCQ} \times 0.8$	0.57	1	1.15	RZQ/3
50 Ohms		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.85	1	1.67	RZQ/6

Table 15: $R_{TT(EFF)}$ Impedance Values with ZQ Calibration (Continued)

R_{TT}	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
75 Ohms	Rpd	V_{CCQ} × 0.2	0.57	1	1.15	RZQ/2
		V_{CCQ} × 0.5	0.85	1	1.15	RZQ/2
		V_{CCQ} × 0.8	0.85	1	1.47	RZQ/2
	Rpu	V_{CCQ} × 0.2	0.85	1	1.47	RZQ/2
		V_{CCQ} × 0.5	0.85	1	1.15	RZQ/2
		V_{CCQ} × 0.8	0.57	1	1.15	RZQ/2
75 Ohms		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.85	1	1.67	RZQ/4
100 Ohms	Rpd	V_{CCQ} × 0.2	0.57	1	1.15	RZQ/1.5
		V_{CCQ} × 0.5	0.85	1	1.15	RZQ/1.5
		V_{CCQ} × 0.8	0.85	1	1.47	RZQ/1.5
	Rpu	V_{CCQ} × 0.2	0.85	1	1.47	RZQ/1.5
		V_{CCQ} × 0.5	0.85	1	1.15	RZQ/1.5
		V_{CCQ} × 0.8	0.57	1	1.15	RZQ/1.5
100 Ohms		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.85	1	1.67	RZQ/3
150 Ohms	Rpd	V_{CCQ} × 0.2	0.57	1	1.15	RZQ/1
		V_{CCQ} × 0.5	0.85	1	1.15	RZQ/1
		V_{CCQ} × 0.8	0.85	1	1.47	RZQ/1
	Rpu	V_{CCQ} × 0.2	0.85	1	1.47	RZQ/1
		V_{CCQ} × 0.5	0.85	1	1.15	RZQ/1
		V_{CCQ} × 0.8	0.57	1	1.15	RZQ/1
150 Ohms		$V_{IL(AC)}$ to $V_{IH(AC)}$	0.85	1	1.67	RZQ/2

Notes:
1. Tolerance limits assume R_{ZQ} of 300 ohms +/- 1% and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage.
2. Refer to Output Driver Sensitivity if either the temperature or the voltage changes after calibration.
3. The minimum values are derated by 6% when the device operates between -40°C and 0°C.

Device Initialization

Some NAND Flash devices do not support V_{CCQ}. For these devices all references to V_{CCQ} are replaced with V_{CC}.

Micron NAND Flash devices are designed to prevent data corruption during power transitions. V_{CC} is internally monitored. (The WP# signal supports additional hardware protection during power transitions.) When ramping V_{CC} and V_{CCQ}, use the following procedure to initialize the device:

1. Ramp V_{CC}.
2. Ramp V_{CCQ}. V_{CCQ} may ramp before, simultaneously, or after V_{CC}.
3. The host must wait for R/B# to be valid and HIGH before issuing RESET (FFh) to any target (see Figure 35). The R/B# signal becomes valid when 50µs has elapsed since the beginning the V_{CC} ramp, and 10µs has elapsed since V_{CCQ} reaches V_{CCQ} (MIN) and V_{CC} reaches V_{CC} (MIN).
4. If not monitoring R/B#, the host must wait at least 100µs after V_{CCQ} reaches V_{CCQ} (MIN) and V_{CC} reaches V_{CC} (MIN). If monitoring R/B#, the host must wait until R/B# is HIGH.
5. Each LUN draws less than an average of I_{ST} measured over intervals of 1ms until the RESET (FFh) command is issued.
6. The RESET (FFh) command must be the first command issued to all targets (CE#s) after the NAND Flash device is powered on. Each target will be busy for ^{t}POR after a RESET command is issued. The RESET busy time can be monitored by polling R/B# or FIXED ADDRESS READ STATUS ENHANCED (71h) command must be used to check initialization status of each LUN on the target. The host must not issue an additional RESET (FFh) command during ^{t}POR.

   If V_{CCQ} is in the 1.8V operational range, then the asynchronous interface is active by default for each target. If V_{CCQ} is in the 1.2V operational range, then the NVDDR3 interface is active by default for each target, but the NV-DDR3 interface will not become active until after ^{t}POR is complete. The host can issue read status commands during ^{t}POR using the NV-DDR3 interface (since read status commands are interface agnostic), and the status register will be updated, but a DQS pulse will not be generated from RE# pulse until ^{t}POR time is complete. If the power-on fails (i.e. E1h status after ^{t}POR), the status register fail status bit will be updated (SR[0]=1), but DQS pulse will not be generated and the NV-DDR3 interface will not be active.
7. The device is now initialized and ready for normal operation.

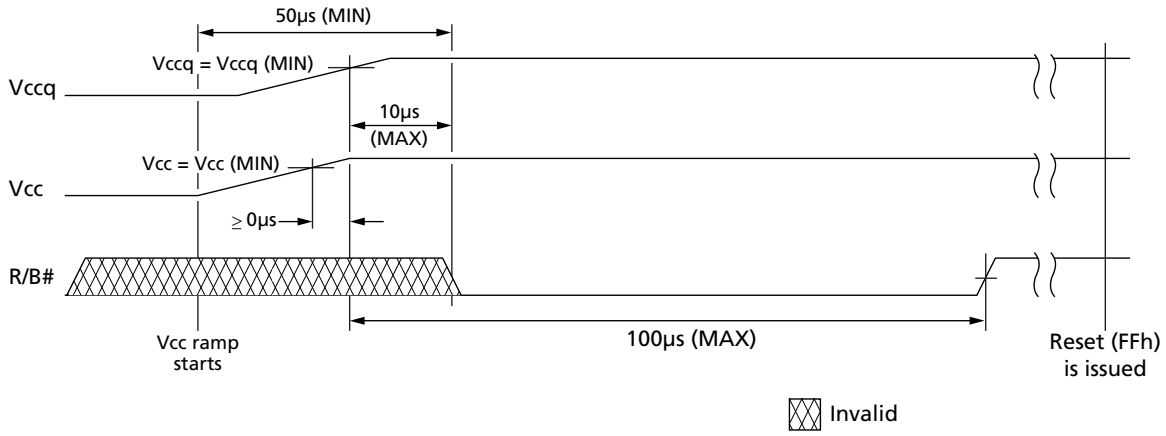
The NV-DDR3 interface is only accessible if the NAND device is powered-on with V_{CCQ} in the 1.2V operational range. See Bus Operations – NV-DDR3 Interface for details.

At power-down, V_{CCQ} may go LOW, either before, simultaneously, or after V_{CC} going LOW.

When V_{CCQ} = 0V, the host must keep RE_t/RE_c, DQS_t/DQS_c signals LOW. RE_t/RE_c, DQS_t/DQS_c signals maybe ramped with V_{CCQ} during power up but not exceed V_{CCQ}. When V_{CCQ} = 0V, the host must keep DQ[7:0] signals LOW or they can be left Hi-Z. DQ[7:0] signals maybe ramped with V_{CCQ} during power up but not exceed V_{CCQ}.

It is not permitted to drive or have the NAND R/B# signal HIGH while the NAND V_{CCQ} voltage is below V_{CCQ} Min. R/B# signals maybe ramped with V_{CCQ} during power up but not exceed V_{CCQ}.

Figure 35: R/B# Power-On Behavior



Note: 1. Disregard V_{CCQ} for devices that use only V_{CC}.

To initialize a discovered target, the following steps shall be taken. The initialization process should be followed for each connected CE# signal, including performing the READ PARAMETER PAGE (ECh) command for each target. Each chip enable corresponds to a unique target with its own independent properties that the host shall observe and subsequently use.

The host should issue the READ PARAMETER PAGE (ECh) command. This command returns information that includes the capabilities, features, and operating parameters of the device. When the information is read from the device, the host shall check the CRC to ensure that the data was received correctly and without error prior to taking action on that data.

If the CRC of the first parameter page read is not valid, the host should read redundant parameter page copies. The host can determine whether a redundant parameter page is present or not by checking if the first four bytes contain at least two bytes of the parameter page signature. If the parameter page signature is present, then the host should read the entirety of that redundant parameter page. The host should then check the CRC of that redundant parameter page. If the CRC is correct, the host may take action based on the contents of that redundant parameter page. If the CRC is incorrect, then the host should attempt to read the next redundant parameter page by the same procedure.

The host should continue reading redundant parameter pages until the host is able to accurately reconstruct the parameter page contents. The host may use bit-wise majority or other ECC techniques to recover the contents of the parameter page from the parameter page copies present. When the host determines that a parameter page signature is not present, then all parameter pages have been read.

After successfully retrieving the parameter page, the host has all information necessary to successfully communicate with that target. If the host has not previously mapped defective block information for this target, the host should next map out all defective blocks in the target. The host may then proceed to utilize the target, including erase and program operations.

V_{PP} Initialization

Some NAND Flash devices do not support V_{PP}.

Micron NAND Flash devices support the V_{PP} signal as a way for the host system to enhance NAND array operations by improving power efficiency. When ramping V_{PP}, use the following procedure to initialize the V_{PP} functionality:

1. V_{PP} can be ramped HIGH before V_{CC} (Min) is reached, simultaneously with V_{CC} (Min) being reached, or after V_{CC} (Min) is reached.
2. V_{PP} must be within its valid voltage range prior to the SET FEATURES (EFh) command to enable the V_{PP} functionality.
3. After V_{PP} is successfully ramped and before V_{PP} functionality can be carried out, the V_{PP} feature must be activated via a SET FEATURE (EFh) command. See the Configurations Operations section for more details.
4. To deactivate V_{PP} functionality outside a device power-down, a SET FEATURE (EFh) command must be issued to disable the V_{PP} functionality while V_{PP} is within its valid voltage range.

At power-down, V_{PP} can ramp LOW before V_{CC} reaches V_{CC} (MIN), simultaneously with V_{CC} reaches V_{CC} (Min), or after V_{CC} (Min) has reached.

Electronic Mirroring

Electronically mirrored DQ[7:0] pinout is available in order to assist in optimizing printed circuit board (PCB) layout by assisting two-sided (clamshell) designs in reducing the complexity and the number of signal routing layers between the top and bottom side of the PCB. This ability for electronic mirrored DQ[7:0] pinout also assists in reducing the vertical profile of a two-sided system. Only the DQ[7:0] signals have the ability to be changed by electronic mirrored functionality, all other NAND signals remain static.

See Figure 36 (page 69) and Figure 37 (page 69) as examples of how packages in the default non-mirrored DQ[7:0] pinout and the mirrored DQ[7:0] pinout could be used in a two-sided PCB system.

Figure 36: Example PCB layout of a two-sided system without electronic mirroring of DQ[7:0]

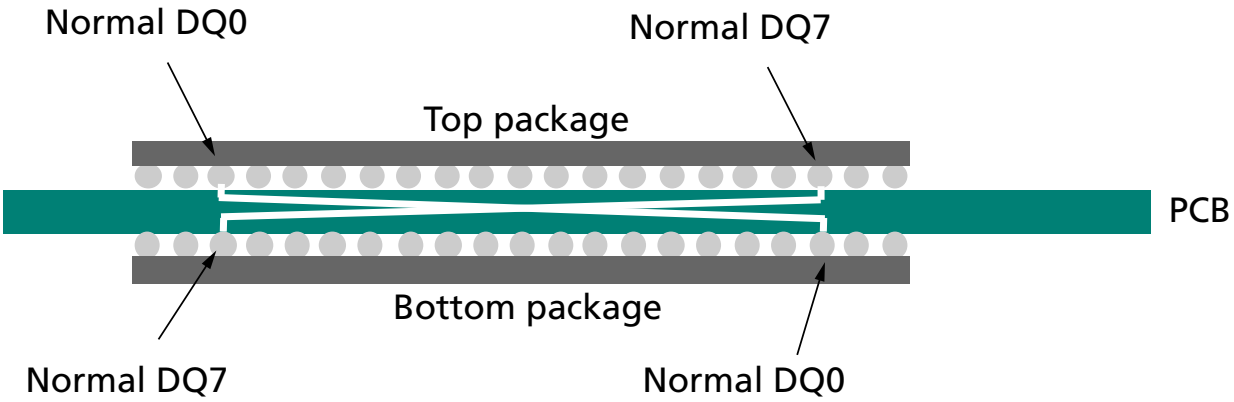
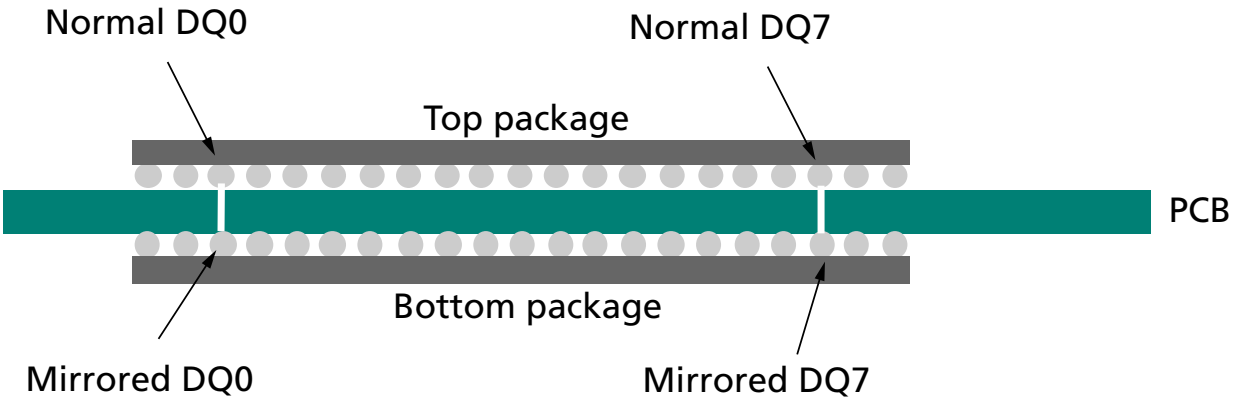


Figure 37: Example PCB layout of a two-sided system with electronic mirroring of DQ[7:0]



The mirror and non-mirrored packages are physically the same with same internal bond connections, but based on how first issued command after device initialization is decoded, the LUNs internally are electrically configured to be non-mirrored or mirrored.

If using the mirrored DQ[7:0] pinout configuration, the READ STATUS (70h) command must be issued in order to properly configure the device DQ[7:0] signals as mirrored or non-mirrored mode after device initialization. This READ STATUS (70h) command appears as "0Eh" on the DQ[7:0] bus of the NAND device in the mirroed position; "0Eh" is not a valid command and is recognized by the NAND device as a 70h command which is the indication to the NAND target (CE#) to configure itself into mirrored DQ[7:0] mode. The READ STATUS (70h) command needs be issued only once per target (CE#) or volume after device initialization for a device in the mirrored position; the device in the mirriored position will remain in the mirrored DQ[7:0] mode until device power-down.

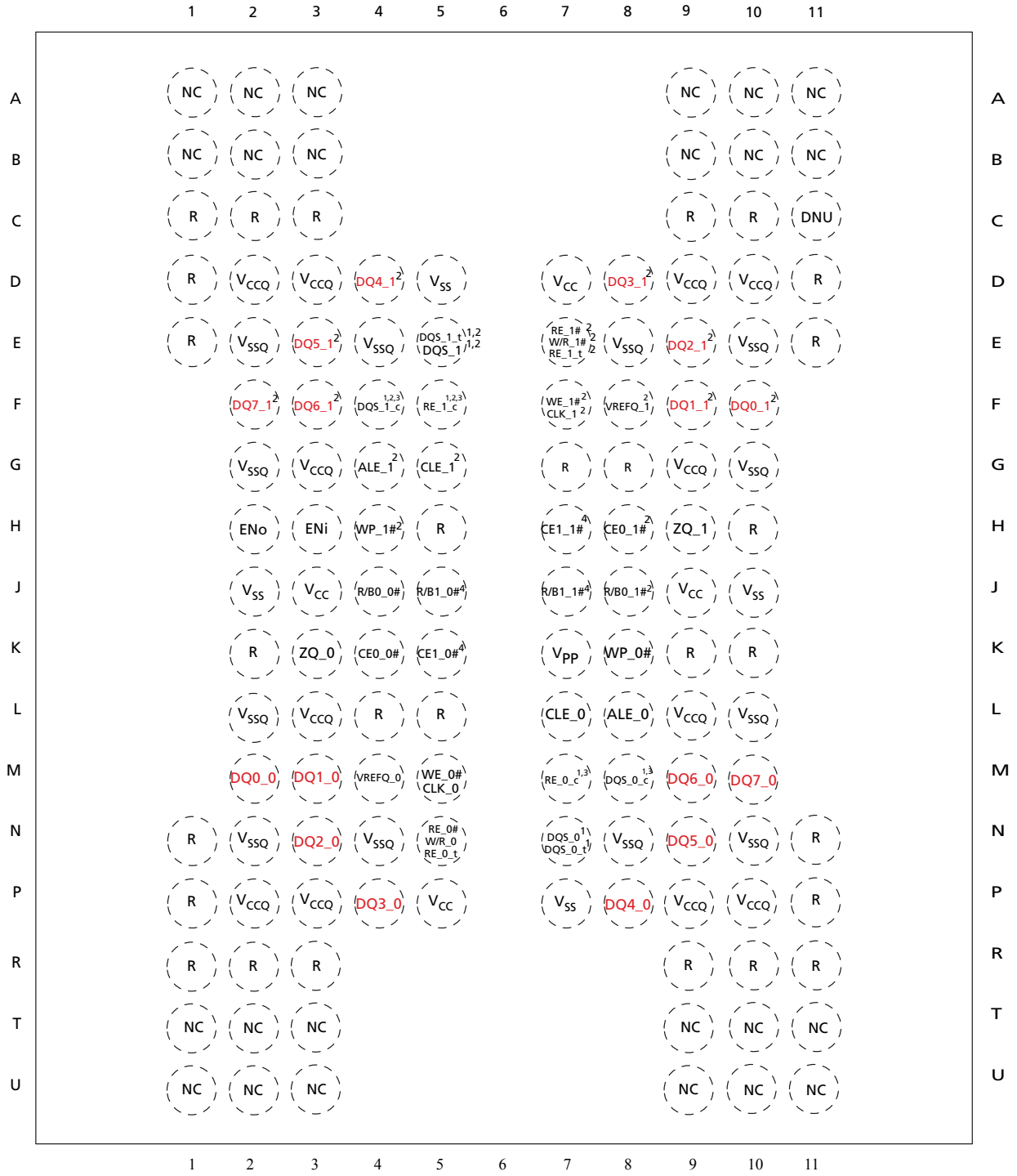
If the READ STATUS (70h) command is issued prior to first RESET (FFh) and CE# pin reduction is enabled, then sequential initialization is enabled. If the READ STATUS (70h) command is issued after the first RESET (FFh) and CE# pin reduction is enabled, then parallel initialization is enabled.

Only the 132-ball and/or 152-ball BGA packages offer electronic mirroring operations. The 272-ball BGA package will not support electronic mirroring due to the limitation of DQ[7:0] signal assignment ordering.

See Figure 38 (page 71) as an example of how a package in the mirrored DQ[7:0] pinout changes signal assignments for the DQ[7:0] signals.

A HARD RESET (FDh) command will not change a device from the mirrored pinout configuration to the non-mirrored pinout configuration.

Figure 38: Example of 132-ball BGA package in mirrored DQ[7:0] pinout



Note: 1. Note the DQ[7:0] signals highlighted in red for the mirrored pinout configuration in comparison to the default non-mirrored pinout configuration. See the Signal Assignments section for the default non-mirrored pinout configuration for this package.

Release: 11/30/15

Activating Interfaces

After performing the steps under Device Initialization (page 66), the asynchronous interface is active for all targets on the device when the device powers on within the 1.8V V_{CCQ} operational range. If the NAND Flash device powers on within the 1.2V V_{CCQ} operational range, the NV-DDR3 interface is active.

Each target's interface is independent of other targets, so the host is responsible for changing the interface for each target.

If the host and NAND Flash device, through error, are no longer using the same interface when within the 1.8V V_{CCQ} operational range, then steps under Activating the Asynchronous Interface are performed to re-synchronize the interfaces.

Activating the Asynchronous Interface

To activate the asynchronous NAND interface, once the synchronous interface is active, the following steps are repeated for each target:

1. The host pulls CE# HIGH, disables its input to CLK, and enables its asynchronous interface.
2. The host pulls CE# LOW and issues the RESET (FFh) command, using an asynchronous command cycle.
3. R/B# goes LOW for ^{t}RST.
4. After ^{t}ITC, and during ^{t}RST, the device enters the asynchronous NAND interface. READ STATUS (70h) and READ STATUS ENHANCED (78h) are the only commands that can be issued.
5. After ^{t}RST, R/B# goes HIGH. Timing mode feature address (01h), subfeature parameter P1 is set to 00h, indicating that the asynchronous NAND interface is active and that the device is set to timing mode 0.

For further details, see Reset Operations.

Activating the NV-DDR Interface

To activate the NV-DDR NAND Flash interface, the following steps are repeated for each target:

1. Issue the SET FEATURES (EFh) command.
2. Write address 01h, which selects the Timing mode feature address.
3. Write P1 with 1Xh, where "X" is the timing mode used in the NV-DDR interface (see Configuration Operations).
4. Write P2–P4 as 00h-00h-00h.
5. R/B# goes LOW for ^{t}ITC. The host should pull CE# HIGH. During ^{t}ITC, the host should not issue any type of command, including status commands, to the NAND Flash device.
6. After ^{t}ITC, R/B# goes HIGH and the synchronous interface is enabled. Before pulling CE# LOW, the host should enable the clock.

Activating the NV-DDR2 Interface

Transitions from NV-DDR directly to NV-DDR2 (or vice versa) is not supported. In this case, the host should transition to the asynchronous interface and then select the desired synchronous interface

Prior to selecting the NV-DDR2 interface, it is recommended that settings for the NV-DDR2 interface be configured. Specifically:

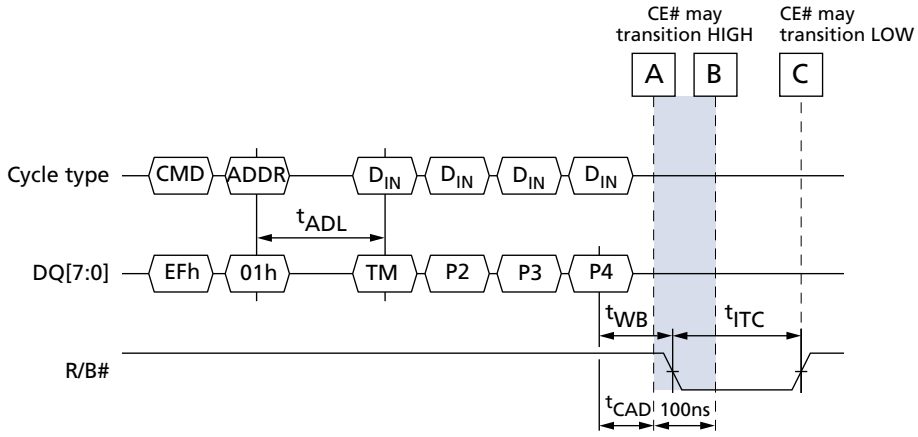
- SET FEATURES (EFh) command should be used to configure the NV-DDR2 Configuration feature address.
- If on-die termination (ODT) is used, the appropriate ODT CONFIGURE (E2) commands should be issued.

These actions should be completed prior to selecting the NV-DDR2 interface. If these settings are modified when the NV-DDR2 interface is already selected, the host should take care to ensure appropriate settings are applied in a manner that avoids signal integrity issues.

To activate the NV-DDR2 NAND Flash interface, the following steps are repeated for each target:

1. Issue the SET FEATURES (EFh) command.
2. Write address 01h, which selects the Timing mode feature address.
3. Write P1 with 2Xh, where "X" is the timing mode used in the NV-DDR2 interface (see Configuration Operations).
4. Write P2–P4 as 00h-00h-00h.
5. R/B# goes LOW for tITC. The host should pull CE# HIGH. During tITC, the host should not issue any type of command, including status commands, to the NAND Flash device.
6. After tITC, R/B# goes HIGH and the NV-DDR2 interface is enabled.

Figure 39: Activating Interfaces



Note: 1. TM = Timing mode.

Activating the NV-DDR3 Interface

The only permittable way to enter the NV-DDR3 interface is to power-on the NAND device within the V_{CCQ} 1.2V operational range. Transitions from the NV-DDR3 interface to the Asynchronous, NV-DDR, or NV-DDR2 interfaces are not supported.

No SET FEATURES (EFh) command is required to activate the NV-DDR3 interface after the device initialization process is complete. Any SET FEATURE (EFh) command to feature address 01h to the data interface bits when in the NV-DDR3 interface will not cause the NAND device to exit the NV-DDR3 interface.

It is recommended that settings for the NV-DDR3 interface be configured. Specifically:

- As the NAND device powers-on directly into the NV-DDR3 interface when within the V_{CCQ} 1.2V operational range, which is capable of beyond 50MT/s interface speeds unlike powering-on in the Asynchronous interface, it is recommended that the host operate in a slower NV-DDR3 timing mode (such as timing mode 2) after power-on to configure the NAND device properly for system signal integrity purposes before transitioning to faster NV-DDR3 timing modes.
- If matrix on-die termination (ODT) is used, the appropriate ODT CONFIGURE (E2) commands should be issued.

CE# Pin Reduction and Volume Addressing

In higher density capacity implementations there may be a significant number of CE# pins required for a host to support where there are many NAND packages with two to four CE# pins per package. The CE# pin reduction mechanism enables a single CE# pin from the host to be shared by multiple NAND targets, thus enabling a significant reduction in the number of CE# pins required by the host system. The CE# pin reduction mechanism may be utilized with any data interface (asynchronous, NV-DDR, NV-DDR2, NV-DDR3).

In the CE# pin reduction mechanism, each NAND package is appointed a volume address during the initialization sequence. After initialization is complete, the host may address a particular volume (NAND target) by using the VOLUME SELECT (E1h) command. See VOLUME SELECT (E1h) for more details.

ENi and ENo pins are added to each NAND package and a daisy chain is created between NAND packages. The first NAND package in the chain has the ENi pin as not connected. All other NAND packages have their ENi pin connected to the previous package's ENo pin in a daisy chain configuration.

At power-on, the ENo pins are driven LOW by the NAND device. ENo shall be High-Z when all CE# signals on the NAND package are HIGH. When a NAND target has had a volume address appointed with the SET FEATURES (EFh) command, then the ENo pin shall be pulled HIGH by the NAND target when the corresponding CE# is LOW. This enables the next NAND target on a subsequent package in the daisy chain to accept commands because the ENi pin pulls HIGH when ENo is no longer pulling LOW. After a volume address has been appointed to a volume (i.e., NAND target), that volume shall become deselected and ignores the ENi pin until the next power cycle.

The state of ENi determines whether the NAND package is able to accept commands. If the ENi pin is HIGH and CE# is LOW for the NAND target, then the NAND target shall accept commands. If the ENi pin is LOW or CE# is HIGH for the NAND Target, then the NAND Target shall not accept commands.

To be selected to process a command, the VOLUME SELECT command shall be issued to the host target using the volume address that was previously appointed for a particular NAND target. After the CE# signal is pulled HIGH for ^{t}CEH time, all LUNs on a volume revert to their previous states.

A HARD RESET (FDh) command will not undo CE# Pin Reduction or any previously set Volume addressing assignments that were performed prior to the HARD RESET (FDh) command.

Figure 40: CE# Pin Reduction Topology with Single Channel

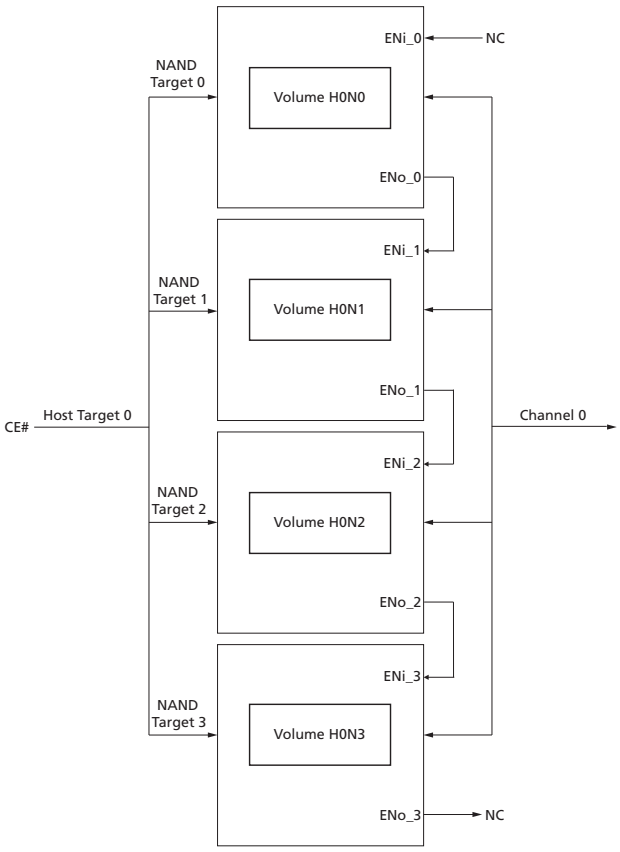
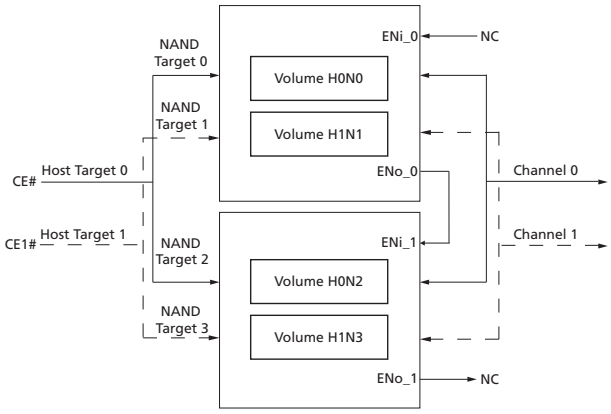


Figure 41: CE# Pin Reduction and Volume Addressing Topology with Dual Channel



Initialization Sequence

The host may issue a RESET (FFh) to all targets in parallel on the selected host target, or the host may sequentially issue RESET (FFh) to each target. The methodology chosen depends on host requirements for maximum current draw. To reset all targets in parallel, the host issues a RESET (FFh) as the first command issued to the NAND device(s). To reset targets sequentially, the host issues a READ STATUS (70h) command as the first command issued to all NAND targets on the selected host target.

During initialization when addressing a newly selected NAND target with an initial command, the host shall wait for the ENo signal to be propagated to the ENi of the subsequent target. Before addressing a new target, the host shall wait (^{t}ENo + ^{t}ENi) and should also include signal propagation time.

In cases where there are multiple NAND targets within a package (multiple CE#), those NAND targets share the same ENo signal, and the host shall not stagger SET FEATURES (EFh) commands that appoint the volume addresses. If the SET FEATURES (EFh) commands are not issued simultaneously, then the host shall wait until volume appointment for previous NAND target(s) is complete before issuing the next SET FEATURES (EFh) command to appoint the volume address for the next NAND target that shares the ENo within a package.

After issuing the SET FEATURE (EFh) command to appoint the volume address, the host shall not issue another command to any NAND target on the associated host target (including status commands) until after the ^{t}FEAT time has elapsed. This is to ensure that the proper NAND target responds to the next command, allowing for the proper ENo/ENi signal levels to be reflected.

The initialization sequence when utilizing the CE# reduction functionality is as follows:

1. The host powers on the NAND device(s).
2. The host pulls CE# LOW.
3. If resetting all NAND targets in parallel, then the host issues the RESET (FFh) command. This command is accepted by all NAND targets connected to the CE# (host target).
4. If resetting each NAND target sequentially, then:
   a. The host issues the READ STATUS (70h) command to check for ready status. Issuing the READ STATUS (70h) command prior to any other command indicates sequential RESET (FFh) of each NAND target. The host then issues the RESET (FFh) command, which is only accepted by NAND devices with ENi set HIGH.
5. The host issues a READ STATUS (70h) command and waits for the device to be ready (RDY = 1; ARDY = 1).
6. The host configures the NAND target via commands necessary to perform that function (READ PARAMETER PAGE (ECh) command, SET FEATURES (EFh) command, etc).
7. The host issues SET FEATURES (EFh) command to the volume configuration feature address to appoint the volume address for the NAND target. The volume address specified shall be unique amongst all NAND targets. After the SET FEATURE (EFh) command completes, ENo is set to one and the volume is deselected until a VOLUME SELECT (E1h) command is issued that selects the volume. The host shall not issue another command to a NAND target connected to the associated host target until after ^{t}FEAT time has elapsed.
8. For each NAND target connected to a host target, steps 4–7 are repeated for sequential initialization, and steps 5–7 are repeated for parallel initialization.

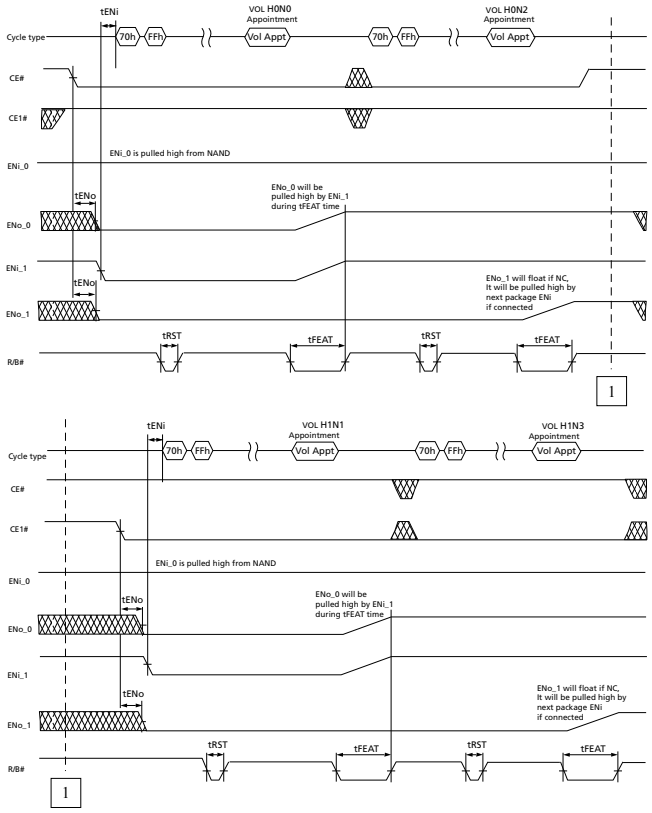
9. When no further NAND targets are found connected to the host target , then repeat steps 2–8 for the next host target (i.e., host CE# pin).
10. To complete the initialization process, a VOLUME SELECT (E1h) command is issued to select the next volume that is going to execute a command.

After volume addresses have been appointed to all NAND targets, the host may complete any additional initialization tasks (for example, configure on-die termination (ODT) for the NV-DDR2 or NV-DDR3 interface) and then proceed with normal operation. Prior to issuing a command to a volume, the VOLUME SELECT (E1h) command shall be issued.

The host CE# signal shall be kept LOW for steps 2–7. If the host CE# signal that is LOW for steps 2–7 is brought HIGH anytime after step 7 but before the initialization process is complete, then ^{t}CS for Asynchronous timing mode 0 shall be used.

Figure 42 (page 78) is an example of sequential reset initialization for the CE# pin reduction topology of Figure 41 (page 76).

Figure 42: Example of Sequential Reset Initialization



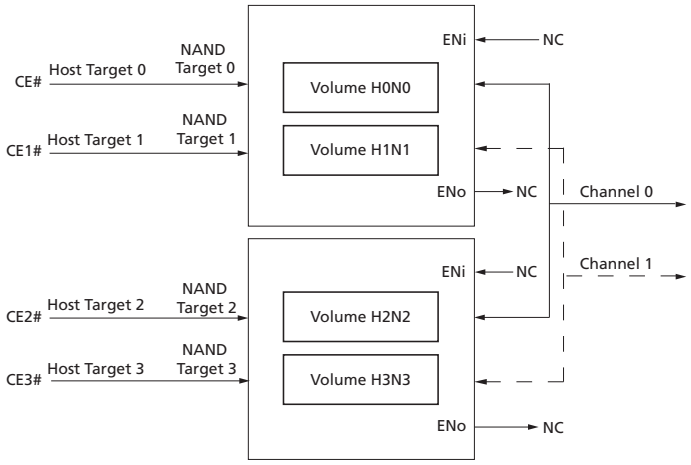
Volume Appointment Without CE# Pin Reduction

If CE# pin reduction is not used (for example, if ENi and ENo are not connected) and the host desires to have the terminator on a package that does not share a CE# with the selected NAND target, then each package that shares the CE# must have a volume appointed at initialization using the SET FEATURE (EFh) command using the volume configuration feature.

Each CE# must have a unique volume address appointed. Once all NAND targets have volume addresses appointed, the appointed volume addresses may be used for termination selection. Volume addressing is not required for operation due to discrete CE# signals; however, the VOLUME SELECT (E1h) command is required for terminator selection when using non-target termination schemes.

During operation, the CE# signal for the selected Volume and for any NAND targets assigned as a terminator for the selected volume need to be brought LOW. When CE# is brought LOW for an unselected volume, all LUNs that are not assigned as terminators for the selected volume are deselected.

Figure 43: Volume Addressing Without CE# Pin Reduction Topology with Dual Channel



Appointing Volume Addresses

To appoint a volume address, the SET FEATURE command is issued with a feature address of volume configuration. The volume address is not retained across power cycles; thus, if volume addressing is going to be used it needs to be appointed after each power-on prior to use of the NAND device(s). The volume address is retained when HARD RESET (FDh) command is issued.

Selecting a Volume

After volume addresses have been appointed, every NAND target (and associated LUN) is selected when the associated CE# is pulled LOW. After CE# is held LOW for at least 100ns, the host issues a VOLUME SELECT (E1h) command to indicate the volume (NAND target) that shall execute the next command issued.

Multiple Volume Operation Restrictions

Volumes are independent entities. A multiple volume operation is when two or more Volumes are simultaneously processing commands. Before issuing a command to an unselected volume, CE# shall be pulled HIGH for a minimum of ^{t}CEH, and the VOLUME SELECT (E1h) command shall then be issued to select the volume to issue a command to next. While commands (including multi-LUN operations) are being performed on the selected volume, a VOLUME SELECT (E1h) command is not required.

Issuing the same command to multiple volumes at the same time is not supported.

For a LUN level command (e.g., READ, PROGRAM), the host may select a different volume during a data input or data output operation and then resume the data transfer operation at a later time for a LUN level command. When re-selecting a Volume and associated LUN to complete the data input or data output operation, the following actions are required:

- Data input: The host shall issue a CHANGE ROW ADDRESS (85h) command prior to resuming data input.
- Data output: The host shall issue a CHANGE READ COLUMN ENHANCED (06h-E0h) or RANDOM DATA OUT (00h-05h-E0h) command prior to resuming data output.

For a target level command (GET FEATURES (EEh), SET FEATURES (EFh)), the host shall complete all data input or data output operations associated with that command prior to selecting a new volume.

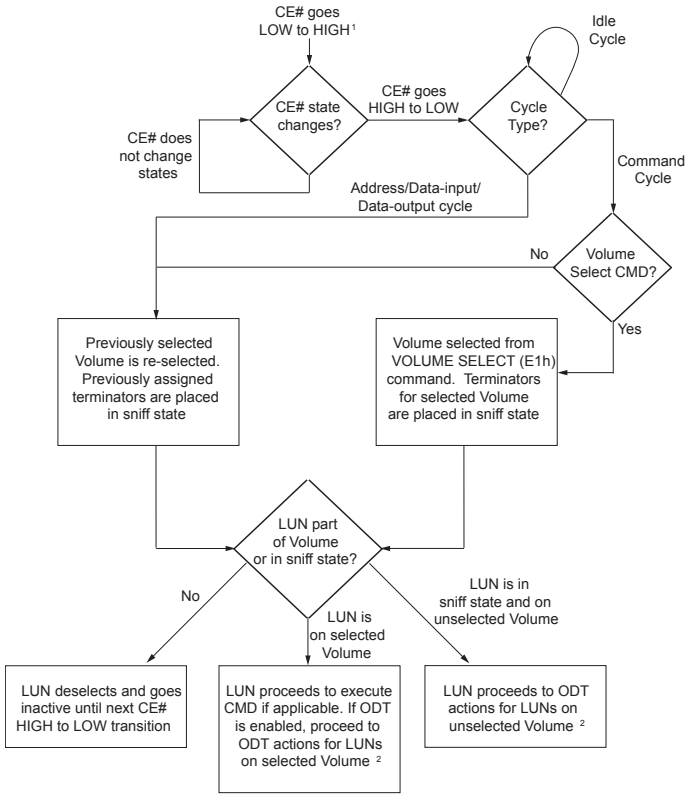
A VOLUME SELECT command shall not be issued during the following atomic portions of the COPYBACK, READ, PROGRAM, and ERASE operations:

- READ operations:
  - READ PAGE (00h-30h)
  - COPYBACK READ (00h-35h)
  - READ PAGE MULTI-PLANE (00h-32h)
  - READ PAGE CACHE RANDOM (00h-31h)
- PROGRAM operations, note: The VOLUME SELECT (E1h) command may be issued prior to the 10h, 11h, or 15h command if the next command to this volume is CHANGE ROW ADDRESS (85h):
  - PROGRAM PAGE (80h-10h)
  - PROGRAM PAGE MULTI-PLANE (80h/81h-11h)
  - PROGRAM PAGE CACHE (80h-15h)
  - COPYBACK PROGRAM (85h-10h)
  - COPYBACK PROGRAM MULTI-PLANE (85h-11h)
- ERASE operations:
  - ERASE BLOCK (60h-D0h)
  - ERASE BLOCK MULTI-PLANE (60h-D1h or 60h-60h-D0h)

Volume Reversion

When using volume addressing, the LUNs shall support Volume reversion. Specifically, if CE# is transitioned from HIGH to LOW and a Volume Select is not the first command, then the LUN shall revert to the previously Selected, Sniff, and Deselected states based on the last specified volume address. If on-die termination is enabled when using the NV-DDR2 or NV-DDR3 data interface there are additional actions described within On Die Termination (ODT).

Figure 44: Volume Reversion behavioral flow



Notes:
1. This state is entered asynchronously when CE# transitions from LOW to HIGH.
2. ODT actions for LUNs on a selected Volume are specified in Figure 27 (page 51). ODT actions for LUNs on an unselected Volume are specified in Figure 28 (page 52).

Command Definitions

Table 16: Command Set

Command	Command Cycle #1	Number of Valid Address Cycles	Data Input Cycles	Command Cycle #2	Number of Valid Address Cycles #2	Command Cycle #3	Valid While Selected LUN is Busy[1]	Valid While Other LUNs are Busy[2]	Notes
Reset Operations									
RESET	FFh	0	–	–	–	–	Yes	Yes	
HARD RESET	FDh	0	–	–	–	–		Yes	
SYNCHRONOUS RESET	FCh	0	–	–	–	–	Yes	Yes	
RESET LUN	FAh	3	–	–	–	–	Yes	Yes	
Identification Operations									
READ ID	90h	1	–	–	–	–			3
READ PARAMETER PAGE	ECh	1	–	–	–	–			
READ UNIQUE ID	EDh	1	–	–	–	–			
Configuration Operations									
VOLUME SELECT	E1h	1	–	–	–	–			
ODT CONFIGURE	E2h	1	4	–	–	–			
GET FEATURES	EEh	1	–	–	–	–			3
SET FEATURES	EFh	1	4	–	–	–			4
GET FEATURES by LUN	D4h	2	–	–	–	–	Yes	Yes	3
SET FEATURES by LUN	D5h	2	4	–	–	–	Yes	Yes	4
ZQ CALIBRATION LONG	F9h	1	–	–	–	–		Yes	
ZQ CALIBRATION SHORT	D9h	1	–	–	–	–		Yes	
Status Operations									
READ STATUS	70h	0	–	–	–	–	Yes		
FIXED ADDRESS READ STATUS ENHANCED	71h	1	–	–	–	–	Yes	Yes	
READ STATUS ENHANCED	78h	3	–	–	–	–	Yes	Yes	
Column Address Operations									
CHANGE READ COLUMN	05h	2	–	E0h	–	–		Yes	
CHANGE READ COLUMN ENHANCED (ONFI)	06h	5	–	E0h	–	–		Yes	

Table 16: Command Set (Continued)

Command	Command Cycle #1	Number of Valid Address Cycles	Data Input Cycles	Command Cycle #2	Number of Valid Address Cycles #2	Command Cycle #3	Valid While Selected LUN is Busy[1]	Valid While Other LUNs are Busy[2]	Notes
CHANGE READ COLUMN ENHANCED (JEDEC)	00h	5	–	05h	2	E0h		Yes	
CHANGE WRITE COLUMN	85h	2	Optional	–	–	–		Yes	
CHANGE ROW ADDRESS	85h	5	Optional	11h (Optional)	–	–		Yes	5
Read Operations									
READ MODE	00h	0	–	–	–	–		Yes	
READ PAGE	00h	5	–	30h	–	–		Yes	6
READ PAGE MULTI-PLANE	00h	5	–	32h	–	–		Yes	
READ PAGE CACHE SEQUENTIAL	31h	0	–	–	–	–		Yes	7
READ PAGE CACHE RANDOM	00h	5	–	31h	–	–		Yes	6,7
READ PAGE CACHE LAST	3Fh	0	–	–	–	–		Yes	7
Program Operations									
PROGRAM PAGE	80h	5	Yes	10h	–	–		Yes	
PROGRAM PAGE MULTI-PLANE	80h or 81h	5	Yes	11h	–	–		Yes	
PROGRAM PAGE CACHE	80h	5	Yes	15h	–	–		Yes	8
PROGRAM SUSPEND	84h	5	–	–	–	–	Yes	Yes	
PROGRAM RESUME	13h	5	–	–	–	–		Yes	
Erase Operations									
ERASE BLOCK	60h	3	–	D0h	–	–		Yes	
ERASE BLOCK MULTI-PLANE (ONFI)	60h	3	–	D1h	–	–		Yes	
ERASE BLOCK MULTI-PLANE (JEDEC)	60h	3	–	60h	3	D0h		Yes	
ERASE SUSPEND	61h	3	–	–	–	–	Yes	Yes	
ERASE RESUME	D2h	–	–	–	–	–		Yes	
Copyback Operations									
COPYBACK READ	00h	5	–	35h	–	–		Yes	6

Table 16: Command Set (Continued)

Command	Command Cycle #1	Number of Valid Address Cycles	Data Input Cycles	Command Cycle #2	Number of Valid Address Cycles #2	Command Cycle #3	Valid While Selected LUN is Busy[1]	Valid While Other LUNs are Busy[2]	Notes
COPYBACK PROGRAM	85h	5	Optional	10h	–	–		Yes	
COPYBACK PROGRAM MULTIPLANE	85h	5	Optional	11h	–	–		Yes	

Notes:
1. Busy means RDY = 0.
2. These commands can be used for interleaved die (multi-LUN) operations.
3. The READ ID (90h), GET FEATURES (EEh), and GET FEATUERS by LUN (D4h) commands output identical data on rising and falling DQS edges.
4. The SET FEATURES (EFh) and SET FEATURES by LUN (D5h) commands requires data transition prior to the rising edge of CLK, with identical data for the rising and falling edges.
5. Command cycle #2 of 11h is conditional. See CHANGE ROW ADDRESS (85h) (page 147) for more details.
6. This command can be preceded by READ PAGE MULTI-PLANE (00h-32h) command to accommodate a maximum simultaneous multi-plane array operation.
7. Issuing a READ PAGE CACHE-series (31h, 00h-31h, 00h-32h, 3Fh) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a READ PAGE (00h-30h) or READ PAGE CACHE-series command; otherwise, it is prohibited.
8. Issuing a PROGRAM PAGE CACHE (80h-15h) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a PROGRAM PAGE CACHE (80h-15h) command; otherwise, it is prohibited.

Reset Operations

RESET (FFh)

The RESET (FFh) command is used to put a target into a known condition and to abort command sequences in progress. This command is accepted by all die (LUNs), even when they are busy.

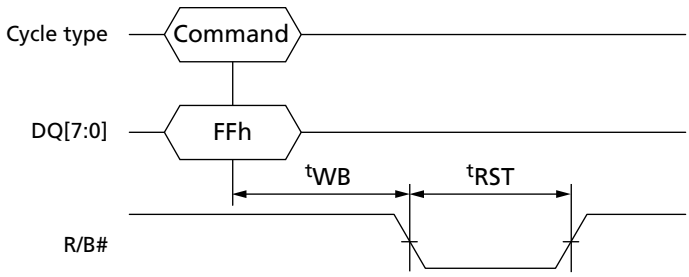
When FFh is written to the command register, the target goes busy for ^{t}RST. During ^{t}RST, the selected target (CE#) discontinues all array operations on all die (LUNs). All pending single- and multi-plane operations are cancelled. If this command is issued while a PROGRAM or ERASE operation is occurring on one or more die (LUNs), the data may be partially programmed or erased and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are valid.

RESET (FFh) must be issued as the first command to each target following power-up (see Device Initialization). Use of the READ STATUS ENHANCED (78h) command is prohibited during the power-on RESET. To determine when the target is ready, use READ STATUS (70h).

If the RESET (FFh) command is issued when the synchronous interface is enabled (NV-DDR/NV-DDR2), the target's interface is changed to the asynchronous interface and the timing mode is set to 0. The RESET (FFh) command can be issued asynchronously when the synchronous (NV-DDR) interface is active, meaning that CLK does not need to be continuously running when CE# is transitioned LOW and FFh is latched on the rising edge of CLK. After this command is latched, the host should not issue any commands during ^{t}ITC. After ^{t}ITC, and during or after ^{t}RST, the host can poll each LUN's status register.

If the RESET (FFh) command is issued when the asynchronous interface is active, the target's asynchronous timing mode remains unchanged. During or after ^{t}RST, the host can poll each LUN's status register.

Figure 45: RESET (FFh) Operation



SYNCHRONOUS RESET (FCh)

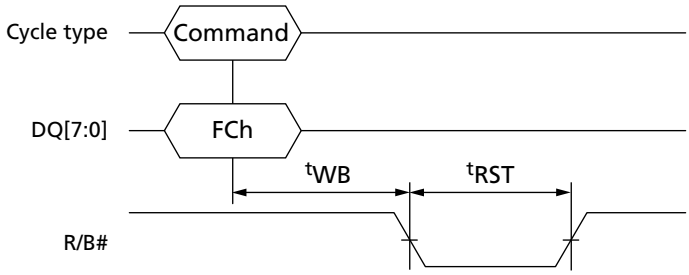
When the synchronous interface is active, the SYNCHRONOUS RESET (FCh) command is used to put a target into a known condition and to abort command sequences in progress. This command is accepted by all die (LUNs), even when they are BUSY.

When FCh is written to the command register, the target goes busy for ^{t}RST. During ^{t}RST, the selected target (CE#) discontinues all array operations on all die (LUNs). All pending single- and multi-plane operations are cancelled. If this command is issued while a PROGRAM or ERASE operation is occurring on one or more die (LUNs), the data may be partially programmed or erased and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are valid and the synchronous interface remains active.

During or after ^{t}RST, the host can poll each LUN's status register.

SYNCHRONOUS RESET is only accepted while the synchronous interface (NV-DDR/NV-DDR2/NV-DDR3) is active. Its use is prohibited when the asynchronous interface is active.

Figure 46: SYNCHRONOUS RESET (FCh) Operation



RESET LUN (FAh)

The RESET LUN (FAh) command is used to put a particular LUN on a target into a known condition and to abort command sequences in progress. This command is accepted by only the LUN addressed by the RESET LUN (FAh) command, even when that LUN is busy.

When FAh is written to the command register, the addressed LUN goes busy for ^{t}RST. During ^{t}RST, the selected LUN discontinues all array operations. All pending single- and multi-plane operations are canceled. If this command is issued while a PROGRAM or ERASE operation is occurring on the addressed LUN, the data may be partially programmed or erased and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are valid.

If the RESET LUN (FAh) command is issued when the synchronous (NV-DDR/NV-DDR2/NV-DDR3) interface is enabled, the targets's interface remains in synchronous mode.

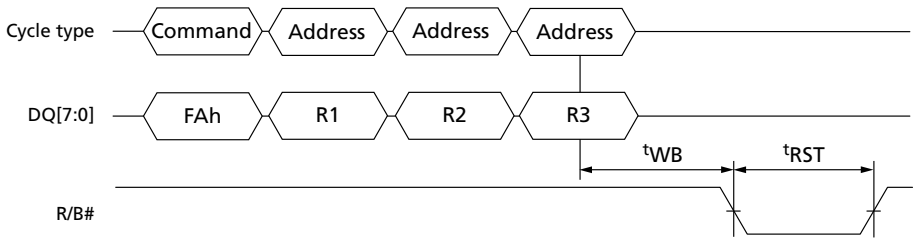
If the RESET LUN (FAh) command is issued when the asynchronous interface is enabled, the target's interface remains in asynchronous mode.

During or after ^{t}RST, the host can poll each LUN's status register.

The RESET LUN (FAh) command is prohibited when not in the default array operation mode.

The RESET LUN (FAh) command can only be issued to a target (CE#) after the RESET (FFh) command has been issued as the first command to a target following power-up.

Figure 47: RESET LUN (FAh) Operation



HARD RESET (FDh)

The HARD RESET (FDh) command is used to put a particular die (LUN) on a target into a known condition similar to that of a power-on initialized state. The HARD RESET (FDh) command is accepted by only the LUN previously selected by a READ STATUS ENHANCED (78h) command. The host is required to issue a READ STATUS ENHANCED (78h) command prior to issuing the HARD RESET (FDh) command, there should be no other NAND commands after the READ STATUS ENHANCED (78h) command and before the HARD RESET (FDh) command issued by the host. The HARD RESET (FDh) command is only permitted to be issued when the selected LUN is not in a busy state (RDY=1, ARDY=1).

HARD RESET (FDh) performs a initialization to the die (LUN) similar to the initialization performed during the first RESET (FFh) command at device power-on. All target LUN parameters and configurations shall be initialized to default values. The target LUN is chosen by the host issuing a READ STATUS ENHANCED (78h) command prior to issuing the HARD RESET (FDh) command. The HARD RESET (FDh) operation is completed within ^{t}POR. After ^{t}POR, the data register and cache register contents of the previously selected LUN that carried out the HARD RESET (FDh) operation are invalid.

In shared CE# configuration, only the selected LUN shall perform the HARD RESET (FDh) command. The host is required to issue the READ STATUS ENHANCED (78h) command prior to issuing the HARD RESET (FDh) command to select LUN to perform the HARD RESET (FDh) operation.

If in the NV-DDR or NV-DDR2 interface, issuing a HARD RESET (FDh) command will revert the NAND interface back to Asynchronous mode. If the HARD RESET (FDh) command is issued with the NV-DDR3 interface is enabled, the target's interface remains in NV-DDR3 and the timing mode is set to 0.

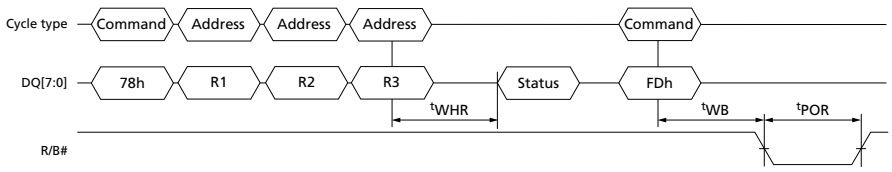
If the HARD RESET (FDh) command is issued when the asynchronous interface is enabled, the target's interface remains in asynchronous mode and timing mode is set to 0.

During or after ^{t}POR, the host can poll each LUN's status register. A status command is only valid 5µs after Hard Reset (FDh) is issued, incorrect status may result if status command is issued within 5µs of Hard Reset (FDh) command.

The HARD RESET (FDh) command is prohibited when not in the default array operation mode.

The HARD RESET (FDh) command can only be issued to a target (CE#) after the RESET (FFh) command has been issued as the first command to a target following power-up. A HARD RESET (FDh) command will not change a device from the mirrored pinout configuration to the non-mirrored pinout configuration or change CE# Pin Reduction. A HARD RESET (FDh) command will change all feature addresses back to their default values for the target LUN with the exception of previously assigned Volume configuration (feature address 58h).

Figure 48: HARD RESET (FDh) Operation



Identification Operations

READ ID (90h)

The READ ID (90h) command is used to read identifier codes programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing 90h to the command register puts the target in read ID mode. The target stays in this mode until another valid command is issued.

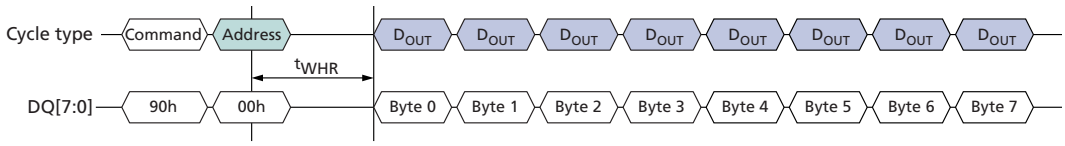
When the 90h command is followed by a 00h address cycle, the target returns a 5-byte identifier code that includes the manufacturer ID, device configuration, and part-specific information.

When the 90h command is followed by a 20h address cycle, the target returns the 6-byte ONFI identifier code.

When the 90h command is followed by a 40h address cycle, the target returns the 5-byte JEDEC identifier code.

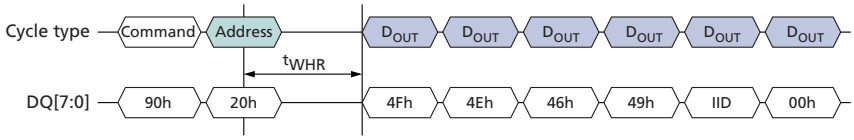
After the 90h and address cycle are written to the target, the host enables data output mode to read the identifier information. When the asynchronous interface is active, one data byte is output per RE# toggle. When the NV-DDR interface is active, one data byte is output per rising edge of DQS when ALE and CLE are HIGH; the data byte on the falling edge of DQS is identical to the data byte output on the previous rising edge of DQS. When the NV-DDR2 or NV-DDR3 interface is active, one data byte is output per rising edge of DQS when ALE and CLE are LOW; the data byte on the falling edge of DQS is identical to the data byte output on the previous rising edge of DQS.

Figure 49: READ ID (90h) with 00h Address Operation



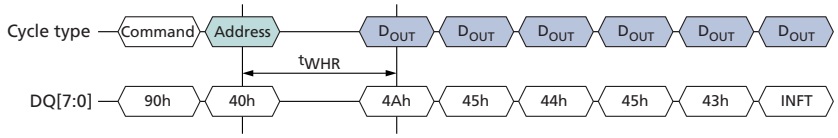
Note: 1. See the READ ID Parameter tables for byte definitions.

Figure 50: READ ID (90h) with 20h Address Operation



Note: 1. See the READ ID Parameter tables for byte definitions.

Figure 51: READ ID (90h) with 40h Address Operation



Note: 1. See the READ ID Parameter tables for byte definitions.

READ ID Parameter Tables

Table 17: Read ID Parameters for Address 00h

Device	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
MT29F256G08CBHBB	2Ch	A4h	64h	32h	AAh	04h	00h	00h
MT29F512G08CEHBB	2Ch	A4h	64h	32h	AAh	04h	00h	00h
MT29F1T08CMHBB	2Ch	A4h	64h	32h	AAh	04h	00h	00h
MT29F2T08CUHBB	2Ch	C4h	E5h	32h	AAh	04h	00h	00h
MT29F4T08CTHBB	2Ch	C4h	E5h	32h	AAh	04h	00h	00h

Note: 1. h = hexadecimal.

Table 18: Read ID Parameters for Address 20h

Device	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
MT29F256G08CBHBB	4Fh	4Eh	46h	49h	01h
MT29F512G08CEHBB	4Fh	4Eh	46h	49h	01h
MT29F1T08CMHBB	4Fh	4Eh	46h	49h	01h
MT29F2T08CUHBB	4Fh	4Eh	46h	49h	01h
MT29F4T08CTHBB	4Fh	4Eh	46h	49h	01h

Notes: 1. h = hexadecimal.
2. XXh = Undefined.

Table 19: Read ID Parameters for Address 40h

Device	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
Asynchronous or Synchronous	4Ah	45h	44h	45h	43h	05h

Note: 1. h = hexadecimal.

READ PARAMETER PAGE (ECh)

The READ PARAMETER PAGE (ECh) command is used to read the ONFI or JEDEC parameter page programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing ECh to the command register puts the target in read parameter page mode. The target stays in this mode until another valid command is issued.

When the ECh command is followed by an 00h or 40h address cycle, the target goes busy for ^{t}R. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode. Use of the READ STATUS ENHANCED (78h) command is prohibited while the target is busy and during data output.

After ^{t}R completes, the host enables data output mode to read the parameter page. When the asynchronous interface is active, one data byte is output per RE# toggle. When the synchronous interface is active, one data byte is output for each rising or falling edge of DQS.

A minimum of three copies of the parameter page are stored in the device. Each parameter page is 256 bytes. If desired, the CHANGE READ COLUMN (05h-E0h) command can be used to change the location of data output. Use of the CHANGE READ COLUMN ENHANCED (06h-E0h or 00h-05h-E0h) command is prohibited.

The READ PARAMETER PAGE (ECh) output data can be used by the host to configure its internal settings to properly use the NAND Flash device. Parameter page data is static per part, however the value can be changed through the product cycle of NAND Flash. The host should interpret the data and configure itself accordingly.

The host should continue reading redundant parameter pages until the host is able to accurately reconstruct the parameter page contents. Parameter pages returned by the target may have invalid CRC values; however, bit-wise majority may be used to recover the contents of the parameter page. The host may use bit-wise majority or other techniques to recover the contents of the parameter page from the parameter page copies present.

Figure 52: READ PARAMETER (ECh) with 00h Address Operation for ONFI

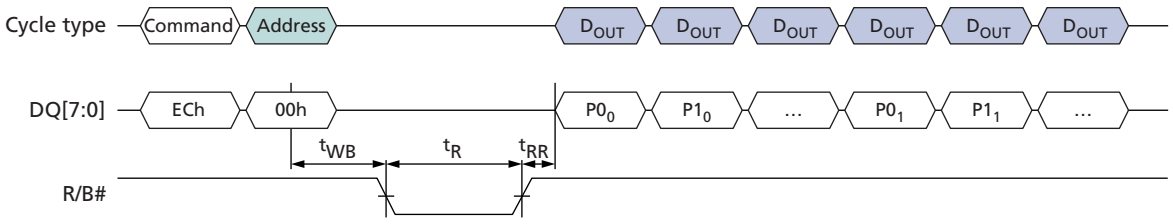
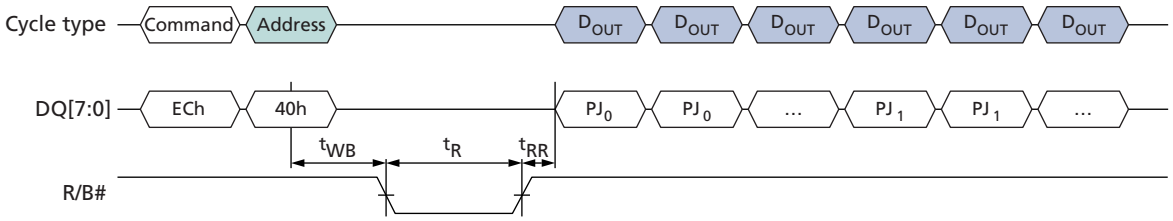


Figure 53: READ PARAMETER (ECh) with 40h Address Operation for JEDEC



Parameter Page Data Structure Tables

Table 20: ONFI Parameter Page Data Structure

Byte	Description	Device	Values
Revision information and features block			
0–3	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"	–	4Fh, 4Eh, 46h, 49h
4–5	Revision number Bit[15:10]: Reserved (0) Bit 9: 1 = supports ONFI version 4.0 Bit 8: 1 = supports ONFI version 3.2 Bit 7: 1 = supports ONFI version 3.1 Bit 6: 1 = supports ONFI version 3.0 Bit 5: 1 = supports ONFI version 2.3 Bit 4: 1 = supports ONFI version 2.2 Bit 3: 1 = supports ONFI verion 2.1 Bit 2: 1 = supports ONFI version 2.0 Bit 1: 1 = supports ONFI version 1.0 Bit 0: Reserved (0)	–	FEh, 03h
6–7	Features supported Bit15: 1 = supports Package Electrical Specification Bit 14: 1 = supports ZQ calibration Bit 13: 1 = supports NV-DDR3 Bit 12: 1 = supports external V_{PP} Bit 11: 1 = supports Volume addressing Bit 10: 1 = supports NV-DDR2 interface Bit 9: 0 = Reserved Bit 8: 1 = supports program page register clear enhancement Bit 7: 1 = supports extended parameter page Bit 6: 1 = supports interleaved (multi-plane) read operations Bit 5: 1 = supports NV-DDR interface Bit 4: 1 = supports odd-to-even page copyback Bit 3: 1 = supports interleaved (multi-plane) program and erase operations Bit 2: 1 = supports non-sequential page programming Bit 1: 1 = supports multiple LUN operations Bit 0: 1 = supports 16-bit data bus width	MT29F256G08CBHBBJ4 MT29F512G08CEHBBJ4 MT29F1T08CMHBBJ4	F8h, FDh
		MT29F2T08CUHBBM4 MT29F4T08CTHBBM5	FAh, FDh

Table 20: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
8–9	Optional commands supported Bit[15:14]: Reserved (0) Bit 13: 1 = supports ZQ calibration (Long and Short) Bit 12: 1 = supports GET/SET Features by LUN Bit 11: 1 = supports ODT CONFIGURE Bit 10: 1 = supports VOLUME SELECT Bit 9: 1 = supports RESET LUN Bit 8: 1 = supports small data move Bit 7: 1 = supports CHANGE ROW ADDRESS Bit 6: 1 = supports CHANGE READ COLUMN ENHANCED Bit 5: 1 = supports READ UNIQUE ID Bit 4: 1 = supports COPYBACK Bit 3: 1 = supports READ STATUS ENHANCED Bit 2: 1 = supports GET FEATURES and SET FEATURES Bit 1: 1 = supports read cache commands Bit 0: 1 = supports PROGRAM PAGE CACHE	–	FFh, 3Fh
10	ONFI-JEDEC JTG primary advanced command support Bit[7:4]: Reserved (0) Bit 3: 1 = supports ERASE BLOCK MULTI-PLANE Bit 2: 1 = supports COPYBACK PROGRAM MULTI-PLANE Bit 1: 1 = supports PROGRAM PAGE MULTI-PLANE Bit 0: 1 = supports CHANGE READ COLUMN	–	0Fh
11	Reserved (0)	–	All 00h
12–13	Extended parameter page length	–	03h, 00h
14	Number of parameter pages	–	3Dh
15–31	Reserved (0)	–	All 00h
Manufacturer information block			
32–43	Device manufacturer (12 ASCII characters) Micron	–	4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h

Table 20: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
44–63	Device model (20 ASCII characters)	MT29F256G08CBHBBJ4	4Dh, 54h, 32h, 39h, 46h, 32h, 35h, 36h, 47h, 30h, 38h, 43h, 42h, 48h, 42h, 42h, 4Ah, 34h, 20h, 20h
		MT29F512G08CEHBBJ4	4Dh, 54h, 32h, 39h, 46h, 35h, 31h, 32h, 47h, 30h, 38h, 43h, 45h, 48h, 42h, 42h, 4Ah, 34h, 20h, 20h
		MT29F1T08CMHBBJ4	4Dh, 54h, 32h, 39h, 46h, 31h, 54h, 30h, 38h, 43h, 4Dh, 48h, 42h, 42h, 4Ah, 34h, 20h, 20h, 20h, 20h
		MT29F2T08CUHBBM4	4Dh, 54h, 32h, 39h, 46h, 32h, 54h, 30h, 38h, 43h, 55h, 48h, 42h, 42h, 4Dh, 34h, 20h, 20h, 20h, 20h
		MT29F4T08CTHBBM5	4Dh, 54h, 32h, 39h, 46h, 34h, 54h, 30h, 38h, 43h, 54h, 48h, 42h, 42h, 4Dh, 35h, 20h, 20h, 20h, 20h
64	JEDEC manufacturer ID	–	2Ch
65–66	Date code	–	00h, 00h
67–79	Reserved (0)	–	All 00h
Memory organization block			
80–83	Number of data bytes per page	–	00h, 40h, 00h, 00h
84–85	Number of spare bytes per page	–	A0h, 08h
86–91	Reserved (0)	–	All 00h
92–95	Number of pages per block	–	00h, 04h, 00h, 00h
96–99	Number of blocks per LUN	–	90h, 08h, 00h, 00h
100	Number of LUNs per chip enable	MT29F256G08CBHBBJ4	01h
		MT29F512G08CEHBBJ4	
		MT29F1T08CMHBBJ4	
		MT29F2T08CUHBBM4	02h
		MT29F4T08CTHBBM5	
101	Number of address cycles Bit[7:4]: Column address cycles Bit[3:0]: Row address cycles	–	23h
102	Number of bits per cell	–	02h

Table 20: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
103–104	Bad blocks maximum per LUN	–	94h, 00h
105–106	Block endurance	–	03h, 03h
107	Guaranteed valid blocks at beginning of target	–	01h
108–109	Block endurance for guaranteed valid blocks	–	00h, 00h
110	Number of programs per page	–	01h
111	Reserved (0)	–	00h
112	Number of bits ECC correctability	–	FFh
113	Number of interleaved address bits Bit[7:4]: Reserved (0) Bit[3:0]: Number of interleaved address bits	–	02h
114	Interleaved operation attributes Bit[7:6]: Reserved (0) Bit 5: Reserved Bit 4: 1 = supports read cache Bit 3: Address restrictions for cache operations Bit 2: 1 = supports program cache Bit 1: 1 = no block address restrictions Bit 0: Overlapped/concurrent interleaving support	–	1Eh
115–127	Reserved (0)	–	All 00h
Electrical parameters block			
128	I/O pin capacitance per chip enable	TBD	00h
129–130	Asynchronous timing mode support Bit[15:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0, shall be 1	MT29F256G08CBHBBJ4 MT29F512G08CEHBBJ4 MT29F1T08CMHBBJ4 MT29F2T08CUHBBM4 MT29F4T08CTHBBM5	3Fh, 00h
131–132	Reserved (0)	–	All 00h
133–134	^{t}PROG Maximum PROGRAM PAGE time (µs)	–	C4h, 09h
135–136	^{t}BERS Maximum BLOCK ERASE time (µs)	–	C8h, AFh
137–138	^{t}R Maximum PAGE READ time (µs)	–	5Dh, 00h
139–140	^{t}CCS Minimum change column setup time (ns)	–	90h, 01h
141	NV-DDR timing mode support Bit[7:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0	MT29F256G08CBHBBJ4 MT29F512G08CEHBBJ4 MT29F1T08CMHBBJ4 MT29F2T08CUHBBM4 MT29F4T08CTHBBM5	3Fh

Table 20: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
142	NV-DDR2 timing mode support Bit 7: 1 = supports timing mode 7 Bit 6: 1 = supports timing mode 6 Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0	MT29F256G08CBHBBJ4 MT29F512G08CEHBBJ4 MT29F1T08CMHBBJ4 MT29F2T08CUHBBM4 MT29F4T08CTHBBM5	FFh
143	NV-DDR/NV-DDR2 features Bit[7:4]: Reserved (0) Bit 3: 0 = device does not require V_{PP} enablement sequence Bit 2: 1 = devices support CLK stopped for data input Bit 1: 1 = typical capacitance values present Bit 0: 0 = use ^{t}CAD MIN value	–	02h
144–145	CLK input pin capacitance, typical	TBD	00h, 00h
146–147	I/O pin capacitance, typical	TBD	00h, 00h
148–149	Input capacitance, typical	TBD	00h, 00h
150	Input pin capacitance, maximum	TBD	00h
151	Driver strength support Bit[7:3]: Reserved (0) Bit 2: 1 = Supports 18 Ohm drive strength Bit 1: 1 = Supports 25 Ohm drive strength Bit 0: 1 = Supports driver strength settings	MT29F256G08CBHBBJ4 MT29F512G08CEHBBJ4 MT29F1T08CMHBBJ4 MT29F2T08CUHBBM4 MT29F4T08CTHBBM5	03h
152–153	^{t}R maximum interleaved (multi-plane) page read time (µs)	–	75h, 00h
154-155	^{t}ADL program page register clear enhancement value (ns)	–	96h, 00h
156–157	Reserved (0)	–	All 00h
158	NV-DDR2/3 features Bit[7:6]: Reserved (0) Bit 5: 0 = external V_{REFQ} not required for >= 200MT/s Bit 4: 1 = supports differential signaling for DQS Bit 3: 1 = supports differential signaling for RE# Bit 2: 1 = supports ODT value of 30 ohms Bit 1: 1 = supports matrix termination ODT Bit 0: 1 = supports self-termination ODT	MT29F256G08CBHBBJ4 MT29F512G08CEHBBJ4 MT29F1T08CMHBBJ4 MT29F2T08CUHBBM4 MT29F4T08CTHBBM5	1Bh
159	NV-DDR2/3 warmup cycles Bit[7:4]: Data input warmup cycles support Bit[3:0]: Data ouput warmup cycles support	–	44h

Table 20: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
160–161	NV-DDR3 timing mode support Bit [15:8]: Reserved (0) Bit 7: 1 = supports timing mode 10 Bit 6: 1 = supports timing mode 9 Bit 5: 1 = supports timing mode 8 Bit 4: 1 = supports timing mode 7 Bit 3: 1 = supports timing mode 6 Bit 2: 1 = supports timing mode 5 Bit 1: 1 = supports timing mode 4 Bit 0: 1 = supports timing mode 0 to 3	MT29F256G08CBHBBJ4 MT29F512G08CEHBBJ4 MT29F1T08CMHBBJ4 MT29F2T08CUHBBM4 MT29F4T08CTHBBM5	3Fh, 00h
162	NV-DDR2 timing mode support Bit [7:3]: Reserved (0) Bit 2: 1 = supports timing mode 10 Bit 1: 1 = supports timing mode 9 Bit 0: 1 = supports timing mode 8	MT29F256G08CBHBBJ4 MT29F512G08CEHBBJ4 MT29F1T08CMHBBJ4 MT29F2T08CUHBBM4 MT29F4T08CTHBBM5	03h
163	Reserved (0)	–	00h
Vendor block			
164–165	Vendor-specific revision number	–	01h, 00h
166	TWO-PLANE PAGE READ support Bit[7:1]: Reserved (0) Bit 0: 1 = Support for TWO-PLANE PAGE READ	–	01h
167	Read cache support Bit[7:1]: Reserved (0) Bit 0: 0 = Does not support Micron-specific read cache function	–	00h
168	READ UNIQUE ID support Bit[7:1]: Reserved (0) Bit 0: 0 = Does not support Micron-specific READ UNIQUE ID	–	00h
169	Programmable DQ output impedance support Bit[7:1]: Reserved (0) Bit 0: 0 = No support for programmable DQ output impedance by B8h command	–	00h
170	Number of programmable DQ output impedance settings Bit[7:3]: Reserved (0) Bit [2:0] = Number of programmable DQ output impedance settings	MT29F256G08CBHBBJ4 MT29F512G08CEHBBJ4 MT29F1T08CMHBBJ4 MT29F2T08CUHBBM4 MT29F4T08CTHBBM5	03h
171	Programmable DQ output impedance feature address Bit[7:0] = Programmable DQ output impedance feature address	–	10h
172	Programmable R/B# pull-down strength support Bit[7:1]: Reserved (0) Bit 0: 1 = Support programmable R/B# pull-down strength	–	01h

Table 20: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
173	Programmable R/B# pull-down strength feature address Bit[7:0] = Feature address used with programmable R/B# pull-down strength	–	81h
174	Number of programmable R/B# pull-down strength settings Bit[7:3]: Reserved (0) Bit[2:0] = Number of programmable R/B# pull-down strength settings	–	04h
175	OTP mode support Bit[7:2]: Reserved (0) Bit 1: 1 = Supports Get/Set Features command set Bit 0: 0 = Does not support A5h/A0h/AFh OTP command set	–	02h
176	OTP page start Bit[7:0] = Page where OTP page space begins	–	03h
177	OTP DATA PROTECT address Bit[7:0] = Page address to use when issuing OTP DATA PROTECT command	–	01h
178	Number of OTP pages Bit[15:5]: Reserved (0) Bit[4:0] = Number of OTP pages	–	1Dh
179	OTP Feature Address	–	90h
180	Read Retry Options Bit[7:4]: Reserved (0) Bit[3:0] = Number of Read Retry options supported	–	10h
181–184	Read Retry Options available. A value of '1' in a bit position shows that Read Retry option is available for use. A value of '0' in a bit position shows that Read Retry option is not available for use. For example, the binary value of '37h, 00h, 00h, 00h' would represent that Read Retry options 0, 1, 2, 4, and 5 are available which would correspond to Read Retry input option selections of 00h, 01h, 02h, 04h, and 05h. It furthermore would show that Read Retry options 3, 6, and 7 to 32 which would correspond to Read Retry input option selections 03h, 06h, 07h to 20h, are not available.	–	FFh, FFh, 00h, 00h
185–249	Reserved (0)	–	All 00h
250–252	Designator Bytes 1 to 3 (ASCII characters) Byte 250 = Designator Byte 1, "R", Byte 251 = Designator Byte 2 Byte 252 = Designator Byte 3	–	52h, 00h, 00h
253	Parameter page revision	–	02h

Table 20: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
254–255	Integrity CRC	MT29F256G08CBHBBJ4	B5h, 64h
		MT29F512G08CEHBBJ4	AEh, B6h
		MT29F1T08CMHBBJ4	8Dh, 20h
		MT29F2T08CUHBBM4	2Dh, 20h
		MT29F4T08CTHBBM5	E2h, 43h
Redundant parameter pages			
256–511	Value of bytes 0–255	–	See bytes 0–255
512–767	Value of bytes 0–255	–	See bytes 0–255
...	...	–	...
15,104–15,359	Value of bytes 0–255	–	See bytes 0–255
15,360–15,615	Value of bytes 0–255	–	See bytes 0–255
Extended parameter pages			
15,616–15,617	Extended parameter page Integrity CRC	–	A9h, E0h
15,618–15,621	Extended parameter page signature Byte 0: 45h, "E" Byte 1: 50h, "P" Byte 2: 50h, "P" Byte 3: 53h, "S"	–	45h, 50h, 50h, 53h
15,622–15,631	Reserved (0)	–	All 00h
15,632	Section 0 type	–	02h
15,633	Section 0 length	–	01h
15,634–15,647	Reserved (0)	–	All 00h
15,648	Number of bits ECC correctability	–	48h
15,649	ECC codeword size	–	0Ah
15,650–15,651	Bad blocks maximum per LUN	–	94h, 00h
15,652–15,653	Block endurance	–	03h, 03h
15,654–15,663	Reserved (0)	–	All 00h
Redundant extended parameter pages			
15,664–15,711	Value of bytes 15,616–15,663	–	See bytes 15,616–15,663
15,712–15,759	Value of bytes 15,616–15,663	–	See bytes 15,616–15,663
...	...	–	...

Table 20: ONFI Parameter Page Data Structure (Continued)

Byte	Description	Device	Values
18,448–18,495	Value of bytes 15,616–15,663	–	See bytes 15,616–15,663
18,496–18,543	Value of bytes 15,616–15,663	–	See bytes 15,616–15,663
18,544 to end of page	Reserved (FFh)	–	All FFh

Table 21: JEDEC Parameter Page Defintion

Byte	Description	Device	Values
Revision Information and Features Block			
0–3	Parameter page signature Byte 0: 4Ah, "J" Byte 1: 45h, "E" Byte 2: 53h, "S" Byte 3: 44h, "D"	–	4Ah, 45h, 53h, 44h
4–5	Revision number Bit[15:3]: Reserved (0) Bit 2: 1 = supports JEDEC version 1.0 and standard revision 1.0 Bit 1: 1 = supports vendor specific parameter page Bit 0: Reserved (0)	–	06h, 00h
6–7	Features supported Bit[15:9]: Reserved (0) Bit 8: 1 = supports program page register clear enhancement Bit 7: 1 = supports external V_{PP} Bit 6: 1 = supports Toggle Mode DDR Bit 5: 1 = supports Synchronous DDR Bit 4: 1 = supports multi-plane read operations Bit 3: 1 = supports multi-plane program and erase operations Bit 2: 1 = supports non-sequential page programming Bit 1: 1 = supports multiple LUN operations Bit 0: 1 = supports 16-bit data bus width	MT29F256G08CBHBBJ4 MT29F512G08CEHBBJ4 MT29F1T08CMHBBJ4 MT29F2T08CUHBBM4 MT29F4T08CTHBBM5	B8h, 01h BAh, 01h

Table 21: JEDEC Parameter Page Defintion (Continued)

Byte	Description	Device	Values
8–10	Features supported Bit[23:11]: Reserved (0) Bit 10: 1 = supports Synchronous Reset Bit 9: 1 = supports Reset LUN (Primary) Bit 8: 1 = supports Small Data Move Bit 7: 1 = supports Multi-plane Copyback Program (Primary) Bit 6: 1 = supports Random Data Out (Primary) Bit 5: 1 = supports Read Unique ID Bit 4: 1 = supports Copyback Bit 3: 1 = supports Read Status Enhanced (Primary) Bit 2: 1 = supports Get Features and Set Features Bit 1: 1 = supports Read Cache commands Bit 0: 1 = supports Page Cache Program command	–	FFh, 07h, 00h
11–12	Secondary commands supported Bit[15:8]: Reserved (0) Bit 7: 1 = supports secondary Read Status Enhanced Bit 6: 1 = supports secondary Multi-plane Block Erase Bit 5: 1 = supports secondary Multi-plane Copyback Program Bit 4: 1 = supports secondary Multi-plane Program Bit 3: 1 = supports secondary Random Data Out Bit 2: 1 = supports secondary Multi-plane Copyback Read Bit 1: 1 = supports secondary Multi-plane Read Cache Random Bit 0: 1 = supports secondary Multi-plane Read	–	58h, 00h
13	Number of Parameter Pages	–	24h
14–31	Reserved (0)	–	All 00h
Manufacturer information block			
32–43	Device manufacturer (12 ASCII characters) Micron	–	4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h

Table 21: JEDEC Parameter Page Defintion (Continued)

Byte	Description	Device	Values
44–63	Device model (20 ASCII characters)	MT29F256G08CBHBBJ4	4Dh, 54h, 32h, 39h, 46h, 32h, 35h, 36h, 47h, 30h, 38h, 43h, 42h, 48h, 42h, 42h, 4Ah, 34h, 20h, 20h
		MT29F512G08CEHBBJ4	4Dh, 54h, 32h, 39h, 46h, 35h, 31h, 32h, 47h, 30h, 38h, 43h, 45h, 48h, 42h, 42h, 4Ah, 34h, 20h, 20h
		MT29F1T08CMHBBJ4	4Dh, 54h, 32h, 39h, 46h, 31h, 54h, 30h, 38h, 43h, 4Dh, 48h, 42h, 42h, 4Ah, 34h, 20h, 20h, 20h, 20h
		MT29F2T08CUHBBM4	4Dh, 54h, 32h, 39h, 46h, 32h, 54h, 30h, 38h, 43h, 55h, 48h, 42h, 42h, 4Dh, 34h, 20h, 20h, 20h, 20h
		MT29F4T08CTHBBM5	4Dh, 54h, 32h, 39h, 46h, 34h, 54h, 30h, 38h, 43h, 54h, 48h, 42h, 42h, 4Dh, 35h, 20h, 20h, 20h, 20h
64–69	JEDEC manufacturer ID	–	2Ch, 00h, 00h, 00h
70–71	Reserved (0)	–	All 00h
72–79	Reserved (0)	–	All 00h
Memory organization block			
80–83	Number of data bytes per page	–	00h, 40h, 00h, 00h
84–85	Number of spare bytes per page	–	A0h, 08h
86–89	Number of data bytes per partial page	–	00h, 04h, 00h, 00h
90–91	Number of spare bytes per partial page	–	8Ah, 00h
92–95	Number of pages per block	–	00h, 04h, 00h, 00h
96–99	Number of blocks per LUN	–	90h, 08h, 00h, 00h
100	Number of LUNs per chip enable	MT29F256G08CBHBBJ4	01h
		MT29F512G08CEHBBJ4	
		MT29F1T08CMHBBJ4	
		MT29F2T08CUHBBM4	02h
		MT29F4T08CTHBBM5	
101	Number of address cycles Bit[7:4]: Column address cycles Bit[3:0]: Row address cycles	–	23h

Table 21: JEDEC Parameter Page Defintion (Continued)

Byte	Description	Device	Values
102	Number of bits per cell	–	02h
103	Number of programs per page	–	01h
104	Multi-plane operation addressing Bit[7:4]: Reserved (0) Bit[3:0]: Number of plane address bits	–	02h
105	Multi-plane operation attributes Bit[7:3]: Reserved (0) Bit 2: 1 = Address restrictions for cache operations Bit 1: 1 = Read cache operations supported Bit 0: 1 = Program cache operations supported	–	07h
106-143	Reserved (0)	–	All 00h
Electrical parameters block			
144–145	Asynchronous SDR speed grade support Bit[15:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0, shall be 1	MT29F256G08CBHBBJ4 MT29F512G08CEHBBJ4 MT29F1T08CMHBBJ4 MT29F2T08CUHBBM4 MT29F4T08CTHBBM5	3Fh, 00h
146–147	Synchronous DDR2 speed grade support Bit[15:8]: Reserved (0) Bit 7: 1 = supports timing mode 7 Bit 6: 1 = supports timing mode 6 Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0, shall be 1	MT29F256G08CBHBBJ4 MT29F512G08CEHBBJ4 MT29F1T08CMHBBJ4 MT29F2T08CUHBBM4 MT29F4T08CTHBBM5	FFh, 00h
148–149	Synchronous DDR speed grade support Bit[15:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0, shall be 1	MT29F256G08CBFBEJ4 MT29F512G08CEFBEJ4 MT29F1T08CMFBEJ4 MT29F2T08CUFBEM4 MT29F4T08CTFBEM5	3Fh, 00h
150	Asynchronous SDR features Bit[7:0]: Reserved (0)	–	00h
151	Reserved (0)	–	00h
152	Synchronous DDR features Bit[7:2]: Reserved (0) Bit 1: 1 = devices leave CLK running for data input Bit 0: 0 = use ^{t}CAD MIN value	–	00h

Table 21: JEDEC Parameter Page Defintion (Continued)

Byte	Description	Device	Values
153–154	^{t}PROG Maximum PROGRAM PAGE time (µs)	–	C4h, 09h
155–156	^{t}BERS Maximum BLOCK ERASE time (µs)	–	C8h, AFh
157–158	^{t}R Maximum PAGE READ time (µs)	–	5Dh, 00h
159–160	^{t}R Maximum Multi-PLANE PAGE READ time (µs)	–	75h, 00h
161–162	^{t}CCS Minimum change column setup time (ns)	–	90h, 01h
163–164	I/O pin capacitance, typical	TBD	00h, 00h
165–166	Input capacitance, typical	TBD	00h, 00h
167–168	CLK input pin capacitance, typical	TBD	00h, 00h
169	Driver strength support Bit[7:3]: Reserved (0) Bit 2: 1 = Supports 18 Ohm drive strength Bit 1: 1 = Supports 25 Ohm drive strength Bit 0: 1 = Supports driver strength settings	MT29F256G08CBHBEJ4	03h
		MT29F512G08CEHBEJ4	
		MT29F1T08CMHBEJ4	
		MT29F2T08CUHBEM4	
		MT29F4T08CTHBEM5	
170–171	^{t}ADL program page register clear enhancement value (ns)	–	96h, 00h
172–207	Reserved (0)	–	All 00h
ECC and endurance block			
208	Guaranteed valid blocks at beginning of target	–	01h
209–210	Block endurance for guaranteed valid blocks	–	00h, 00h
211	Number of bits ECC correctability	–	48h
212	ECC codeword size	–	0Ah
213–214	Bad blocks maximum per LUN	–	94h, 00h
215–216	Block endurance	–	03h, 03h
217–218	Reserved (0)	–	All 00h
219–271	Reserved (0)	–	All 00h
Reserved			
272–419	Reserved (0)	–	All 00h
Vendor specific block			
420–421	Vendor-specific revision number	–	02h, 00h
422	Read Retry Options Bit[7:4]: Reserved (0) Bit[3:0] = Number of Read Retry options supported	–	10h

Table 21: JEDEC Parameter Page Defintion (Continued)

Byte	Description	Device	Values
423–426	Read Retry Options available. A value of '1' in a bit position shows that Read Retry option is available for use. A value of '0' in a bit position shows that Read Retry option is not available for use. For example, the binary value of '37h, 00h, 00h, 00h' would represent that Read Retry options 0, 1, 2, 4, and 5 are available which would correspond to Read Retry input option selections of 00h, 01h, 02h, 04h, and 05h. It furthermore would show that Read Retry options 3, 6, and 7 to 32 which would correspond to Read Retry input option selections 03h, 06h, 07h to 20h, are not available.	–	FFh, FFh, 00h, 00h
427–429	Designator Bytes 1 to 3 (ASCII characters) Byte 250 = Designator Byte 1, "R", Byte 251 = Designator Byte 2 Byte 252 = Designator Byte 3	–	52h, 00h, 00h
430–509	Reserved (0)	–	All 00h
CRC for Parameter Page			
510–511	Integrity CRC	MT29F256G08CBHBBJ4	18h, E0h
		MT29F512G08CEHBBJ4	0Fh, 10h
		MT29F1T08CMHBBJ4	FEh, 8Ah
		MT29F2T08CUHBBM4	7Eh, 22h
		MT29F4T08CTHBBM5	E9h, DFh
Redundant JEDEC Parameter Pages			
512–1023	See byte values 0–511	–	See bytes 0–511
1024–1535	See byte values 0–511	–	See bytes 0–511
...	...	–	...
17,408–17,919	See byte values 0–511	–	See bytes 0–511
17,920–18,431	See byte values 0–511	–	See bytes 0–511
18,432 to end of page	Reserved (FFh)	–	All FFh

Note: 1. h = hexadecimal.

READ UNIQUE ID (EDh)

The READ UNIQUE ID (EDh) command is used to read a unique identifier programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

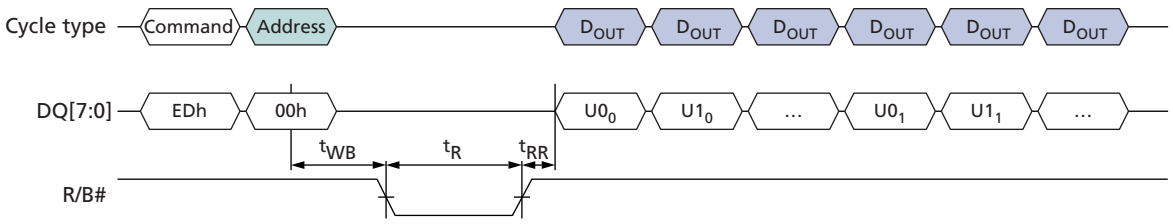
Writing EDh to the command register puts the target in read unique ID mode. The target stays in this mode until another valid command is issued.

When the EDh command is followed by a 00h address cycle, the target goes busy for ^{t}R. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode.

After ^{t}R completes, the host enables data output mode to read the unique ID. When the asynchronous interface is active, one data byte is output per RE# toggle. When the synchronous interface is active, two data bytes are output, one byte for each rising or falling edge of DQS.

Sixteen copies of the unique ID data are stored in the device. Each copy is 32 bytes. The first 16 bytes of a 32-byte copy are unique data, and the second 16 bytes are the complement of the first 16 bytes. The host should XOR the first 16 bytes with the second 16 bytes. If the result is 16 bytes of FFh, then that copy of the unique ID data is correct. In the event that a non-FFh result is returned, the host can repeat the XOR operation on a subsequent copy of the unique ID data. If desired, the CHANGE READ COLUMN (05h-E0h) command can be used to change the data output location. Use of the CHANGE READ COLUMN ENHANCED (06h-E0h) command is prohibited.

Figure 54: READ UNIQUE ID (EDh) Operation



Configuration Operations

The SET FEATURES (EFh) and GET FEATURES (EEh) commands are used to modify the target's default power-on behavior. These commands use a one-byte feature address to determine which subfeature parameters will be read or modified. Each feature address (in the 00h to FFh range) is defined in . The The SET FEATURES (EFh) or SET FEATURES by LUN (D5h) commandwrites subfeature parameters (P1-P4) to the specified feature address. The GET FEATURES (EEh) or GET FEATURES by LUN (D4h) command reads the subfeature parameters (P1-P4) at the specified feature address.

Unless otherwise specified, the values of the feature addresses do not change when RESET (FAh, FFh, FCh) is issued by the host. A HARD RESET (FDh) command will reset all feature addresses to their default values for the target LUN. A HARD RESET (FDh) command will not undo any previously set Electronic Mirroring, CE# Pin Reduction, or Volume Addressing assignments that were performed prior to the HARD RESET (FDh) command.

Table 22: Feature Address Definitions

Feature Address	Definition
00h	Reserved
01h	Timing mode
02h	NV-DDR2 and NV-DDR3 configuration
03h–0Fh	Reserved
10h	Programmable output drive strength
11h–2Fh	Reserved
30h	V_{PP} configuration
31h–57h	Reserved
58h	Volume configuration
59h–7Fh	Reserved
80h	Programmable output drive strength
81h	Programmable R/B# pull-down strength
82h–88h	Reserved
89h	Read Retry
8Ah–8Fh	Reserved
90h	Array operation mode
91h–E5h	Reserved
E6h	Sleep mode
E7h	Temperature sensor
E8h–F4h	Reserved
F5h	Snap Read / Express Read
F6h	Sleep Lite
F7h–FFh	Reserved

SET FEATURES (EFh)

The SET FEATURES (EFh) command writes the subfeature parameters (P1-P4) to the specified feature address to enable or disable target-specific features. This command is accepted by the target only when all die (LUNs) on the target are idle.

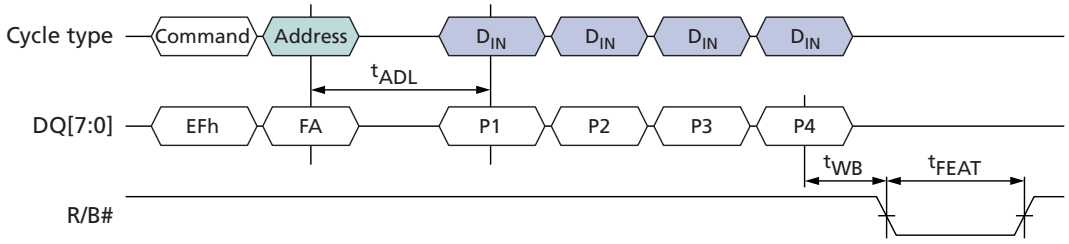
Writing EFh to the command register puts the target in the set features mode. The target stays in this mode until another command is issued.

The SET FEATURES (EFh) command is followed by a valid feature address as specified in . The host waits for ^{t}ADL before the subfeature parameters are input. When the asynchronous interface is active, one subfeature parameter is latched per rising edge of WE#. When the NV-DDR, NV-DDR2, or NV-DDR3 interface is active, one subfeature parameter is latched per rising edge of DQS_t. The data on the falling edge of DQS_t should be identical to the subfeature parameter input on the previous rising edge of DQS_t. The device is not required to wait for the repeated data byte before beginning internal actions.

After all four subfeature parameters are input, the target goes busy for ^{t}FEAT, unless otherwise specified. The READ STATUS (70h) command can be used to monitor for command completion.

Feature address 01h (Timing mode) operation is unique. If SET FEATURES is used to modify the interface type, the target will be busy for ^{t}ITC. See Activating Interfaces (page 72) for details.

Figure 55: SET FEATURES (EFh) Operation



GET FEATURES (EEh)

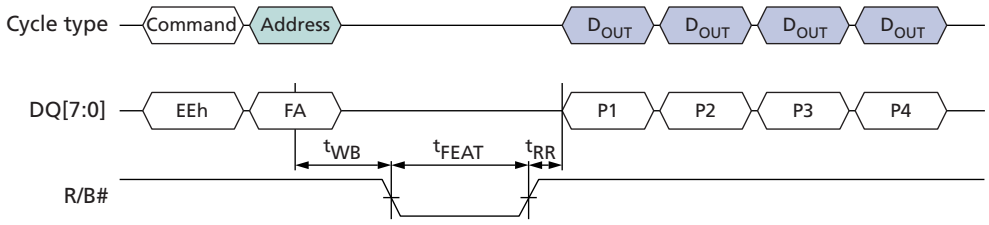
The GET FEATURES (EEh) command reads the subfeature parameters (P1-P4) from the specified feature address. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing EEh to the command register puts the target in get features mode. The target stays in this mode until another valid command is issued.

When the GET FEATURES (EEh) command is followed by a feature address, the target goes busy for ^{t}FEAT, unless otherwise specified. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode. During and prior to data output, use of the READ STATUS ENHANCED (78h) command is prohibited.

After ^{t}FEAT completes, the host enables data output mode to read the subfeature parameters. When the asynchronous interface is active, one data byte is output per RE_# toggle. When the NV-DDR, NV-DDR2, or NV-DDR3 interface is active, one subfeature parameter is output per DQS_t toggle on rising or falling edge of DQS_t.

Figure 56: GET FEATURES (EEh) Operation



GET/SET FEATURES by LUN (D4h/D5h)

The original GET FEATURES (EEh) and SET FEATURES (EFh) commands were target (CE#) based operations that did not take into account LUN addressing. By that, setting a feature address or getting a value for a feature address for a given target (CE#) applied to all LUNs on that target (CE#). GET FEATURES by LUN (D4h) and SET FEATURES by LUN (D5h) commands have the ability to also select a LUN address gives added flexibility to set the same feature address to different values for each LUN on a target (CE#) for more complex and versatile system solutions.

GET FEATURES by LUN (D4h) and SET FEATURES by LUN (D5h) operations work in the same manner as the non-LUN versions of those commands that did not take LUN addressing into account. The GET FEATURES by LUN (D4h) and SET FEATURES by LUN (D5h) commands both have an added LUN address cycle that is before the address cycle of the feature address which denotes the LUN to select for the operation. See (page 0) for the decode of the LUN address cycle.

Table 23: GET/SET FEATURES by LUN Operation LUN address cycle decoding

Description	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
LUN											
LUN selection	LUN0								0	0b	
	LUN1								1	1b	
Reserved	–	–	–	–	–	–	–	–			

GET FEATURES by LUN (D4h) and SET FEATURES by LUN (D5h) can be issued to any addressable LUN that is not busy (RDY = 1, ARDY = 1). Target LUN status can be determined by using the READ STATUS ENHANCED (78h) command. When doing multiple LUN operations, refer to the Interleaved Die (Mutli-LUN) Operation section for details on proper operations.

Figure 57: GET FEATURES by LUN (D4h) Operation

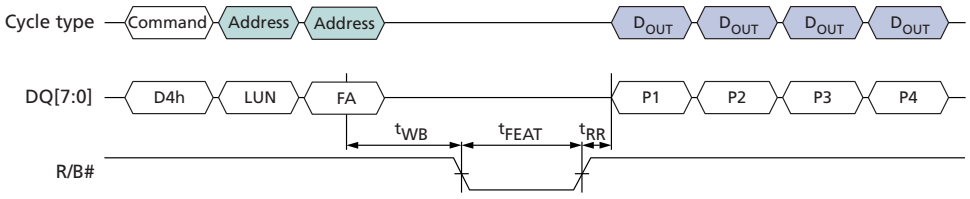


Figure 58: SET FEATURES by LUN (D5h) Operation

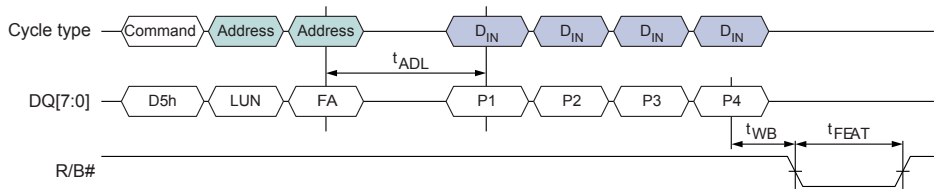


Table 24: Feature Address 01h: Timing mode

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Timing mode	Mode 0 (default)					0	0	0	0	x0h	1, 2
	Mode 1					0	0	0	1	x1h	
	Mode 2					0	0	1	0	x2h	
	Mode 3					0	0	1	1	x3h	
	Mode 4					0	1	0	0	x4h	
	Mode 5					0	1	0	1	x5h	
	Mode 6					0	1	1	0	x6h	
	Mode 7					0	1	1	1	x7h	
	Mode 8					1	0	0	0	x8h	
	Mode 9					1	0	0	1	x9h	
	Mode 10					1	0	1	0	xAh	
	Reserved					1	x	x	x	Bh–Fh	
Data interface	Asynchronous (default)			0	0					0xh	1
	NV-DDR			0	1					1xh	
	NV-DDR2			1	0					2xh	
	Reserved			1	1					3xh	
Program clear	Program command clears all cache registers on a target (default)		0							0b	
	Program command clears only the cache register of the selected plane of addressed LUN on a target		1							1b	
Reserved		0								0b	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											

Table 24: Feature Address 01h: Timing mode (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes:
1. Asynchronous timing mode 0 is the default, power-on value when the NAND device is powered-on with V_{CCQ} in the 1.8V operational range. NV-DDR3 timing mode 0 is the default, power-on value when the NAND device is powered-on with V_{CCQ} in the 1.2V operational range.
2. If the NV-DDR or NV-DDR2 interface is active, a RESET (FFh) command will change the timing mode and data interface bits of feature address 01h to their default values. If the asynchronous interface is active, a RESET (FFh) command will not change the values of the timing mode or data interface bits to their default valued. Transition from the NV-DDR interface to the NV-DDR2 interface or vice versa is not permitted. The Data interface bits have no functionality for the NV-DDR3 interface.

Table 25: Feature Address 02h: NV-DDR2 and NV-DDR3 configuration

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Voltage Reference (VEN)	External V_{REFQ} is disabled and internal voltage is used as reference for DQ signals(default)								0	0b	1, 2
	External V_{REFQ} is enabled and used as reference for DQ signals								1	1b	
Complementary DQS (CMPD)	DQS_c signal disabled (default)							0		0b	
	DQS_c signal enabled							1		1b	
Complementary RE# (CMPR)	RE_c signal disabled (default)						0			0b	
	RE_c signal enabled						1			1b	
Reserved	-					0				0b	

Table 25: Feature Address 02h: NV-DDR2 and NV-DDR3 configuration (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
DQ[7:0],DQS_t, DQS_c, RE_t, and RE_c ODT enable	ODT disabled (default)	0	0	0	0					0h	3
	ODT enabled with R_{TT} of 150 Ohms	0	0	0	1					1h	
	ODT enabled with R_{TT} of 100 Ohms	0	0	1	0					2h	
	ODT enabled with R_{TT} of 75 Ohms	0	0	1	1					3h	
	ODT enabled with R_{TT} of 50 Ohms	0	1	0	0					4h	
	Reserved	0	1	0	1					5h	
		0	1	1	0					6h	
		0	1	1	1					7h	
		1	X	X	X					8h-Fh	
P2											
Warmup RE_t/ RE_c and DQS cycles for data output	0 cycles (default)					0	0	0	0	0h	4
	1 warmup cycle					0	0	0	1	1h	
	2 warmup cycles					0	0	1	0	2h	
	4 warmup cycles					0	0	1	1	3h	
	4 warmup cycles					0	1	0	0	4h	
	Reserved					0	1	0	1	5h	
						0	1	1	0	6h	
						0	1	1	1	7h	
						1	X	X	X	8h-Fh	
Warmup DQS cycles for data input	0 cycles (default)	0	0	0	0					0h	5
	1 warmup cycle	0	0	0	1					1h	
	2 warmup cycles	0	0	1	0					2h	
	4 warmup cycles	0	0	1	1					3h	
	4 warmup cycles	0	1	0	0					4h	
	Reserved	0	1	0	1					5h	
		0	1	1	0					6h	
		0	1	1	1					7h	
		1	X	X	X					8h-Fh	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											

Table 25: Feature Address 02h: NV-DDR2 and NV-DDR3 configuration (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Reserved		0	0	0	0	0	0	0	0	00h	

Notes:
1. If set to one, then external V_{REFQ} is used as a reference for the input and I/O signals. If cleared to zero, then internal V_{REFQ} is used as a reference for the input and I/O signals. This setting applies to input and I/O signals, including DQ[7:0], DQS_t, DQS_c, RE_t, RE_c, WE#, ALE, and CLE. CE# and WP# are CMOS signals and always use internal V_{REFQ}.
2. If the NV-DDR3 interface is active, a RESET (FFh) command will not change the bit values of feature address 02h to their default values. If the NV-DDR2 interface is active, a RESET (FFh) command will change the bit values feature address 02h to their default values.
3. This field controls the on-die termination settings for the DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c signals. R_{TT} settings may be specified separately for DQ[7:0]/DQS and the RE# signals. The DQ[7:0]/DQS may be specified separately for data input versus data output operation. Refer to the definition of the ODT CONFIGURE (E2h) command. If values are specified with the ODT CONFIGURE (E2h) command, then this field is not used. GET FEATURES (EEh) returns the previous value set in this field, regardless of the R_{TT} settings specified using ODT CONFIGURE (E2h).
4. Number of warmup cycles for DQS and RE_t/RE_c and DQS_t/DQS_c for data output. The number of initial "dummy" RE_t/RE_c cycles at the start of data output operations. There are corresponding "dummy" DQS_t/DQS_c cycles to the "dummy" RE_t/RE_c cycles that the host shall ignore during data output.
5. This field indicates the number of warmup cycles of DQS that are provided for data input. These are the number of initial "dummy" DQS_t/DQS_c cycles at the start of data input operations.

Table 26: Feature Address 30h: V_{PP}

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
External V_{PP} configuration	Disabled (default)								0	00h	
	Enabled								1	01h	1
Reserved		0	0	0	0	0	0	0		00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Note:
1. This setting controls whether external V_{PP} is enabled. This setting is retained across RESET (FAh, FCh, FFh) commands. A HARD RESET (FDh) command will disable the V_{PP} feature and clear the V_{PP} feature address back to its default value for the target LUN.

Table 27: Feature Address 58h: Volume configuration

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Volume Address	Field used to assign a value for a given Volume Address					X	X	X	X		1
Reserved	-	0	0	0	0					0h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Note: 1. After the Volume Address is appointed, the ENo pin for that Volume is set to one, the ENi pin for that Volume is ignored until the next power cycle, and the Volume is deselected until a VOLUME SELECT (E1h) command is issued that selects the associated Volume. The host shall only set this feature once per power cycle for each Volume. The address specified is then used in VOLUME SELECT (E1h) command for accessing this NAND Target. This setting is retained across RESET (FAh, FCh, FFh) commands. A HARD RESET (FDh) command will not undo any previously set Volume Addressing assignments that were performed prior to the HARD RESET (FDh) command.

Table 28: Feature Addresses 10h and 80h: Programmable Output Drive Strength

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Output drive strength	Not supported							0	0	00h	1
	25 Ohms							0	1	01h	
	35 Ohms (default)							1	0	02h	
	50 Ohms							1	1	03h	
Reserved		0	0	0	0	0	0			00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Note: 1. See Output Drive Impedance for details.

Table 29: Feature Address 81h: Programmable R/B# Pull-Down Strength

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
R/B# pull-down strength	Full (default)							0	0	00h	1
	Three-quarter							0	1	01h	
	One-half							1	0	02h	
	One-quarter							1	1	03h	
Reserved		0	0	0	0	0	0			00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Note: 1. This feature address is used to change the default R/B# pull-down strength. Its strength should be selected based on the expected loading of R/B#. Full strength is the default, power-on value.

Table 30: Feature Addresses 89h: Read Retry

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Read Retry	Disable (default)					0	0	0	0	00h	
	Option 1					0	0	0	1	01h	
	Option 2					0	0	1	0	02h	
	Option 3					0	0	1	1	03h	
	Option 4					0	1	0	0	04h	
	Option 5					0	1	0	1	05h	
	Option 6					0	1	1	0	06h	
	Option 7					0	1	1	1	07h	
	Option 8					1	0	0	0	08h	2
	Option 9					1	0	0	1	09h	
	Option 10					1	0	1	0	0Ah	
	Option 11					1	0	1	1	0Bh	
	Option 12					1	1	0	0	0Ch	
	Option 13					1	1	0	1	0Dh	
	Option 14					1	1	1	0	0Eh	
	Option 15					1	1	1	1	0Fh	
Reserved		0	0	0	0					00h	

Table 30: Feature Addresses 89h: Read Retry (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes:
1. See Read Retry Operation for details.
2. ^{t}R will be longer with selected option. See Electrical Specifications - Array Characteristics section for details.

Table 31: Feature Address 90h: Array Operation Mode

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Array Operation Mode	Normal (default)								0	00h	
	OTP Block								1	01h	1
Reserved		0	0	0	0	0	0	0		00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes:
1. See One-Time Programmable (OTP) Operations for details.
2. A RESET (FFh) command will cause the bits of the array operation mode to change to their default values. If in NV-DDR/NV-DDR2/NV-DDR3 mode, a SYNCHRONOUS RESET (FCh) command will cause the bits of the array operation mode to change to their default values. The HARD RESET (FDh) command is prohibited when not in the default array operation mode.

Table 32: Feature Address E6h: Sleep Mode

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											

Table 32: Feature Address E6h: Sleep Mode (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Sleep mode	Sleep mode disabled (default)								0	0b	
	Sleep mode enabled								1	1b	
	Sleep_V_{CCQ} mode disabled (default)							0		0b	
	Sleep_V_{CCQ} mode enabled							1		1b	
Reserved	–	–	–	–	–	–	–				
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Sleep mode is a power state in which the LUNs power consumption is minimal. Sleep_V_{CCQ} mode is a power state in which V_{CCQ} can be removed to reduce I_{SBQ}. The trade off for this functionality is longer wake up duration from the Sleep and/or Sleep_V_{CCQ} state.

The die (LUN) will retain its entire configuration (including Set Feature settings, RV level values, etc..) during Sleep mode, but does not retain the contents of the cache or data registers. During Sleep_V_{CCQ} mode the die will retain its entire configuration (including settings, RV level values, etc) and the contents of the cache or data registers.

Sleep Mode is enabled by issuing a SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to feature address E6h. After the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command is issued, the target (CE#) or target LUN will enter Sleep mode upon bringing CE# HIGH. The target (CE#) or target LUN will enter Sleep_V_{CCQ} mode when CE# is brought HIGH and V_{CCQ} is powered down. Powering down V_{CCQ} is a requirement to enter Sleep_V_{CCQ}. Both Sleep and Sleep_V_{CCQ} modes can be entered simultaneously or separately.

During Sleep mode, upon asserting CE# LOW, the LUN will exit the mode and change state to Normal mode. During Sleep_V_{CCQ} mode or when both Sleep and Sleep_V_{CCQ} modes are entered, upon asserting CE# LOW and issuing the RESET (FFh) command, the LUN will exit the current sleep mode(s) and change state to Normal mode. The transition period between Sleep Mode and Normal Mode shall be less than ^{t}SLP. After the transition, the LUN will move to Normal Ready mode and be ready to receive commands. When exiting from Sleep_V_{CCQ} mode the host is required to issue a RESET (FFh) command to the LUN. If both Sleep and Sleep_V_{CCQ} modes are entered the host is required to issue a RESET (FFh) command to the LUN and the ^{t}RST time associated with that RESET (FFh) command will be equivalent to ^{t}SLP.

For a configuration of more than one LUN sharing the same CE# (or Volume Address), if SET FEATURES (EFh) command is used to enter Sleep and/or Sleep_V_{CCQ} mode(s), the

shared LUNs shall jointly enter/exit to/from Sleep/Sleep_V_{CCQ} mode. All LUNs on a target (CE#) shall monitor in parallel the SET FEATURES (EFh) or SET FEATURE by LUN (D5h) command to enter the mode. As CE# is shared, upon asserting the signal, all LUNs on a target shall exit from Sleep Mode. Upon issuing the RESET (FFh)) command to LUNs that share a CE#, all LUNs shall exit form Sleep_V_{CCQ} (or Sleep/Sleep_V_{CCQ}) mode.

For Sleep mode, it is not required to have all targets (CE#s) of a NAND device enabled for Sleep mode. A host can have as little as LUN enabled for Sleep mode. For Sleep_V_{CCQ} mode, it is required to have all devices that share a common V_{CCQ} enabled for Sleep_V_{CCQ} mode prior to removing V_{CCQ} from the NAND device.

Once Sleep mode is entered, the host is required to keep the NAND device in Sleep mode for a minimum time of 1µs before exiting Sleep mode.

The host shall not issue any commands with exception of RESET (FFh, FAh, FCh, FDh) between issuing the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to enable Sleep mode (Feature Address E6h) and bringing CE# HIGH to enter Sleep mode. The host shall not issue any commands between issuing the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to enable Sleep_V_{CCQ} mode (i.e. Feature Address E6h, P1[1]=1) and bringing CE# HIGH and powering down V_{CCQ} to enter Sleep_V_{CCQ} mode

When V_{CCQ} = 0V, the host must keep RE_t/RE_c, DQS_t/DQS_c signals LOW. RE_t/RE_c, DQS_t/DQS_c signals maybe ramped with V_{CCQ} during power up but not exceed V_{CCQ}. When V_{CCQ} = 0V, the host must keep DQ[7:0] signals LOW or they can be left Hi-Z. DQ[7:0] signals maybe ramped with V_{CCQ} during power up but not exceed V_{CCQ}.

If a RESET (FFh, FAh, FCh, FDh) command is issued to the target (CE#) or LUN after a SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to enable Sleep mode is issued, but before CE# goes HIGH, the target (CE#) or LUN will not enter Sleep Mode upon CE# HIGH. In other words, the setting for Sleep mode is not retained across RESET (FFh, FAh, FCh, FDh) operations. If Sleep and Sleep_V_{CCQ} are both entered with SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command, no commands are allowed to be issued to the NAND until after V_{CCQ} is powered down and then powered back up. If Sleep_V_{CCQ} mode is entered with SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command, any commands issued to the NAND device, including RESET (FFh, FAh, FCh, FDh), will be ignored until after V_{CCQ} power is removed.

When exiting Sleep and/or Sleep_V_{CCQ} mode, CE# shall be asserted LOW for a minimum of ^{t}CE_SLP.

When exiting Sleep Mode, the host is required to wait ^{t}SLP before issuing any commands (including RESET) to the device. During ^{t}SLP period the device may draw significantly more current than I_{SB} even when CE# is HIGH. When exiting Sleep/Sleep_V_{CCQ} mode, the host is required to wait ^{t}SLP after issuing RESET (FFh) command to exit the mode. During this ^{t}SLP period, the device may draw significantly more current than I_{SB} even when CE# is HIGH.

Table 33: Sleep Mode parameters

Parameter	Min	Max	Units
^{t}SLP	–	50	µs
^{t}CE_SLP	–	200	ns

Table 33: Sleep Mode parameters (Continued)

Parameter	Min	Max	Units
Sleep_V_{CCQ} exit (^{t}RST)	–	10	µs
Sleep and Sleep_V_{CCQ} ext (^{t}RST)	–	50	µs
CE# LOW exiting Sleep or Sleep_V_{CCQ}	200	–	ns
V_{CCQ} time to be < 100mV during Sleep_V_{CCQ} mode	25	–	µs
$I_{SB\_SLEEP/SLEEP\_VCCQ}$	–	20	µA
I_{SBQ_SLEEP}	–	25	µA
$I_{SBQ\_SLEEP\_VCCQ}$	–	0	µA

Sleep mode entry/exit required method:

1. Issue a SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to feature address E6h with subfeature P1 = 1h to enable Sleep mode entry
2. CE# is brought HIGH after Sleep mode entry and the NAND target (CE#) enters Sleep mode
3. CE# is brought LOW to exit Sleep mode. Sleep mode entry is cleared (i.e. DQ0 of subfeature P1 of feature address E6h is automatically cleared).
4. During the ^{t}SLP time allowed for the NAND target to return to normal mode from Sleep mode. no commands (including RESET) are allowed to the target.
5. To re-enter Sleep mode the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to feature address E6h with subfeature P1 = 1h to enable Sleep mode entry must be issued again.

Sleep_VCCQ entry/exit required method:

1. Issue a SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to feature address E6h with subfeature P1 = 2h to enable Sleep_V_{CCQ} mode entry
2. CE# is brought HIGH and then V_{CCQ} is removed after Sleep_V_{CCQ} mode entry has been selected and the device enters Sleep_V_{CCQ} mode. Once the host issues SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to feature address E6h to enter Sleep_V_{CCQ} mode, the host must execute a power cycle on V_{CCQ} before any command may be entered. User is required bring V_{CCQ} below 100mV for at least 25µs. While V_{CCQ} is powered down R/B#, DQs, and DQS signals shall be left floating or cannot be driven higher than 0V.
3. V_{CCQ} is powered on. When powering up V_{CCQ}, the host is required to follow V_{CCQ} power on requirements and no input signal transitions shall occur when ramping V_{CCQ} and V_{CCQ} < 0.85V. The device stays in the interface configured when Sleep_V_{CCQ} mode was entered.
4. The host shall issue a RESET (FFh) command to the NAND device to exit Sleep_V_{CCQ} mode. The Sleep_V_{CCQ} mode entry is cleared (i.e. the SET Feature Bit for Sleep mode entry is automatically cleared). The ^{t}RST time for the RESET (FFh) command is within ^{t}RST (i.e. no NAND trims are loaded as they were maintained during Sleep_V_{CCQ} mode).

5. To re-enter Sleep_V_{CCQ} mode the the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to feature address E6h with subfeature P1 = 2h to enabled Sleep_V_{CCQ} mode entry must be issued again.

Sleep and Sleep_VCCQ entry/exit required method:

1. Issue a SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to feature address E6h with subfeature P1 = 3h to enable Sleep and Sleep_V_{CCQ} mode entry
2. CE# is brought HIGH and then V_{CCQ} is removed after Sleep/Sleep_V_{CCQ} Mode entry and the device enters both Sleep and Sleep_V_{CCQ} Mode. Once the user issues SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to enter Sleep/Sleep_V_{CCQ} Mode, the host must execute a power cycle on V_{CCQ} before any command may be entered. The host is required bring V_{CCQ} below 100mV for at least 1µs. While V_{CCQ} is powered down R/B#, DQs, and DQS signals shall be left floating or cannot be driven higher than 0V.
3. To exit Sleep and Sleep_V_{CCQ} mode, V_{CCQ} is powered on. When powering up V_{CCQ}, the host is required to follow V_{CCQ} power on requirements and no input signal transitions shall occur when ramping V_{CCQ} and V_{CCQ} < 0.85V. The device stays in the interface configured when Sleep/Sleep_V_{CCQ} was entered.
4. The host shall issue a RESET (FFh) command to all targets (CE#s) of the NAND device to exit Sleep_V_{CCQ} Mode. The Sleep_V_{CCQ} mode entry is cleared (i.e. the SET Feature Bit for Sleep mode entry is automatically cleared). The tRST time for the RESET (FFh) command is up to ^{t}SLP (i.e. no NAND trims are loaded as they were maintained during Sleep/Sleep_V_{CCQ} mode).
5. During the ^{t}SLP time allowed for the NAND target to return to normal mode from Sleep/Sleep_VCCQ mode. no commands (including RESET) are allowed to the target.
6. To re-enter Sleep/Sleep_V_{CCQ} mode the the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to feature address E6h with subfeature P1 = 3h to enabled Sleep/Sleep_V_{CCQ} mode entry must be issued again.

Table 34: Feature Address E7h: Temperature Sensor Readout

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Temperature Sensor Readout	-37°C example output		0	0	0	0	0	0	0	00h	1, 2
	-35.8°C example output		0	0	0	0	0	0	1	01h	
	–		X	X	X	X	X	X	X	–	
	89°C example output		1	1	0	1	0	0	1	69h	
	90.2°C example output		1	1	0	1	0	1	0	6Ah	
	Reserved		–	–	–	–	–	–	–	6Bh–7Fh	
Reserved		0								0b	
P2											

Table 34: Feature Address E7h: Temperature Sensor Readout (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes:
1. Each bit is roughly 1.2°C. For example, an output of 55h is roughly 65°C.
2. Device reading out temperature beyond specified operational temperature ranges for a given device is not meant to signify support of those temperatures.

Only a GET FEATURES (EEh) or GET FEATURES by LUN (D4h) commands are permitted to feature address E7h, SET FEATURES (EFh) and SET FEATURES by LUN (D5h) commands are not supported to feature address E7h. The temperature sensor shall return the current temperature value no more than ^{t}TEMP after the host controller issues the GET FEATURES (EEh) or GET FEATURES by LUN (D4h) command to feature address E7h. GET FEATURES (EEh) and GET FEATURES by LUN (D4h) commands are not supported to feature address E7h when the target (CE#) or target LUN is in any busy state.

If there is only 1 LUN per CE# of a NAND device, then either the GET FEATURES (EEh) or GET FEATURES by LUN (D4h) command can be used to access the Temperature Sensor Readout (Feature Address E7h). If there is more than one LUN per CE#, then the GET FEATURES by LUN (D4h) command shall be used to access the Temperature Sensor Readout (Feature Address E7h), not the GET FEATURES (EEh) command, to avoid possible data contention.

Table 35: Feature Address F5h: Snap Read / Express Read

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Snap Read/ Express Read Enable	Reserved								0	0b	
	Snap Read / Express Read disable (default)						0	0		00b	
	Express Read enable						0	1		01b	
	Reserved						1	0		10b	
	Snap Page Read enable						1	1		11b	
	Reserved	0	0	0	0	0				00000b	
P2											
Partial Page Length (LSB)	Lower 8 Bits of Partial Page Length	1	0	0	0	1	1	0	0	8Ch	1

Table 35: Feature Address F5h: Snap Read / Express Read (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P3											
Partial Page Length (MSB)	Upper 8 Bits of Partial Page Length	0	0	0	1	1	0	1	0	14h	1
P4											
Reserved	–	0	0	0	0	0	0	0	0	00h	

Note: 1. Subfeature P2 = 8Ch and subfeature P3 = 14h have partial page length of 5,260 bytes required for Snap Read. For Express Read, the subfeatures P2 and P3 bytes are "don't care".

Feature Address F5h: Snap Read / Express Read controls two different feature configurations. The Snap Read Feature provides fastest possible read of a partial page. The Express Read Feature allows the host to begin clocking out data before the read command has fully completed, also allowing for faster ^{t}R for Read operations with internal NAND Randomizer disabled. A Snap Read includes Express read functionality.

Note that Snap Read cannot be used in conjunction with the NAND internal data randomizer. If performing a Snap Read from a page that has been programmed with the NAND internal randomizer enabled, indeterminate data will be output.

The Snap Read requires the host to define a partial page length subsection of 5,260 bytes. The partial page length is determined by the values entered into sub-feature parameters P2 and P3 of the Feature Address F5h: Snap Read / Express Read. The desired number of bytes to be read is converted into binary format, and then the lower eight bits are entered into subfeature P2 and the upper 8 bits are entered into subfeature P3. When Snap Read is enabled the host must enter a value of 8Ch for subfeature P2 and 14h for subfeature P3 corresponding to a partial page length of 5,260 bytes.

When a Snap Read is issued, the byte address specified by the command will determine the starting byte for the partial page read and the end address of the partial page will be determined by the start byte address plus the partial page length minus one. When using the NV-DDR2 interface, CA0 is forced to 0 internally, so start byte address is always an even byte. If the "start byte address plus partial page length minus one" range exceeds the maximum page width, the maximum column address will be used as the valid data end address. Data will be invalid for any bytes not included in the range of byte addresses specified by the partial page read operation. In the event that a partial page length of 0 is entered then all data bytes will be invalid.

Snap read is only performed if enabled and if READ PAGE (00h-30h) command is issued to the device. If READ PAGE CACHE RANDOM (00h-31h), READ PAGE CACHE SEQUENTIAL (31h), READ PAGE CACHE LAST (3Fh), READ PAGE MULTI-PLANE (00h-32h), or FEATURE ADDRESS 89h: READ RETRY options selected that has a longer ^{t}R time are issued to the device, the Snap Read is not executed and the command issued is executed.

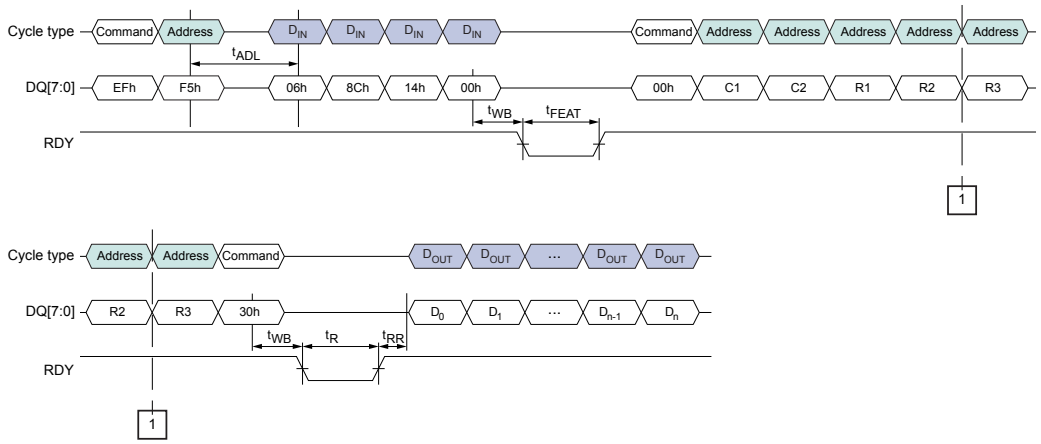
Snap Read is not supported if reading from a non-fully programmed WL (i.e. shared pages programmed). If Snap Read is performed on a partially programmed WL undetermined data will result.

Snap Read is supported in Erase Suspend or Program Suspend state.

Snap Read should not be used to check for Bad Blocks when building a Bad Block Table. If READ UNIQUE ID (EDh), READ OTP PAGE, or READ PARAMETER PAGE (ECh) commands are issued to the device when Snap Read is enabled, Snap Read is not executed and the READ UNIQUE ID (EDh), READ OTP PAGE, or READ PARAMETER PAGE (ECh) commands are executed.

Snap Read incorporates the Express Read feature, so any Express Read requirements must also be met for Snap Read.

Figure 59: Example of Snap Page Read Sequence



Note: 1. Byte address of data byte D_n is defined by the starting column address specified by C1 and C2 plus the partial page length defined by P2 and P3.

The Express Read Feature allows the host to begin clocking data out of the part once the data in the data register becomes valid. This will happen before the entire read algorithm is completed, thus reducing the apparent ^{t}R time for Read operations with internal NAND Randomizer disabled. Before any additional array commands can be issued the entire read algorithm must be completed.

When the Express Read Feature is enabled the host must monitor the Status Register using either READ STATUS (70h) or READ STATUS ENHANCED (78h) commands. Status Register bit 6 (RDY) will provide a method for the host to determine when data can begin being clocked out of the device. Status Register bit 5 (ARDY) will remain low until the entire read algorithm has been completed. The host must not issue any additional array operations until Status Register bit 5 (ARDY) is ready. In addition to Read Status (70h/78h) and RESET (FFh/FCh/FAh) commands, the host is allowed to issue CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) when Status Register bit 5 (ARDY) is LOW and Status Register bit 6 (RDY) is HIGH during Express Read.

Express Read may be enabled for any read command, but in some cases Express Read will not be executed and no ^{t}R improvement witnessed. If Express Read is enabled during READ PAGE CACHE RANDOM (00h-31h), READ PAGE CACHE SEQUENTIAL (31h), READ PAGE CACHE LAST (3Fh), or FEATURE ADDRESS 89h: READ RETRY options selected that has a longer ^{t}R time, Express Read will not be executed and no ^{t}R improvement witnessed.

Figure 60: Example of Express Read Sequence

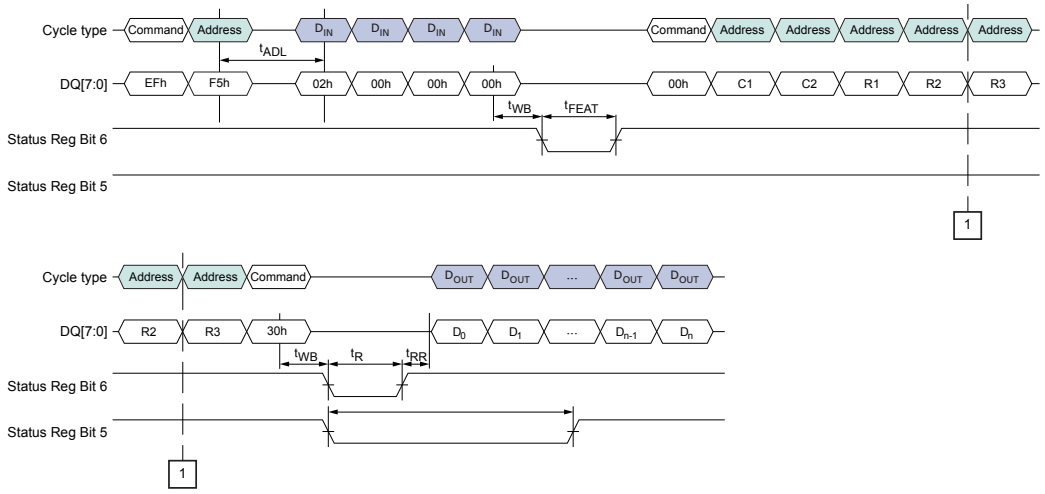


Table 36: Feature Address F6h: Sleep Lite

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Sleep Light configuration	Sleep Lite Disable (default)							0	0	00b	
	Sleep Lite Enable							0	1	01b	
	Sleep Lite - Target Level Enable							1	1	11b	
	Reserved	-	-	-	-	-	-				
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

The Sleep Lite feature allows the host to place unselected LUNs on an active target (CE#) into a low power state to reduce overall Icc where the current consumption by any LUN in Sleep Lite will be I_{SB} and I_{SBQ}. This feature only applies to NAND targets where more than one LUN exists per CE#. Once a LUN has been placed in Sleep Lite mode it is unable to accept any host commands.

The Sleep Lite feature will allow for any number of LUNs within a selected target to be placed in a low power state through the use of the SET FEATURES by LUN (D5h) command. When multiple LUNs within a target are to remain active the host will need to issue a SET FEATURES by LUN (D5h) command to each LUN that is to be put into Sleep Lite mode. In the event that the host only wants a single LUN to be active (all other LUNs to be placed into Sleep Lite mode) two different methods exist. The host could issue SET FEATURES by LUN (D5h) commands to each LUN on the target as suggested

in the method 1 example. An alternative solution would be for the host to use a target level SET FEATURES (EFh) command with the Sleep Lite - Target Level Enable (P1 = 11b) option as suggested in the method 2 example.

Method 1 for a 2 LUN per CE# configuration example:

1. Issue SET FEATURE by LUN (D5h) command to LUN0 to enable Sleep Lite (P1 = 01b)
2. LUN0 is in Sleep Lite mode. LUN2 remains active.

Method 2 for a 2 LUN per CE# configuration example:

1. LUN1 is selected (could be done using READ STATUS ENHANCED (78h) command or other means)
2. Issue SET FEATURE (EFh) command to enable Sleep Lite - Target Level (P1 = 11b)
3. LUN0 enters Sleep Lite mode. LUN1 remains active.

Because LUNs in Sleep Lite mode cannot accept host commands the only method for exiting Sleep Lite mode is by toggling CE#.

Since LUNs in Sleep Lite cannot accept commands, if GET FEATURE by LUN (D4h) command is issued to a LUN in Sleep Lite there will be no response. If a GET FEATURE (EEh) command is issued to a Target, the Target response will only be from the LUNs that are not in Sleep Lite and the GET FEATURES (EEh) returned data will specify not in Sleep Lite (P0=00h), hence there is no way to check if any of the LUNs on the Target are in Sleep Lite.

Special consideration is taken in the event that On Die Termination (ODT) is enabled. If the Sleep Lite feature is enabled on a LUN that is configured as a target terminator for the selected volume, that LUN should enter the sniff state. This is the same state the LUN enters if it is configured for non-Target termination and not on the selected volume. If the LUN is configured as a target terminator for the selected volume and a data burst is occurring, ODT should be enabled regardless of the status of the Sleep Lite feature. If a LUN is not configured as a target terminator for the selected volume then it should simply enter Sleep Lite when the Sleep Lite feature is enabled. See On Die Termination (ODT) section for additional details on ODT functionality.

Table 37: LUN state for Matrix Termination with Sleep Lite Feature

LUN is on selected Volume?	Terminator for selected Volume?	Sleep Lite Feature Enabled	LUN state
Yes	No	No	Selected
Yes	No	Yes	Sleep Lite
Yes	Yes	No	Selected
Yes	Yes	Yes	Sniff
No	Yes	N/A	Sniff
No	No	N/A	Deselected

VOLUME SELECT (E1h)

The Volume Select function is used to select a particular Volume based on the address specified. VOLUME SELECT (E1h) command is required to be used when CE# pin reduction is used or when matrix termination is used.

This command is accepted by all Targets that share a particular CE# pin. The command may be executed with any LUN on the Volume in any state. The VOLUME SELECT (E1h) command may only be issued as the first command after CE# is pulled LOW; CE# shall have remained HIGH for ^{t}CEH and CE# LOW for at least 100ns prior to the command in order for the VOLUME SELECT (E1h) command to be properly received by all NAND Targets connected to the Host Target. The DQS (DQS_t) signal shall remain HIGH for the entire Volume Select command sequence.

If Volumes that share a Host Target are configured to use different data interfaces, then the host shall issue the VOLUME SELECT (E1h) command using the Asynchronous data interface.

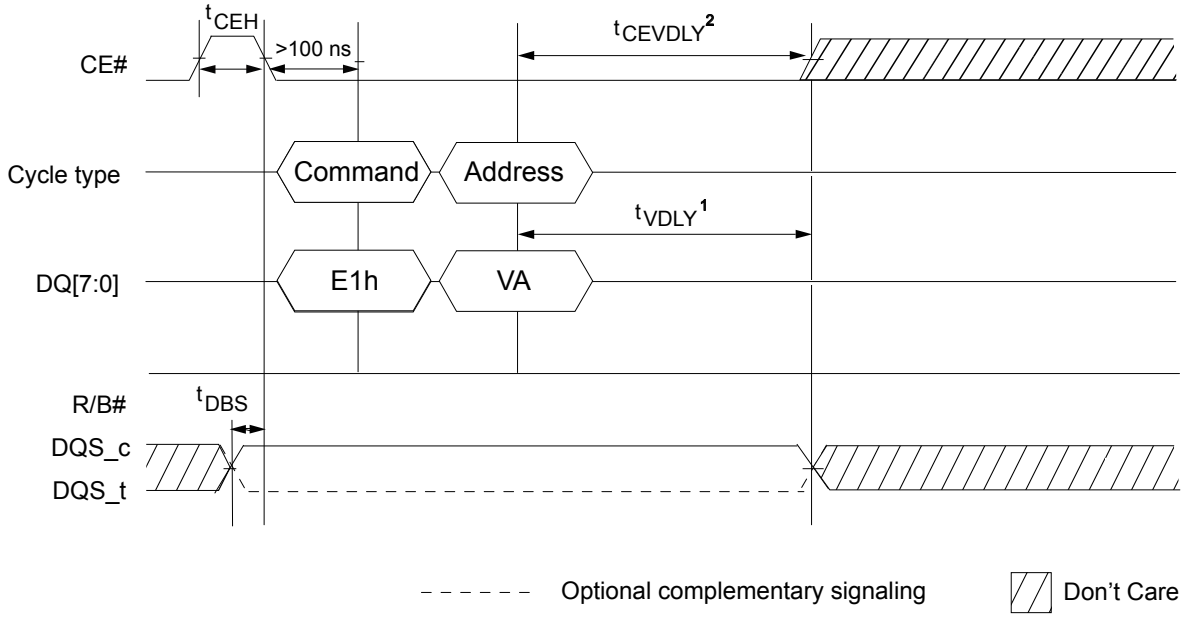
When the VOLUME SELECT (E1h) command is issued, all NAND Targets that have a Volume address that does not match the address specified shall be deselected to save power (equivalent behavior to CE# pulled HGH). If one of the LUNs in an unselected Volume is the assigned terminator for the Volume addressed, then that LUN will enter the sniff state.

If the Volume address specified does not correspond to any appointed Volume address, then all NAND Targets shall be deselected until a subsequent VOLUME SELECT (E1h) command is issued. If the VOLUME SELECT (E1h) command is not the first command issued after CE# is pulled LOW, then the NAND Targets revert to their previous selected, deselected, or sniff states.

The host shall not issue new commands to any LUN on any Volume until after ^{t}VDLY. This delay is required to ensure the appropriate Volume is selected for the next command issued. Also the host shall not bring CE# HIGH on any Volume until after ^{t}CEVDLY. This delay is required to ensure the appropriate Volume is selected based on the previously issued VOLUME SELECT (E1h) command.

The Volume address is retained across RESET (FAh, FCh, FFh) commands. A HARD RESET (FDh) command will not undo any previously set Volume Addressing assignments that were performed prior to the HARD RESET (FDh) command. After HARD RESET (FDh) command is issued the NAND Targets do not revert to their previous selected, deselected, or sniff states and a Volume Select Command (E1h) is required to select the desired Volume.

Figure 61: VOLUME SELECT (E1h) Operation



Notes:
1. The host shall not issue new commands to any LUN on any Volume until after t_{VDLY}. This delay is required to ensure the appropriate Volume is selected for the next command issued.
2. The host shall not bring CE# high on any Volume until after t_{CEVDLY}. This delay is required to ensure the appropriate Volume is selected based on the previously issued VOLUME SELECT command.

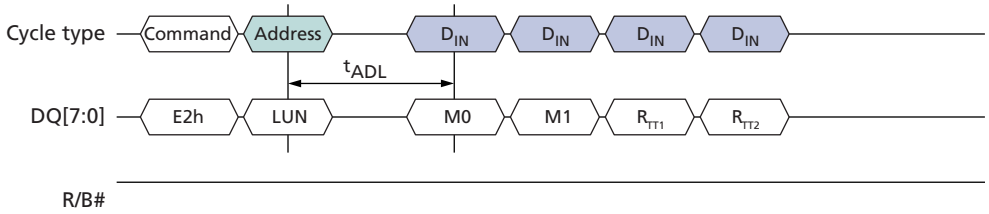
Table 38: Volume Address

	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Volume Address											
VA						Volume Address				-	
Reserved		0	0	0	0					-	

ODT CONFIGURE (E2h)

The ODT CONFIGURE (E2h) command is used to configure on-die termination. Specifically, ODT CONFIGURE (E2h) specifies whether a particular LUN is a terminator for a Volume(s) and the R_{TT} settings. If the LUN is specified as a terminator for one or more Volumes, then the LUN shall enable on-die termination when either data input or data output cycles are executed on the Volume(s) it is acting as a terminator for depending on the settings of . The on-die termination settings are retained across RESET (FAh, FCh, FFh) commands, but are not retained across HARD RESET (FDh) commands for the target LUN.

Figure 62: ODT CONFIGURE (E2h) Operation



The LUN address correspond to the same structure as the last address cycle for the NAND device which determines which LUN will act as the terminator.

The ODT Configuration Matrix structure is defined in table below. For the Volume Address fields M0 and M1, if a bit is set to one then the LUN shall act as the terminator for the corresponding Volume(s) (Vn) where n corresponds to the Volume address.

The ODT CONFIGURE (E2h) command is only available while in the NV-DDR2 or NV-DDR3 interface.

Table 39: ODT Configuration Matrix

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
M0 – Lower byte of the ODT configuration matrix											
Volume Address	Volumes that will be terminated by selected LUN	V7	V6	V5	V4	V3	V2	V1	V0	-	
M1 – Upper byte of the ODT configuration matrix											
Volume Address	Volumes that will be terminated by selected LUN	V15	V14	V13	V12	V11	V10	V9	V8	-	
R_{TT1}											

Table 39: ODT Configuration Matrix (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
DQ[7:0]/DQS_t/DQS_c R_{TT} and ODT enable for data input	ODT disabled (default)					0	0	0	0	0h	
	ODT enabled with R_{TT} of 150 Ohms					0	0	0	1	1h	
	ODT enabled with R_{TT} of 100 Ohms					0	0	1	0	2h	
	ODT enabled with R_{TT} of 75 Ohms					0	0	1	1	3h	
	ODT enabled with R_{TT} of 50 Ohms					0	1	0	0	4h	
Reserved	–					0	1	0	1	5h	
						0	1	1	0	6h	
						0	1	1	1	7h	
						1	X	X	X	8h-Fh	
DQ[7:0]/DQS_t/DQS_c R_{TT} and ODT enable for data output	ODT disabled (default)	0	0	0	0					0h	
	ODT enabled with R_{TT} of 150 Ohms	0	0	0	1					1h	
	ODT enabled with R_{TT} of 100 Ohms	0	0	1	0					2h	
	ODT enabled with R_{TT} of 75 Ohms	0	0	1	1					3h	
	ODT enabled with R_{TT} of 50 Ohms	0	1	0	0					4h	
Reserved	–	0	1	0	1					5h	
		0	1	1	0					6h	
		0	1	1	1					7h	
		1	X	X	X					8h-Fh	
R_{TT2}											

Table 39: ODT Configuration Matrix (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
RE_t and RE_c R_{TT} ODT enable	ODT disabled (default)					0	0	0	0	0h	
	ODT enabled with R_{TT} of 150 Ohms					0	0	0	1	1h	
	ODT enabled with R_{TT} of 100 Ohms					0	0	1	0	2h	
	ODT enabled with R_{TT} of 75 Ohms					0	0	1	1	3h	
	ODT enabled with R_{TT} of 50 Ohms					0	1	0	0	4h	
Reserved	–					0	1	0	1	5h	
						0	1	1	0	6h	
						0	1	1	1	7h	
						1	X	X	X	8h-Fh	
Reserved	-	0	0	0	0					0h	

ZQ Calibration

ZQ Calibration is performed by issuing F9h command for ZQCL (ZQ long calibration) and D9h command for ZQCS (ZQ short calibration). ZQ Calibration is used to calibrate NAND R_{ON} & ODT values. A longer time is required to calibrate output driver and on-die termination circuits at initialization and relatively smaller time to perform periodic calibrations.

The ZQCL (F9h) command is used to perform the initial calibration after power-up initialization sequence. The command enable ZQCL (F9h) may be issued at any time by the controller depending on the system environment. ZQCL (F9h) triggers the calibration engine inside the NAND device and once calibration is achieved, the calibrated values are transferred from the calibration engine to NAND I/O signals, which gets reflected as updated output driver and on-die termination values

ZQCL (F9h) operations are allowed a timing period of ^{t}ZQCL to perform the full calibration and then transfer of output driver and on-die termination values. When ZQCL (F9h) operation is complete, the host shall check status. If the FAIL bit is set (i.e. SR[0]=1), then the calibration procedure failed and user should check the RZQ resistor connection. If ZQCL (F9h) calibration fails the device will use the optimal driver settings.

ZQCS (D9h) command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter ^{t}ZQCS. One ZQCS (D9h) command can effectively correct a minimum of 1.5% (ZQ Correction) of R_{ON} and R_{TT} impedance error within ^{t}ZQCS for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS (D9h) commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS (D9h) commands, given the temperature ($T_{Driftrate}$) and voltage ($V_{Driftrate}$) drift rates that the NAND is subject to in the application, is illustrated below. The interval could be defined by the following formula:

Figure 63: Calibration time interval equation

$$Interval = \frac{ZQCorrection}{[(T_{SENS} \times T_{Driftrate}) + (V_{SENS} \times V_{Driftrate})]}$$

Where T_{SENS} = max($dR_{TT}dT$, $dR_{ON}dTM$) and V_{Sens} = max ($dR_{TT}dV$, $dR_{ON}dVM$) define the NAND temperature and voltage sensitivities. For example, if T_{Sens} = 0.5% / °C, V_{Sens} = 0.2% / mV, $T_{Driftrate}$ = 1°C / sec and $V_{Driftrate}$ = 15 mV/sec, then the interval between ZQCS (D9h) commands is calculated as:

Figure 64: Example of interval calculation between ZQCS (D9h) commands

$$\frac{1.5}{[(0.5 \times 1) + (0.2 \times 15)]} = 0.429 = 429\text{ms}$$

No other activities, including STATUS (70h/78h) operations, should be performed on the NAND channel (i.e. data bus) by the controller for the duration of ^{t}ZQCL or ^{t}ZQCS. The quiet time on the NAND channel allows accurate calibration of output driver and on-die termination values. For multi-channel packages, all channels should not have any data transfer occur during ZQ calibration even if not a shared channel with the LUN performing ZQ calibration. Once NAND calibration is achieved, the NAND should disable ZQ current consumption path to reduce power. NAND array operations may not occur on the device performing ZQCL (F9h) or ZQCS (D9h) operations. NAND array operations may occur on any devices that share the ZQ resistor with the device performing ZQCL (F9h) or ZQCS (D9h) operations. All devices connected to the DQ bus shall be in high impedance during the calibration procedure. The R/B# signal will be brought LOW by the device during calibration time, but if other deviecs are driving a shared R/B# LOW then the host is required to wait the maximum ^{t}WB + ^{t}ZQCL or ^{t}ZQCS time before issuing any commands to the data bus.

If a RESET (FFh, FAh, FCh) command is issued during a ZQ calibration operation, the RESET (FFh, FAh, FCh) operation is executed. After the RESET (FFh, FAh, FCh) command, the host is required to issue a new calibration command as soon as possible. If the RESET (FFh, FAh, FCh) command was issued during the ZQCL (F9h) operation, the NAND device will revert to factory settings for output driver strength and ODT values (i.e. as if no ZQ calibration operation was performed). If the RESET (FFh, FAh, FCh) command was issued during ZQCS (D9h) operation the NAND device will use the calibrated values.

ZQ Calibration Long (F9h)

The ZQ CALIBRATION LONG (ZQCL) (F9h) command is used to perform the initial calibration during a power-up initialization or reset sequence. Writing F9h to the command register, folllowed by one row address cycle containing the LUN address, begins the ZQCL (F9h) on the selected LUN. This command may be issued at any time by the host, depending on the system environment. The ZQCL (F9h) command triggers the calibration engine inside the NAND. After calibration is achieved, the calibrated values are transferred from the calibration engine to the NAND I/Os, which are reflected as updated R_{ON} and R_{TT} values.

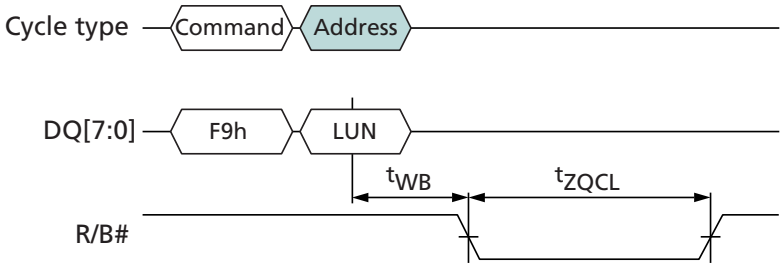
During ZQCL (F9h) operations, no array operations are allowed on the NAND device that is performing the ZQCL (F9h) operation. Array operations are allowed on any of the other NAND devices that share the ZQ signal with the NAND device that is performing the ZQCL (F9h) operation.

The NAND is allowed a timing window defined by either ^{t}ZQCL to perform a full calibration and transfer of values. When ZQCL (F9h) is issued during the initialization sequence, the timing parameter ^{t}ZQCL must be satisfied.

When ZQCL (F9h) operation is complete, the host shall check status. If the FAIL bit is set (i.e. SR[0]=1), then the calibration procedure failed and user should check the R_{ZQ} resis-

tor connection. If the ZQCL (F9h) operation fails the device will use the optimal driver settings.

Figure 65: ZQ Calibration Long (F9h)



ZQ Calibration Short (D9h)

The ZQ CALIBRATION SHORT (ZQCS) command (D9h) is used to perform periodic calibrations to account for small voltage and temperature variations. Writing D9h to the command register, folllowed by one row address cycle containing the LUN address, beings the ZQCS (D9h) on the selected LUN. A shorter timing window is provided to perform the reduced calibration and transfer of values as defined by timing parameter ^{t}ZQCS. A ZQCS (D9h) command can effectively correct a minimum of 1.5% R_{ON} and R_{TT} impedance error within ^{t}ZQCS, assuming the maximum sensitivities specified in the Output Driver Voltage and Temperature Sensitivity table.

During a ZQCS (D9h) operation, no array operations are allowed on the NAND device that is performing the ZQCS (D9h) operation. Array operations are allowed on any of the other NAND devices that share the ZQ signal with the NAND device that is performing the ZQCS (D9h) operation.

When the ZQCS (D9h) operation is complete, the host shall check status. If the FAIL bit is set (i.e. SR[0]=1), then the calibration procedure failed and user should issue ZQCL (F9h) command. If the ZQCS (F9h) operation fails the device will use the optimal driver settings, but output driver strength may still not be within specified range. If after the ZQCS (D9h) operation fails and subsequent ZQCL (F9h) operation passes, the NAND device output driver strength and R_{TT} are within specified range and the calibration sequence was successful. The user should not rerun the ZQCS (D9h) operation in this case. If after the ZQCS (D9h) operation fails and subsequent ZQCL (F9h) operation fails, the NAND device output driver strength and R_{TT} are not within specified range and the calibration sequence was unsuccessful. In this case, the device has the optimal driver settings, but signal integrity issues may occur.

Figure 66: ZQ Calibration Short (D9h)

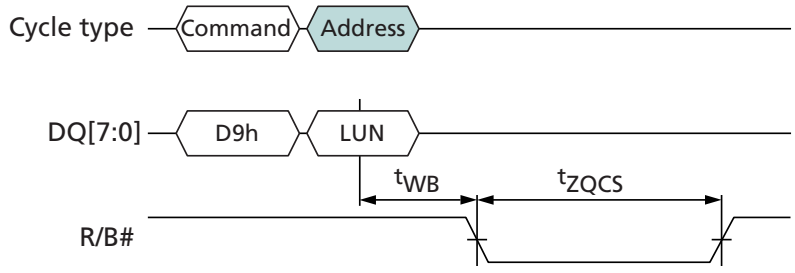


Table 40: LUN address cycle decoding

Description	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
LUN											
LUN selection	LUN0						0	0	0	-	
	LUN1						0	0	1	-	
Reserved	Don't Care	-	-	-	-	-				-	1

Note: 1. Can be either '1' or '0'.

ZQ external resistor value, tolerance, and capacitive loading

In order to use the ZQ Calibration function, a 300 ohm ±1% tolerance external resistor must be connected between the ZQ pin and ground. The ZQ resistance is the sum of the trace resistance and the actual resistor resistance. The user should attempt to place ZQ resistor as close as possible to the NAND device to reduce the trace resistance. The resistance presented to the NAND needs to be ±1% of 300 ohms. The single resistor can be used for each NAND or one resistor can be shared between all NAND devices in the package if the ZQ calibration timings for each NAND do not overlap. The capacitance of the LUN component of the ZQ signal will be less than an I/O signal. Depending on the number of LUNs per package, the total capacitance (capacitance of package + capacitance of LUN(s)) of the ZQ signal may exceed an I/O signal. For packages with eight or more LUN that share a ZQ signal, the total ZQ capacitance will not exceed 15% greater than the number of LUNs times the LUN capacitance of an I/O signal [i.e. Total ZQ capacitance < 1.15 * LUN capacitance (I/O) * number of LUNs].

The NV-DDR3 driver supports two different R_{ON} values. These R_{ON} values are R_{ON} = 35 Ohms and 50 Ohms. Output driver impedance R_{ON} is defined by the value of the external reference resistor R_{ZQ} as follows:

- $R_{ON}35 = R_{ZQ} / 8.5$ (nominal 35 ohms ±15% with nominal R_{ZQ} = 300 ohms)

Table 41: I/O Drive Strength Settings

Interface	Setting	Drive Strength	V_{CCQ}	Notes
Asynchronous, NV-DDR, NV-DDR2, or NV-DDR3 without ZQ Calibration	25 Ohms	1.4x = 25 Ohms	1.8V	
	35 Ohms	1.0x = 35 Ohms	1.8V/1.2V	
	50 Ohms	0.7x = 50 Ohms		

Table 41: I/O Drive Strength Settings (Continued)

Interface	Setting	Drive Strength	V_{CCQ}	Notes
NV-DDR2/ NV-DDR3 with ZQ Calibration	25 Ohms	-	1.8V/1.2V	1
	35 Ohms	RZQ / 8.5		
	50 Ohms	RZQ / 6		

Note: 1. The 25 Ohm drive strength does not support ZQ Calibration operations. If ZQ Calibration operations are used when the 25 Ohm drive strength is selected, the default NAND drive strength settings are still used.

Status Operations

Each die (LUN) provides its status independently of other die (LUNs) on the same target through its 8-bit status register.

After the READ STATUS (70h) or READ STATUS ENHANCED (78h) command is issued, status register output is enabled. The contents of the status register are returned on DQ[7:0] for each data output request.

When the asynchronous, NV-DDR2, or NV-DDR3 interfaces are active and status register output is enabled, changes in the status register are seen on DQ[7:0] as long as CE# and RE# are LOW; it is not necessary to toggle RE# to see the status register update.

When the NV-DDR interface is active and status register output is enabled, changes in the status register are seen on DQ[7:0] as long as CE# and W/R# are LOW and ALE and CLE are HIGH. DQS also toggles (with ^{t}DQSCK delay) while ALE and CLE are captured HIGH. If status register output is enabled and CE# and W/R# are LOW and ALE and CLE are also captured LOW, changes in the status register are still seen asynchronously on DQ[7:0] but DQS does not toggle.

While monitoring the status register to determine when a data transfer from the Flash array to the data register (^{t}R) is complete, the host must issue the READ MODE (00h) command to disable the status register and enable data output (see READ MODE (00h) (page 151)).

The READ STATUS (70h) command returns the status of the most recently selected die (LUN). To prevent data contention during or following an interleaved die (multi-LUN) operation, the host must enable only one die (LUN) for status output by using the READ STATUS ENHANCED (78h) command (see Interleaved Die (Multi-LUN) Operations (page 185)).

Table 42: Status Register Definition

SR Bit	Definition	Independent per Plane[1]	Description
7	WP#	–	Write Protect: 0 = Protected 1 = Not protected In the normal array mode, this bit indicates the value of the WP# signal. In OTP mode this bit is set to 0 if a PROGRAM OTP PAGE operation is attempted and the OTP area is protected.
6	RDY	–	Ready/Busy I/O: 0 = Busy 1 = Ready This bit indicates that the selected die (LUN) is not available to accept new commands, address, or data I/O cycles with the exception of RESET LUN (FAh), SYNCHRONOUS RESET (FCh), RESET (FFh), READ STATUS (70h), and READ STATUS ENHANCED (78h). This bit applies only to the selected die (LUN).

Table 42: Status Register Definition (Continued)

SR Bit	Definition	Independent per Plane[1]	Description
5	ARDY	–	Ready/Busy Array: 0 = Busy 1 = Ready This bit goes LOW (busy) when an array operation is occurring on any plane of the selected die (LUN). It goes HIGH when all array operations on the selected die (LUN) finish. This bit applies only to the selected die (LUN).
4	–	–	Reserved (0)
3	–	–	Reserved (0)
2	SUSPEND	–	Erase and Program Suspend: Used in conjunction with FAIL of the status register (SR[0]) SUSPEND = 0, FAIL = 0: Erase or Program operation completed with successful status. SUSPEND = 0, FAIL = 1: Erase or Program operation completed with fail status. SUSPEND = 1, FAIL = 0: Erase or Program operation successful suspended SUSPEND = 1, FAIL = 1: Reserved.
1	FAILC	Yes	Pass/Fail (N–1): 0 = Pass 1 = Fail This bit is set if the previous operation on the selected die (LUN) failed. This bit is valid only when RDY (SR bit 6) is 1. It applies to PROGRAM-, and COPYBACK PROGRAM-series operations (80h-10h, 80h-15h, 85h-10h). This bit is not valid following an ERASE-series or READ-series operation. The valid operations for this bit are PROGRAM- and COPYBACK PROGRAM-series operations. This bit is not an indicator for the status of ERASE- or READ-series operations. This bit retains the status of the previous valid operation. For example, if an erase operation is complete and the previous operation was a program operation the FAILC bit will provide pass/fail status information for the previous program operation.
0	FAIL	Yes	Pass/Fail (N): 0 = Pass 1 = Fail This bit is set if the most recently finished operation on the selected die (LUN) failed. This bit is valid only when ARDY (SR bit 5) is 1. It applies to PROGRAM-, ERASE-, and COPYBACK PROGRAM-series operations (80h-10h, 80h-15h, 60h-D0h, 85h-10h). This bit is not valid following a READ-series operation.

Note: 1. After a multi-plane operation begins, the FAILC and FAIL bits are ORed together for the active planes when the READ STATUS (70h) command is issued. After the READ STATUS ENHANCED (78h) command is issued, the FAILC and FAIL bits reflect the status of the plane selected.

READ STATUS (70h)

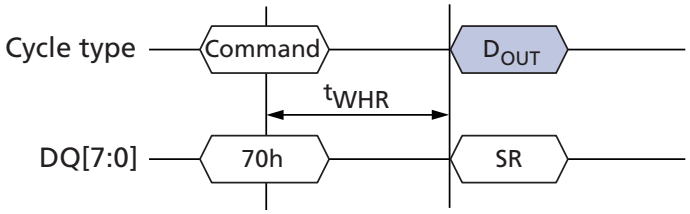
The READ STATUS (70h) command returns the status of the last-selected die (LUN) on a target. This command is accepted by the last-selected die (LUN) even when it is busy (RDY = 0).

If there is only one die (LUN) per target, the READ STATUS (70h) command can be used to return status following any NAND command.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select the die (LUN) that should report status. In this situation, using the READ STATUS (70h) command will result in bus contention, as two or more die (LUNs) could respond until the next operation is issued. The READ STATUS (70h) command can be used following all single die (LUN) operations.

If following a multi-plane operation, regardless of the number of LUNs per target, the READ STATUS (70h) command indicates an error occurred (FAIL = 1), use the READ STATUS ENHANCED (78h) command—once for each plane—to determine which plane operation failed.

Figure 67: READ STATUS (70h) Operation



READ STATUS ENHANCED (78h)

The READ STATUS ENHANCED (78h) command returns the status of the addressed die (LUN) on a target even when it is busy (RDY = 0). This command is accepted by all die (LUNs), even when they are BUSY (RDY = 0).

Writing 78h to the command register, followed by three row address cycles containing the page, block, and LUN addresses, puts the selected die (LUN) into read status mode. The selected die (LUN) stays in this mode until another valid command is issued. Die (LUNs) that are not addressed are deselected to avoid bus contention.

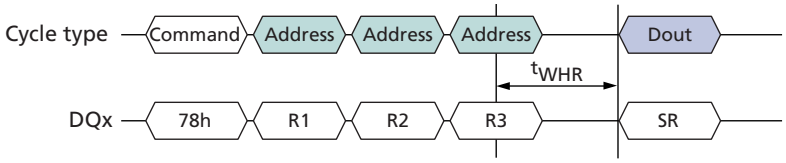
The selected LUN's status is returned when the host requests data output. The RDY and ARDY bits of the status register are shared for all of the planes of the selected die (LUN). The FAILC and FAIL bits are specific to the plane specified in the row address.

The READ STATUS ENHANCED (78h) command also enables the selected die (LUN) for data output. To begin data output following a READ-series operation after the selected die (LUN) is ready (RDY = 1), issue the READ MODE (00h) command, then begin data output. If the host needs to change the cache register that will output data, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command after the die (LUN) is ready (see CHANGE READ COLUMN ENHANCED (06h-E0h) (page 144)).

Use of the READ STATUS ENHANCED (78h) command is prohibited during the power-on RESET (FFh) command and when OTP mode is enabled. It is also prohibited follow-

ing some of the other reset, identification, and configuration operations. See individual operations for specific details.

Figure 68: READ STATUS ENHANCED (78h) Operation



FIXED ADDRESS READ STATUS ENHANCED (71h)

The FIXED ADDRESS READ STATUS ENHANCED (71h) command returns the status of the addressed die (LUN) on a target even when it is busy (RDY = 0). This command is accepted by all die (LUNs), even when they are BUSY (RDY = 0). The FIXED ADDRESS READ STATUS ENHANCED (71h) command can be used instead of READ STATUS ENHANCED (78h) command, but address cycle bit locations are fixed and do not change based on NAND architecture, number of bits per cell, or any mode selections.

Use of the FIXED ADDRESS READ STATUS ENHANCED (71h) command is allowed during the poweron RESET (FFh) command (during tPOR) and when OTP mode is enabled. It is also allowed following some of the other reset, identification, and configuration operations that READ STATUS ENHANCED (78h) is prohibited.

Writing 71h to the command register, followed by one row address cycle containing the hardcoded LUN selections, puts the selected die (LUN) into read status mode. The selected die (LUN) stays in this mode until another valid command is issued. Die (LUNs) that are not addressed are deselected to avoid bus contention.

The status output for 71h command is identical to the status output for 70h command. The selected LUN's status is returned when the host requests data output. The RDY, ARDY, FAILC and FAIL bits of the status register are shared for all of the planes of the selected die (LUN).

The FIXED ADDRESS READ STATUS ENHANCED (71h) command also enables the selected die (LUN) for data output. To begin data output following a READ-series operation after the selected die (LUN) is ready (RDY = 1), issue the READ MODE (00h) command, then begin data output. If the host needs to change the cache register that will output data, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command after the die (LUN) is ready (see CHANGE READ COLUMN ENHANCED (06h-E0h).

Figure 69: FIXED ADDRESS READ STATUS ENHANCED (71h) Operation

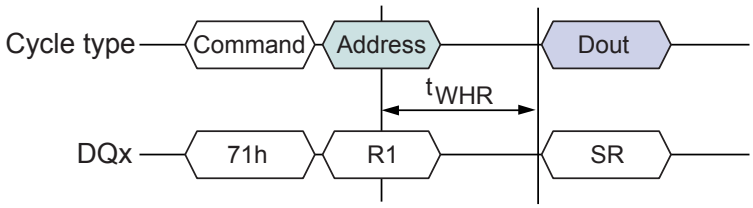


Table 43: R1 address cycle decoding for 71h Operation

Description	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
R1											
Bits LA0 (DQ0) for LUN selection	LUN0							0	0	000b	
	LUN1							0	1	001b	
Reserved	Don't Care	—	—	—	—	—	—			—	1

Note: 1. Can be either '1' or '0'.

Column Address Operations

The column address operations affect how data is input to and output from the cache registers within the selected die (LUNs). These features provide host flexibility for managing data, especially when the host internal buffer is smaller than the number of data bytes or words in the cache register.

When the asynchronous interface is active, column address operations can address any byte in the selected cache register.

When the synchronous interface is active, column address operations are aligned to word boundaries (CA0 is forced to 0), because as data is transferred on DQ[7:0] in two-byte units.

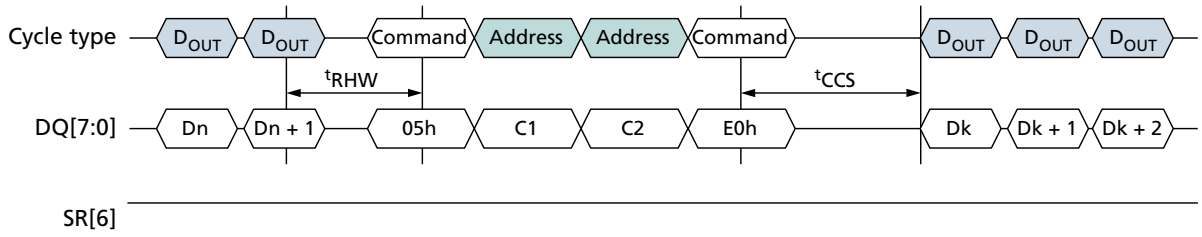
CHANGE READ COLUMN (05h-E0h)

The CHANGE READ COLUMN (05h-E0h) command changes the column address of the selected cache register and enables data output from the last selected die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during CACHE READ operations (RDY = 1; ARDY = 0).

Writing 05h to the command register, followed by two column address cycles containing the column address, followed by the E0h command, puts the selected die (LUN) into data output mode. After the E0h command cycle is issued, the host must wait at least ^{t}CCS before requesting data output. The selected die (LUN) stays in data output mode until another valid command is issued.

In devices with more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be issued prior to issuing the CHANGE READ COLUMN (05h-E0h). In this situation, using the CHANGE READ COLUMN (05h-E0h) command without the READ STATUS ENHANCED (78h) command will result in bus contention, as two or more die (LUNs) could output data.

Figure 70: CHANGE READ COLUMN (05h-E0h) Operation



CHANGE READ COLUMN ENHANCED (06h-E0h)

The CHANGE READ COLUMN ENHANCED (06h-E0h) command enables data output on the addressed die's (LUN's) cache register at the specified column address. This command is accepted by a die (LUN) when it is ready (RDY = 1; ARDY = 1).

Writing 06h to the command register, followed by two column address cycles and three row address cycles, followed by E0h, enables data output mode on the address LUN's cache register at the specified column address. After the E0h command cycle is issued, the host must wait at least ^{t}CCS before requesting data output. The selected die (LUN) stays in data output mode until another valid command is issued.

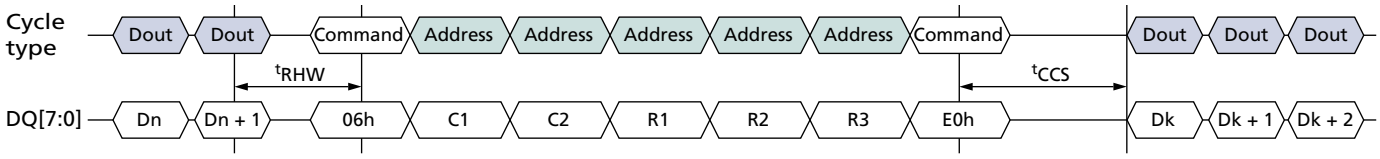
Following a multi-plane read page operation, the CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to select the cache register to be enabled for data output. After data output is complete on the selected plane, the command can be issued again to begin data output on another plane.

In devices with more than one die (LUN) per target, after all of the die (LUNs) on the target are ready (RDY = 1), the CHANGE READ COLUMN ENHANCED (06h-E0h) command can be used following an interleaved die (multi-LUN) read operation. Die (LUNs) that are not addressed are deselected to avoid bus contention.

In devices with more than one die (LUN) per target, during interleaved die (multi-LUN) operations where more than one or more die (LUNs) are busy (RDY = 1; ARDY = 0 or RDY = 0; ARDY = 0), the READ STATUS ENHANCED (78h) command must be issued to the die (LUN) to be selected prior to issuing the CHANGE READ COLUMN ENHANCED (06h-E0h). In this situation, using the CHANGE READ COLUMN ENHANCED (06h-E0h) command without the READ STATUS ENHANCED (78h) command will result in bus contention, as two or more die (LUNs) could output data.

If there is a need to update the column address without selecting a new cache register or LUN, the CHANGE READ COLUMN (05h-E0h) command can be used instead.

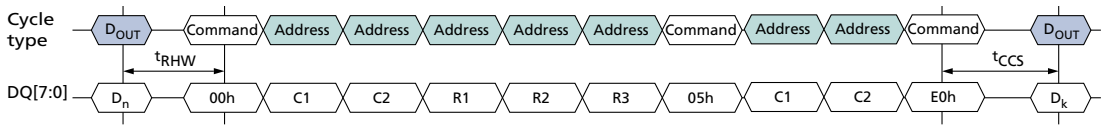
Figure 71: CHANGE READ COLUMN ENHANCED (06h-E0h) Operation



CHANGE READ COLUMN ENHANCED (00h-05h-E0h) Operation

This operation behaves the same as the CHANGE READ COLUMN ENHANCED (06h-E0h) command.

Figure 72: CHANGE READ COLUMN ENHANCED (00h-05h-E0h) Operation



CHANGE WRITE COLUMN (85h)

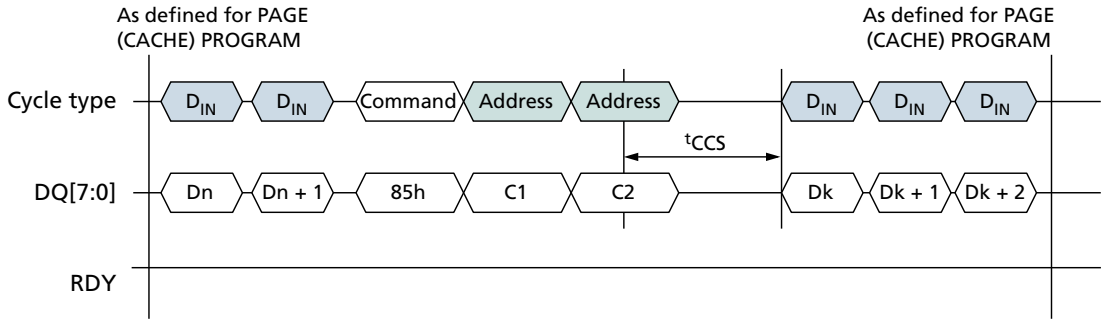
The CHANGE WRITE COLUMN (85h) command changes the column address of the selected cache register and enables data input on the last-selected die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during cache program operations (RDY = 1; ARDY = 0).

Writing 85h to the command register, followed by two column address cycles containing the column address, puts the selected die (LUN) into data input mode. After the second address cycle is issued, the host must wait at least ^{t}CCS before inputting data. The selected die (LUN) stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The CHANGE WRITE COLUMN (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle (10h, 11h, 15h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE MULTI-PLANE (80h-11h), PROGRAM PAGE CACHE (80h-15h), COPYBACK PROGRAM (85h-10h), and COPYBACK PROGRAM MULTI-PLANE (85h-11h).

In devices that have more than one die (LUN) per target, the CHANGE WRITE COLUMN (85h) command can be used with other commands that support interleaved die (multi-LUN) operations.

Figure 73: CHANGE WRITE COLUMN (85h) Operation



CHANGE ROW ADDRESS (85h)

The CHANGE ROW ADDRESS (85h) command changes the row address (block and page) where the cache register contents will be programmed in the NAND Flash array. It also changes the column address of the selected cache register and enables data input on the specified die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during cache programming operations (RDY = 1; ARDY = 0).

Write 85h to the command register. Then write two column address cycles and three row address cycles. This updates the page and block destination of the selected plane for the addressed LUN and puts the cache register into data input mode. After the fifth address cycle is issued the host must wait at least ^{t}CCS before inputting data. The selected LUN stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The CHANGE ROW ADDRESS (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle (10h, 11h, 15h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE MULTI-PLANE (80h-11h), PROGRAM PAGE CACHE (80h-15h), COPYBACK PROGRAM (85h-10h), and COPYBACK PROGRAM MULTI-PLANE (85h-11h). When used with these commands, the LUN address and plane select bits are required to be identical to the LUN address and plane select bits originally specified.

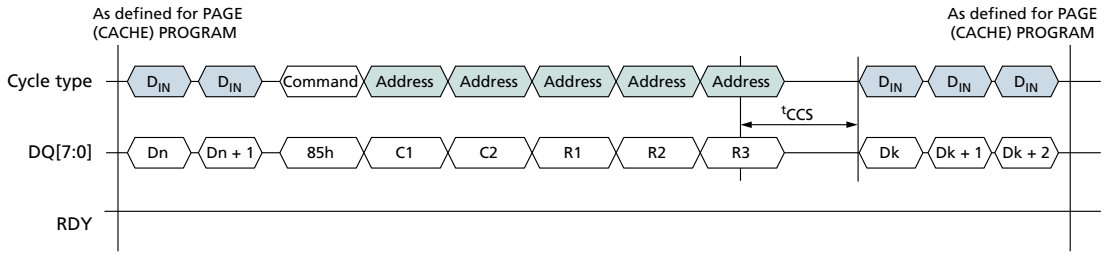
The CHANGE ROW ADDRESS (85h) command enables the host to modify the original page and block address for the data in the cache register to a new page and block address.

In devices that have more than one die (LUN) per target, the CHANGE ROW ADDRESS (85h) command can be used with other commands that support interleaved die (multi-LUN) operations.

The CHANGE ROW ADDRESS (85h) command can be used with the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) commands to read and modify cache register contents in small sections prior to programming cache register contents to the NAND Flash array. This capability can reduce the amount of buffer memory used in the host controller.

To modify the cache register contents in small sections, first issue a PAGE READ (00h-30h) or COPYBACK READ (00h-35h) operation. When data output is enabled, the host can output a portion of the cache register contents. To modify the cache register contents, issue the 85h command, the column and row addresses, and input the new data. The host can re-enable data output by issuing the 11h command, waiting ^{t}DBSY, and then issuing the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) command. It is possible toggle between data output and data input multiple times. After the final CHANGE ROW ADDRESS (85h) operation is complete, issue the 10h command to program the cache register to the NAND Flash array.

Figure 74: CHANGE ROW ADDRESS (85h) Operation



Read Operations

Read operations are used to copy data from the NAND Flash array of one or more of the planes to their respective cache registers and to enable data output from the cache registers to the host through the DQ bus.

Read Operations

The READ PAGE (00h-30h) command, when issued by itself, reads one page from the NAND Flash array to its cache register and enables data output for that cache register.

During data output the following commands can be used to read and modify the data in the cache registers: CHANGE READ COLUMN (05h-E0h) and CHANGE ROW ADDRESS (85h).

Read Cache Operations

To increase data throughput, the READ PAGE CACHE-series (31h, 00h-31h) commands can be used to output data from the cache register while concurrently copying a page from the NAND Flash array to the data register.

To begin a read page cache sequence, begin by reading a page from the NAND Flash array to its corresponding cache register using the READ PAGE (00h-30h) command. R/B# goes LOW during ^{t}R and the selected die (LUN) is busy (RDY = 0, ARDY = 0). After ^{t}R (R/B# is HIGH and RDY = 1, ARDY = 1), issue either of these commands:

- READ PAGE CACHE SEQUENTIAL (31h)—copies the next sequential page from the NAND Flash array to the data register
- READ PAGE CACHE RANDOM (00h-31h)—copies the page specified in this command from the NAND Flash array (any plane) to its corresponding data register

After the READ PAGE CACHE-series (31h, 00h-31h) command has been issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^{t}RCBSY while the next page begins copying data from the array to the data register. After ^{t}RCBSY, R/B# goes HIGH and the die's (LUN's) status register bits indicate the device is busy with a cache operation (RDY = 1, ARDY = 0). The cache register becomes available and the page requested in the READ PAGE CACHE operation is transferred to the data register. At this point, data can be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data output by the die (LUN).

After outputting the desired number of bytes from the cache register, either an additional READ PAGE CACHE-series (31h, 00h-31h) operation can be started or the READ PAGE CACHE LAST (3Fh) command can be issued.

If the READ PAGE CACHE LAST (3Fh) command is issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^{t}RCBSY while the data register is copied into the cache register. After ^{t}RCBSY, R/B# goes HIGH and RDY = 1 and ARDY = 1, indicating that the cache register is available and that the die (LUN) is ready. Data can then be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output.

For READ PAGE CACHE-series (31h, 00h-31h, 3Fh), during the die (LUN) busy time, ^{t}RCBSY, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h) and RESET (FFh, FCh). When RDY = 1 and ARDY = 0, the only valid commands during READ PAGE CACHE-series (31h, 00h-31h) operations are status opera-

tions (70h, 78h), READ MODE (00h), READ PAGE CACHE-series (31h, 00h-31h), CHANGE READ COLUMN (05h-E0h), and RESET (FFh, FCh).

SET FEATURES operations are not supported within a cache read sequence that has not been closed out with a READ PAGE CACHE LAST (3Fh) command.

Multi-Plane Read Operations

Multi-plane read page operations improve data throughput by copying data from more than one plane simultaneously to the specified cache registers. This is done by pre-pending one or more READ PAGE MULTI-PLANE (00h-32h) commands in front of the READ PAGE (00h-30h) command.

When the die (LUN) is ready, the CHANGE READ COLUMN ENHANCED (06h-E0h) command determines which plane outputs data. During data output, the following commands can be used to read and modify the data in the cache registers: CHANGE READ COLUMN (05h-E0h) and CHANGE ROW ADDRESS (85h). See Multi-Plane Operations for details.

Multi-Plane Read Cache Operations

Multi-plane read cache operations can be used to output data from more than one cache register while concurrently copying one or more pages from the NAND Flash array to the data register. This is done by prepending READ PAGE MULTI-PLANE (00h-32h) commands in front of the READ PAGE CACHE RANDOM (00h-31h) command.

To begin a multi-plane read page cache sequence, begin by issuing a MULTI-PLANE READ PAGE operation using the READ PAGE MULTI-PLANE (00h-32h) and READ PAGE (00h-30h) commands. R/B# goes LOW during ^{t}R and the selected die (LUN) is busy (RDY = 0, ARDY = 0). After ^{t}R (R/B# is HIGH and RDY = 1, ARDY = 1), issue either of these commands:

- READ PAGE CACHE SEQUENTIAL (31h)—copies the next sequential page from the previously addressed planes from the NAND Flash array to the data registers.
- READ PAGE MULTI-PLANE (00h-32h) commands, if desired, followed by the READ PAGE CACHE RANDOM (00h-31h) command—copies the pages specified from the NAND Flash array to the corresponding data registers.

After the READ PAGE CACHE-series (31h, 00h-31h) command has been issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^{t}RCBSY while the next pages begin copying data from the array to the data registers. After ^{t}RCBSY, R/B# goes HIGH and the LUN's status register bits indicate the device is busy with a cache operation (RDY = 1, ARDY = 0). The cache registers become available and the pages requested in the READ PAGE CACHE operation are transferred to the data registers. Issue the CHANGE READ COLUMN ENHANCED (06h-E0h) command to determine which cache register will output data. After data is output, the CHANGE READ COLUMN ENHANCED (06h-E0h) command can be used to output data from other cache registers. After a cache register has been selected, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data output.

After outputting data from the cache registers, either an additional MULTI-PLANE READ CACHE-series (31h, 00h-31h) operation can be started or the READ PAGE CACHE LAST (3Fh) command can be issued.

If the READ PAGE CACHE LAST (3Fh) command is issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^{t}RCBSY while the data registers are cop-

ied into the cache registers. After ^{t}RCBSY, R/B# goes HIGH and RDY = 1 and ARDY = 1, indicating that the cache registers are available and that the die (LUN) is ready. Issue the CHANGE READ COLUMN ENHANCED (06h-E0h) command to determine which cache register will output data. After data is output, the CHANGE READ COLUMN ENHANCED (06h-E0h) command can be used to output data from other cache registers. After a cache register has been selected, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data output.

For READ PAGE CACHE-series (31h, 00h-31h, 3Fh), during the die (LUN) busy time, ^{t}RCBSY, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h) and RESET (FFh, FCh). When RDY = 1 and ARDY = 0, the only valid commands during READ PAGE CACHE-series (31h, 00h-31h) operations are status operations (70h, 78h), READ MODE (00h), multi-plane read cache-series (31h, 00h-32h, 00h-31h), CHANGE READ COLUMN (05h-E0h, 06h-E0h), and RESET (FFh, FCh).

SET FEATURES operations are not supported within a cache read sequence that has not been closed out with a READ PAGE CACHE LAST (3Fh) command.

See Multi-Plane Operations for additional multi-plane addressing requirements.

READ MODE (00h)

The READ MODE (00h) command disables status output and enables data output for the last-selected die (LUN) and cache register after a READ operation (00h-30h, 00h-35h) has been monitored with a status operation (70h, 78h). This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 3Fh, 00h-31h) operations (RDY = 1 and ARDY = 0).

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) prior to issuing the READ MODE (00h) command. This prevents bus contention.

READ PAGE (00h-30h)

The READ PAGE (00h–30h) command copies a page from the NAND Flash array to its respective cache register and enables data output. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

To read a page from the NAND Flash array, write the 00h command to the command register, the write five address cycles to the address registers, and conclude with the 30h command. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}R as data is transferred.

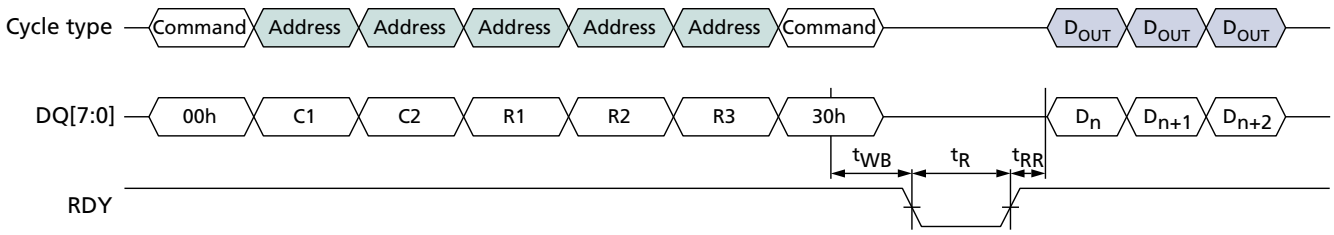
To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) can be used. If the status operations are used to monitor the LUN's status, when the die (LUN) is ready (RDY = 1, ARDY = 1), the host disables status output and enables data output by issuing the READ MODE (00h) command. When the host requests data output, output begins at the column address specified.

During data output the CHANGE READ COLUMN (05h-E0h) command can be issued.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) prior to the issue of the READ MODE (00h) command. This prevents bus contention.

The READ PAGE (00h-30h) command is used as the final command of a multi-plane read operation. It is preceded by one or more READ PAGE MULTI-PLANE (00h-32h) commands. Data is transferred from the NAND Flash array for all of the addressed planes to their respective cache registers. When the die (LUN) is ready (RDY = 1, ARDY = 1), data output is enabled for the cache register linked to the least significant plane addressed, regardless of input order. When the host requests data output, output begins at the column address last specified in the READ PAGE (00h-30h) command. The CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to enable data output in the other cache registers. See Multi-Plane Operations for additional multi-plane addressing requirements.

Figure 75: READ PAGE (00h-30h) Operation



READ PAGE CACHE SEQUENTIAL (31h)

The READ PAGE CACHE SEQUENTIAL (31h) command reads the next sequential page within a block into the data register while the previous page is output from the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

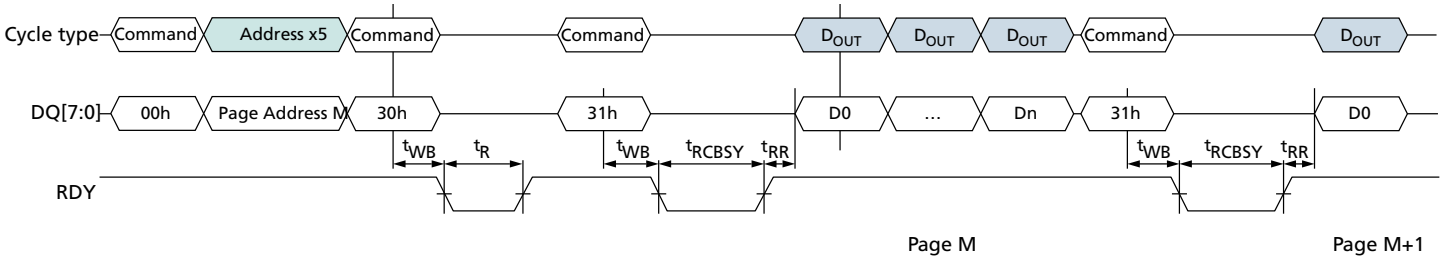
To issue this command, write 31h to the command register. After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY. After ^{t}RCBSY, R/B# goes HIGH and the die (LUN) is busy with a cache operation (RDY = 1, ARDY = 0), indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point, data can be output from the cache register beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output from the cache register.

The READ PAGE CACHE SEQUENTIAL (31h) command can be used to cross block boundaries. If the READ PAGE CACHE SEQUENTIAL (31h) command is issued after the last page of a block is read into the data register, the next page read will be the next logical block in the plane which the 31h command was issued. If the READ PAGE CACHE SEQUENTIAL (31h) command is issued after the last page of a plane is read into the data register, the NAND device will keep outputting the data from the last page of the plane. The last page of the plane is not re-read from the NAND array. Data is kept in the cache register and read from there. Do not issue the READ PAGE CACHE SEQUENTIAL (31h) to cross die (LUN) boundaries. Instead, issue the READ PAGE CACHE LAST (3Fh) command.

If the READ PAGE CACHE SEQUENTIAL (31h) command is issued after a MULTI-PLANE READ PAGE operation (00h-32h, 00h-30h), the next sequential pages are read into the data registers while the previous pages can be output from the cache registers. During multi-plane sequential cache read mode, if the READ PAGE CACHE SEQUENTIAL (31h) command is issued after reading the last page in the last block in one plane and a last page in a random block in the other plane, the circuit increments the block address and page address for only the plane that has not reached the end of its plane addressing. After the die (LUN) is ready (RDY = 1, ARDY = 0), the CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to select which cache register outputs data.

SET FEATURES operations are not supported within a cache read sequence that has not been closed out with a READ PAGE CACHE LAST (3Fh) command.

Figure 76: READ PAGE CACHE SEQUENTIAL (31h) Operation



READ PAGE CACHE RANDOM (00h-31h)

The READ PAGE CACHE RANDOM (00h-31h) command reads the specified block and page into the data register while the previous page is output from the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

To issue this command, write 00h to the command register, then write five address cycles to the address register, and conclude by writing 31h to the command register. The column address in the address specified is ignored. The die (LUN) address must match the same die (LUN) address as the previous READ PAGE (00h-30h) command or, if applicable, the previous READ PAGE CACHE RANDOM (00h-31h) command. There is no restriction on the plane address.

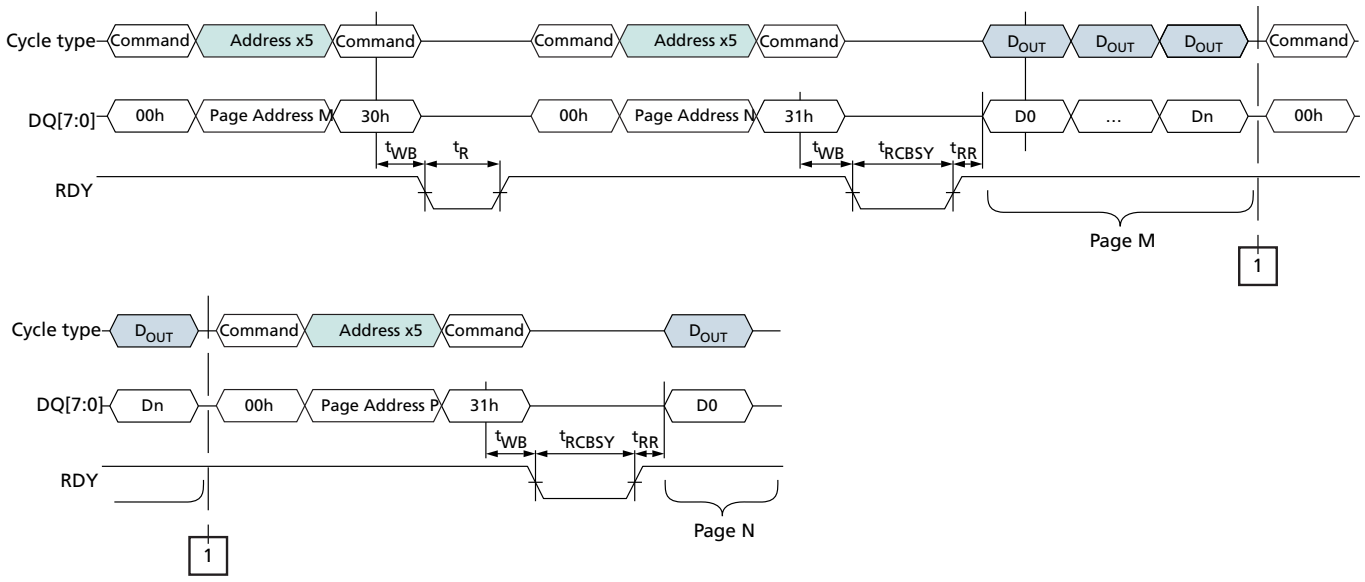
After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY. After ^{t}RCBSY, R/B# goes HIGH and the die (LUN) is busy with a cache operation (RDY = 1, ARDY = 0), indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point, data can be output from the cache register beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output from the cache register.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command followed by the READ MODE (00h) command must be used to select only one die (LUN) and prevent bus contention.

If a MULTI-PLANE CACHE RANDOM (00h-32h, 00h-31h) command is issued after a MULTI-PLANE READ PAGE operation (00h-32h, 00h-30h), then the addressed pages are read into the data registers while the previous pages can be output from the cache registers. After the die (LUN) is ready (RDY = 1, ARDY = 0), the CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to select which cache register outputs data.

SET FEATURES operations are not supported within a cache read sequence that has not been closed out with a READ PAGE CACHE LAST (3Fh) command.

Figure 77: READ PAGE CACHE RANDOM (00h-31h) Operation



READ PAGE CACHE LAST (3Fh)

The READ PAGE CACHE LAST (3Fh) command ends the read page cache sequence and copies a page from the data register to the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

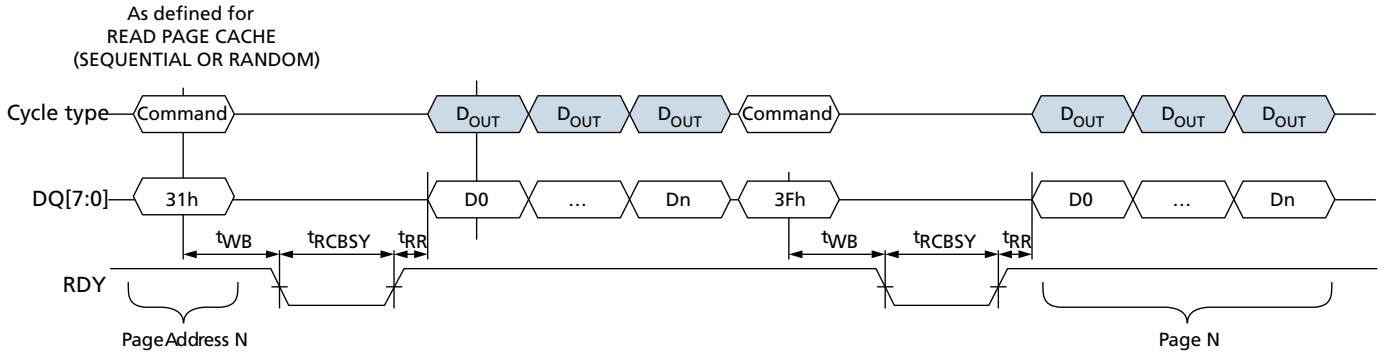
To issue the READ PAGE CACHE LAST (3Fh) command, write 3Fh to the command register. After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY. After ^{t}RCBSY, R/B# goes HIGH and the die (LUN) is ready (RDY = 1, ARDY = 1). At this point, data can be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output from the cache register.

In devices that have more than one LUN per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command followed by the READ MODE (00h) command must be used to select only one die (LUN) and prevent bus contention.

If the READ PAGE CACHE LAST (3Fh) command is issued after a MULTI-PLANE READ PAGE CACHE operation (31h; 00h-32h, 00h-30h), the die (LUN) goes busy until the pages are copied from the data registers to the cache registers. After the die (LUN) is ready (RDY = 1, ARDY = 1), the CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to select which cache register outputs data.

SET FEATURES operations are not supported within a cache read sequence that has not been closed out with a READ PAGE CACHE LAST (3Fh) command.

Figure 78: READ PAGE CACHE LAST (3Fh) Operation



READ PAGE MULTI-PLANE (00h-32h)

The READ PAGE MULTI-PLANE (00h-32h) command queues a plane to transfer data from the NAND flash array to its cache register. This command can be issued one or more times. Each time a new plane address is specified, that plane is also queued for data transfer. The READ PAGE (00h-30h) command is issued to select the final plane and to begin the read operation for all previously queued planes. All queued planes will transfer data from the NAND Flash array to their cache registers.

To issue the READ PAGE MULTI-PLANE (00h-32h) command, write 00h to the command register, then write five address cycles to the address register, and conclude by writing 32h to the command register. The column address in the address specified is ignored.

After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}DBSY. After ^{t}DBSY, R/B# goes HIGH and the die (LUN) is ready (RDY = 1, ARDY = 1). At this point, the die (LUN) and block are queued for data transfer from the array to the cache register for the addressed plane. During ^{t}DBSY, the only valid commands are status operations (70h, 78h) and reset commands (FFh, FCh). Following ^{t}DBSY, to continue the MULTI-PLANE READ operation, the only valid commands are status operations (70h, 78h), READ PAGE MULTI-PLANE (00h-32h), READ PAGE (00h-30h), and READ PAGE CACHE RANDOM (00h-31h).

Additional READ PAGE MULTI-PLANE (00h-32h) commands can be issued to queue additional planes for data transfer.

If the READ PAGE (00h-30h) command is used as the final command of a MULTI-PLANE READ operation, data is transferred from the NAND Flash array for all of the addressed planes to their respective cache registers. When the die (LUN) is ready (RDY = 1, ARDY = 1), data output is enabled for the cache register linked to the least significant plane addressed, regardless of input order. When the host requests data output, it begins at the column address specified in the READ PAGE (00h-30h) command. To enable data output in the other cache registers, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command. Additionally, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address within the currently selected plane.

If the READ PAGE CACHE SEQUENTIAL (31h) is used as the final command of a MULTI-PLANE READ CACHE operation, data is copied from the previously read operation from each plane to each cache register and then data is transferred from the NAND Flash array for all previously addressed planes to their respective data registers. When the die (LUN) is ready (RDY = 1, ARDY = 0), data output is enabled. The CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to determine which cache register outputs data first. To enable data output in the other cache registers, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command. Additionally, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address within the currently selected plane.

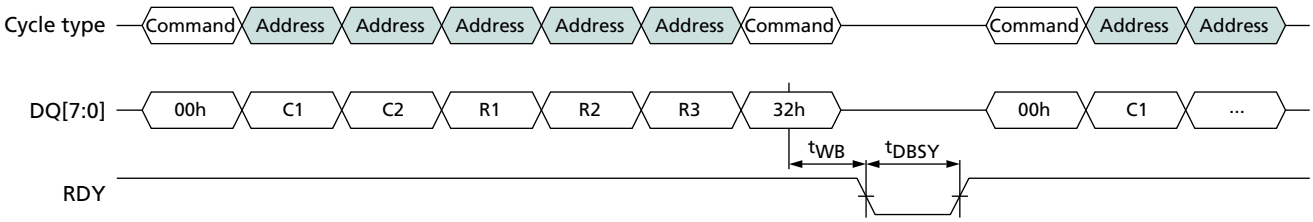
If the READ PAGE CACHE RANDOM (00h-31h) command is used as the final command of a MULTI-PLANE READ CACHE operation, data is copied from the previously read operation from the data register to the cache register and then data is transferred from the NAND Flash array for all of the addressed planes to their respective data registers. When the die (LUN) is ready (RDY = 1, ARDY = 0), data output is enabled. The CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to determine which cache register outputs data first. To enable data output in the other cache registers, use the CHANGE

READ COLUMN ENHANCED (06h-E0h) command. Additionally, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address within the currently selected plane.

SET FEATURES operations are not supported within a cache read sequence that has not been closed out with a READ PAGE CACHE LAST (3Fh) command.

See Multi-Plane Operations for additional multi-plane addressing requirements.

Figure 79: READ PAGE MULTI-PLANE (00h-32h) Operation



Read Retry Operations

Read retry operations are used as an additional method to recover from bit errors beyond the ECC correction threshold.

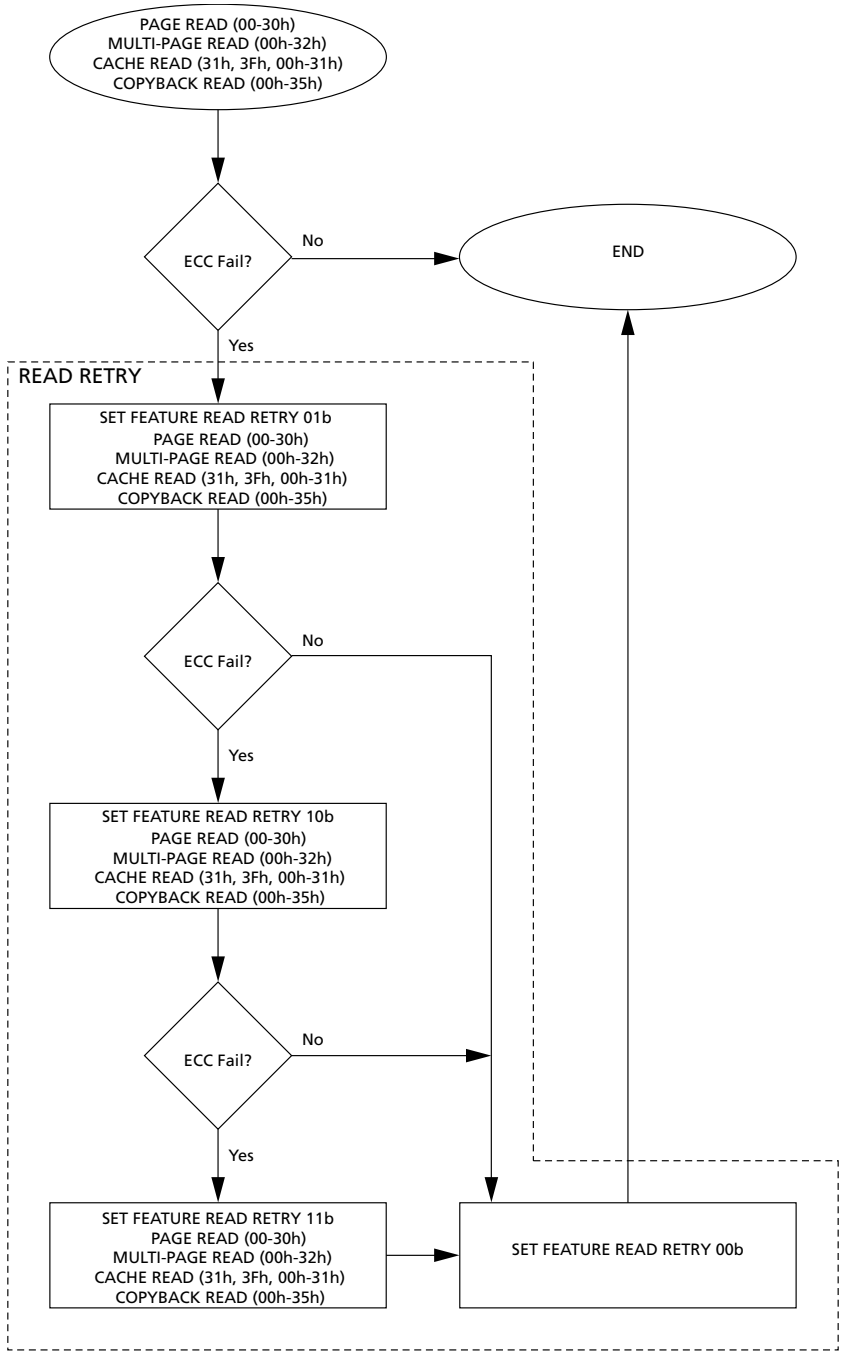
Read Retry Operations

The read retry operations are a coordination of read operations and SET FEATURES (EFh) or SET FEATURES by LUN (D5h) with feature address 89h, selecting different internal read settings in attempt to recover data that is beyond the ECC correction threshold. Using the read retry operations with any array read operation commands is allowed. See Configuration Operations and Feature Address 89h: Read Retry for details.

If reading a page has failed for bit errors beyond the ECC correction threshold, the host issues the SET FEATURE (EFh) or SET FEATURES by LUN (D5h) command to feature address 89h with P1 subfeature set to a read retry option, as defined in that feature address. A new NAND array READ operation can now be performed. If the read still fails for bit errors beyond the ECC correction threshold, issue the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command with the read retry (89h) feature address to select the next consecutive read retry option and repeat read retry operations until the data is correctable or the last option has been attempted. If the re-read is now correctable within the ECC threshold limits, the next read retry option should be set to its default value before the next NAND array READ operation. See Figure 80 (page 160) for flow diagram of read retry operations.

When the user writes to the read retry feature address, all subsequent reads use the internal NAND settings associated with that value until either the read retry feature address is rewritten or the device is powered down. This feature should not be used with the following commands: READ PARAMETER PAGE (ECh), READ UNIQUE ID (EDh), READ OTP PAGE (00h-30h).

Figure 80: Read Retry Flow Chart



Note: 1. There may be more read retry options than are shown in the figure for this NAND device. See Configuration Operations and Read Retry (89h) feature address for details.

Program Operations

Program operations are used to move data from the cache or data registers to the NAND array of one or more planes. During a program operation the contents of the cache and/or data registers are modified by the internal control logic.

Within a block, pages must be programmed sequentially from the least significant page address to the most significant page address (i.e. 0, 1, 2, 3, …). Programming pages out of order within a block is prohibited.

Program Operations

The PROGRAM PAGE (80h-10h) command, when not preceded by the PROGRAM PAGE MULTI-PLANE (80h-11h) command, programs one page from the cache register to the NAND Flash array. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that the operation has completed successfully.

Program Cache Operations

The PROGRAM PAGE CACHE (80h-15h) command can be used to improve program operation system performance. When this command is issued, the die (LUN) goes busy (RDY = 0, ARDY = 0) while the cache register contents are copied to the data register, and the die (LUN) is busy with a program cache operation (RDY = 1, ARDY = 0. While the contents of the data register are moved to the NAND Flash array, the cache register is available for an additional PROGRAM PAGE CACHE (80h-15h) or PROGRAM PAGE (80h-10h) command.

For PROGRAM PAGE CACHE-series (80h-15h) operations, during the die (LUN) busy times, ^{t}CBSY and ^{t}LPROG, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 71h, 78h) and reset (FFh, FCh, FAh). When RDY = 1 and ARDY = 0, the only valid commands during PROGRAM PAGE CACHE-series (80h-15h) operations are status operations (70h, 71h, 78h), PROGRAM PAGE CACHE (80h-15h), PROGRAM PAGE (80h-10h), CHANGE WRITE COLUMN (85h), CHANGE ROW ADDRESS (85h), and reset (FFh, FCh, FAh).

Multi-Plane Program Operations

The PROGRAM PAGE MULTI-PLANE (80h-11h) command can be used to improve program operation system performance by enabling multiple pages to be moved from the cache registers to different planes of the NAND Flash array. This is done by prepending one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands in front of the PROGRAM PAGE (80h-10h) command. See Multi-Plane Operations for details.

Multi-Plane Program Cache Operations

The PROGRAM PAGE MULTI-PLANE (80h-11h) command can be used to improve program cache operation system performance by enabling multiple pages to be moved from the cache registers to the data registers and, while the pages are being transferred from the data registers to different planes of the NAND Flash array, free the cache registers to receive data input from the host. This is done by prepending one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands in front of the PROGRAM PAGE CACHE (80h-15h) command. See Multi-Plane Operations for details.

PROGRAM PAGE (80h-10h)

The PROGRAM PAGE (80h-10h) command enables the host to input data to a cache register, and move the data from the cache register to the specified block and page address

in the array of the selected die (LUN). This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) when it is busy with a PROGRAM PAGE CACHE (80h-15h) operation (RDY = 1, ARDY = 0).

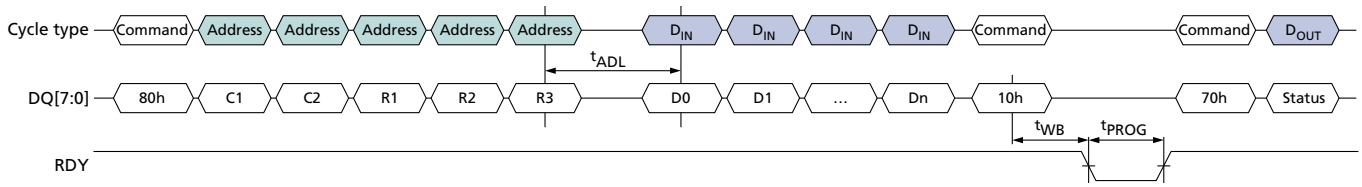
To input a page to the cache register and move it to the NAND array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by a PROGRAM PAGE MULTI-PLANE (80h-11h) command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Then write five address cycles containing the column address and row address of the lower page address. Data input cycles follow for the lower page address. Serial data is input beginning at the column address specified. At any time during the data input cycle the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands may be issued. When data input is complete, write 10h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}PROG as the lower page data is transferred.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 71h, 78h) may be used. When the die (LUN) is ready (RDY = 1, ARDY = 1).

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) or FIXED ADDRESS READ STATUS (71h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

When the last PROGRAM PAGE (80h-10h) command is used as the final command of a multi-plane program operation, it is preceded by one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands, data is transferred from the cache registers for all of the addressed planes to the NAND array. The host should check the status of the operation by using the status operations (70h, 71h, 78h). See Multi-Plane Operations for multi-plane addressing requirements.

Figure 81: PROGRAM PAGE (80h-10h) Operation



PROGRAM PAGE CACHE (80h-15h)

The PROGRAM PAGE CACHE (80h-15h) command enables the host to input data to a cache register; copies the data from the cache register to the data register; then moves the data register contents to the specified block and page address in the array of the selected die (LUN). After the data is copied to the data register, the cache register is available for additional PROGRAM PAGE CACHE (80h-15h) or PROGRAM PAGE (80h-10h) commands. The PROGRAM PAGE CACHE (80h-15h) command is accepted by the die (LUN) when it is ready (RDY =1, ARDY = 1). It is also accepted by the die (LUN) when busy with a PROGRAM PAGE CACHE (80h-15h) operation (RDY = 1, ARDY = 0).

To input a page to the cache register and move it to the NAND array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by a PROGRAM PAGE MULTI-PLANE (80h-11h) command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Then write five address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands may be issued. When data input is complete, write 10h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}CBSY to allow the data register to become available from a previous program cache operation to copy data from the cache register to the data register, and then to begin moving the data register contents to the specified pages and block address.

To determine the progress of ^{t}CBSY, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 71h, 78h) can be used. When the LUN's status shows that it is busy with a PROGRAM CACHE operation (RDY = 1, ARDY = 0), the host should check the status of the FAILC bit to see if a previous cache operation was successful.

If, after ^{t}CBSY, the host wants to wait for the program cache operation to complete, without issuing the PROGRAM PAGE (80h-10h) command, the host should monitor ARDY until it is 1. The host should then check the status of the FAIL and FAILC bits.

In devices with more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) or FIXED ADDRESS READ STATUS (71h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

The PROGRAM PAGE CACHE (80h-15h) command is used as the final command of a multi-plane program cache operation. It is preceded by one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands. Data for all of the addressed planes is transferred from the cache registers to the corresponding data registers, then moved to the NAND

Flash array. The host should check the status of the operation by using the status operations (70h, 71h, 78h). See Multi-Plane Operations for multi-plane addressing requirements.

Figure 82: PROGRAM PAGE CACHE (80h–15h) Operation (Start)

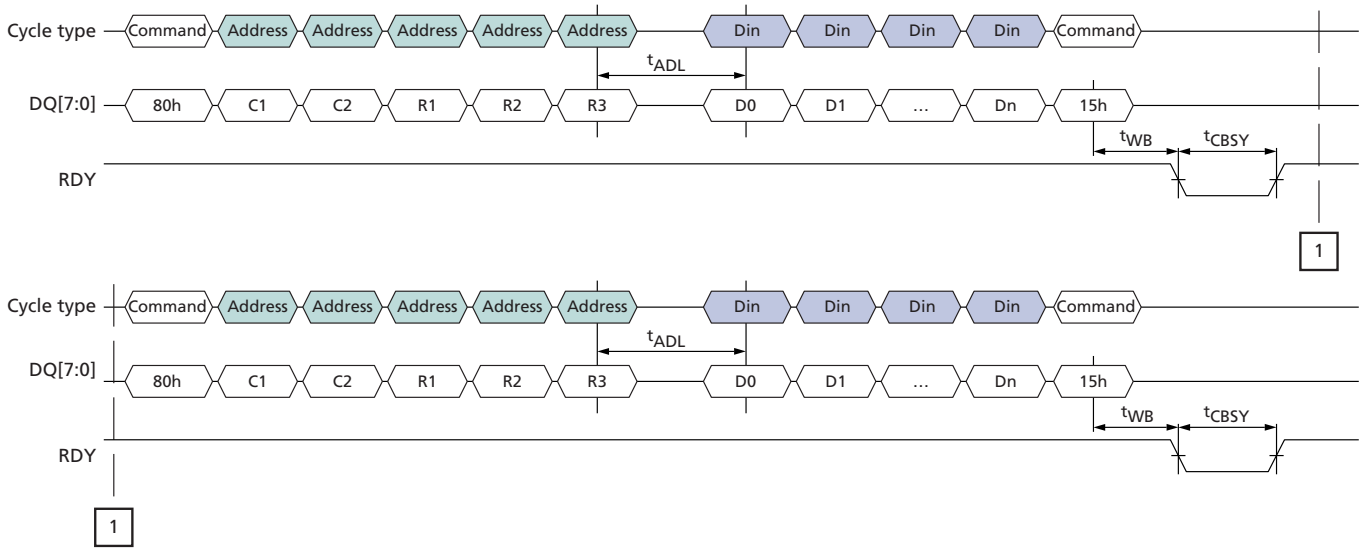
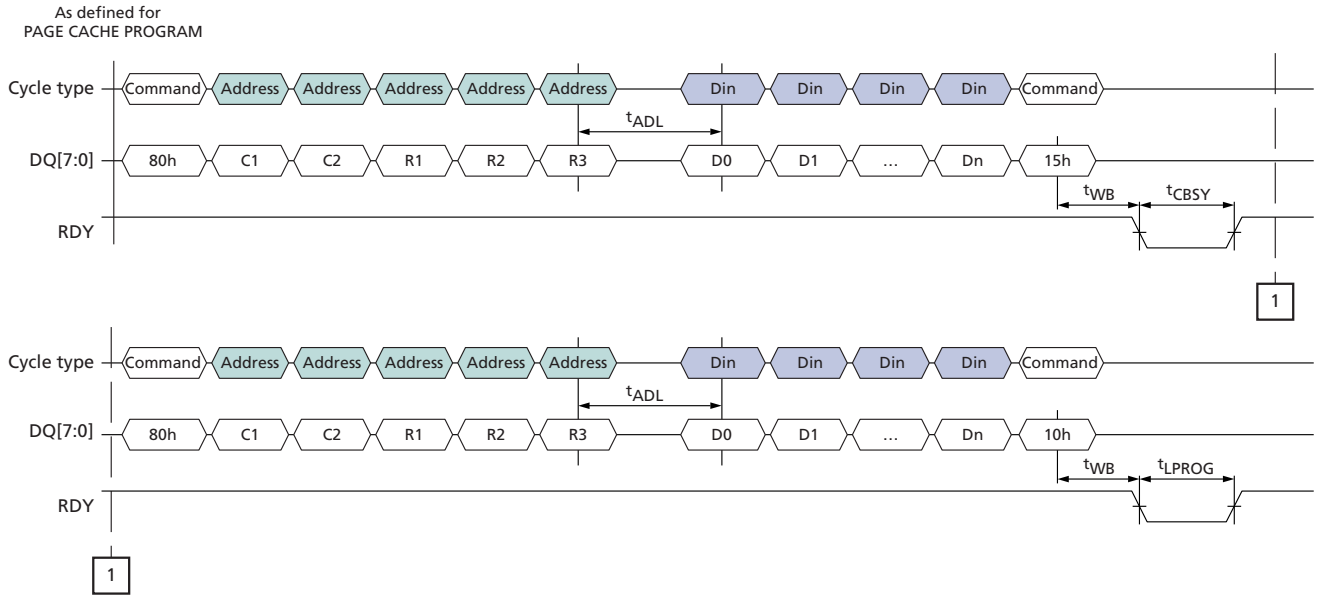


Figure 83: PROGRAM PAGE CACHE (80h–15h) Operation (End)



PROGRAM PAGE MULTI-PLANE (80h-11h)

The PROGRAM PAGE MULTI-PLANE (80h-11h) command enables the host to input data to the addressed plane's cache register and queue the cache register to ultimately be moved to the NAND Flash array. This command can be issued one or more times. Each time a new plane address is specified that plane is also queued for data transfer. To input data for the final plane and to begin the program operation for all previously queued planes, issue either the PROGRAM PAGE (80h-10h) command or the PROGRAM PAGE CACHE (80h-15h) command. All of the queued planes will move the data to the NAND Flash array. This command is accepted by the die (LUN) when it is ready (RDY = 1).

To input a page to the cache register and queue it to be moved to the NAND Flash array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by an 11h command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Write five address cycles containing the column address and row address for a lower page; data input cycles follow for the lower page. Serial data is input beginning at the column address specified. At any time during the data input cycle, the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands can be issued. When data input is complete, write 11h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}DBSY.

To determine the progress of ^{t}DBSY, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 71h, 78h) can be used.

When the LUN's status shows that it is ready (RDY = 1) and the lower page data is committed for the first NAND plane enter, write another 80h to the command register and then write five address cycles containing the column address and row address of the lower page address of another NAND plane. Data input cycles follow for the lower page

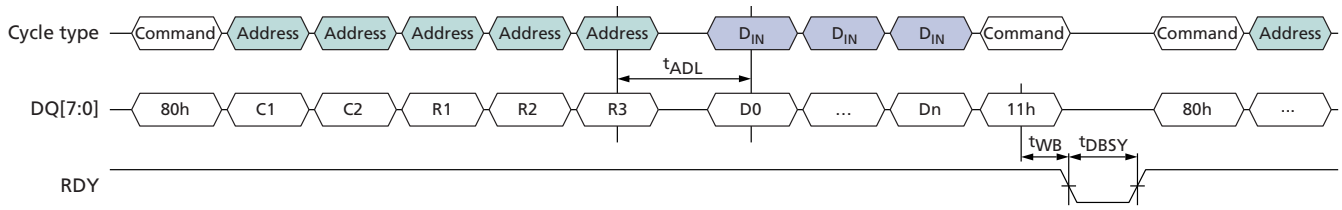
address of the NAND plane. Serial data is input beginning at the column address specified. At any time during the data input cycle the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands may be issued. When data input is complete, write 11h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}DBSY.

When the PROGRAM PAGE (80h-10h) command is used as the final command of a multi-plane program operation, data is transferred from the cache registers to the NAND Flash array for all of the addressed planes during ^{t}PROG. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the status of the FAIL bit for each of the planes to verify that programming completed successfully

When the PROGRAM PAGE CACHE (80h-15h) command is used in place of the PROGRAM PAGE (80h-10h) comamnd, the final command of a MULTI-PLANE PROGRAM CACHE operation, data is transferred from the cache registers to the data registers after the previous array operations finish. The data is then moved from the data registers to the NAND Flash array for all of the addressed planes. This occurs during ^{t}CBSY. After ^{t}CBSY, the host should check the status of the FAILC bit for each of the planes from the previous program cache operation, if any, to verify that programming completed successfully.

For the PROGRAM PAGE MULTI-PLANE (80h-11h), PROGRAM PAGE (80h-10h), and PROGRAM PAGE CACHE (80h-15h) commands, see Multi-Plane Operations for multi-plane addressing requirements.

Figure 84: PROGRAM PAGE MULTI-PLANE (80h–11h) Operation



For JEDEC compliance the PROGRAM PAGE MULTI-PLANE (81h-11h) command is also supported. This would also include the last command 81h-10h to conclude a PROGRAM PAGE MULTI-PLANE sequence and 81h-15h to conclude a PROGRAM PAGE CACHE MULTI-PLANE sequence.

PROGRAM SUSPEND (84h) and PROGRAM RESUME (13h)

The PROGRAM SUSPEND (84h) command is used to pause a program in execution for the LUN specified (RDY = 0, ARDY = 0 or RDY = 1, ARDY = 0). If a PROGRAM SUSPEND (84h) command is issued when RDY (SR[6]) is set to one or zero and ARDY (SR[5]) is set to one or zero and the LUN is not performing a program operation then the PROGRAM SUSPEND (84h) command should be ignored (i.e. ^{t}PSPDN = 0). If a multi-plane program is executing, the program operation for all multi-plane addresses is paused and the LUN shall make forward progress for the program operation prior to suspending the operation.

The SUSPEND (SR[2]) bit of the status register is valid for this command after ARDY transitions from zero to one and until the suspended program is resumed or RESET (FFh, FCh, FAh, FDh) is issued. The FAIL (SR[0]) bit of the status register is valid for this command after ARDY transitions from zero to one until the next transition of ARDY to zero. SUSPEND shall be set to one if a program was suspended successfully, in this case FAIL (SR[0]) shall be cleared to zero. SR[2] shall be cleared to zero if the program was completed, in this case SR[0] reflects whether the program was successful.

Table 44: PROGRAM SUSPEND (84h) Status Details

Description	SR[2]	SR[0]
PROGRAM completed with successful status	0	0
PROGRAM completed with fail status	0	1
PROGRAM suspended	1	0
Reserved	1	1

To suspend an ongoing program operation to a LUN, issue 84h command, then write five address cycles containing the row address; the block, page, and column addresses are ignored. The selected LUN status will be reflected in the status bits FAIL (SR[0]) and SUSPEND (SR[2]) in the status register after the status bit RDY is set to one. The selected LUN which the program operation was suspended on will respond within ^{t}PSPD.

If issuing a program command while an erase operation on the same LUN is suspended, the program operation is not allowed to be suspended.

To resume a suspended program operation to a LUN, issue 13h command, then write five address cycles containing the row address matching the LUN in the suspended state; the block, page, and column addresses are ignored. The suspended program operation will then resume and finish within ^{t}PROG.

While a program is suspended, if the host issues a RESET (FFh, FCh, FAh, FDh) command for the affected LUN, then the program that was suspended is canceled and status is cleared. With the exception of Erase and Program commands, all commands are allowed during suspended state (some with limitations listed in subsequent paragraphs). SET FEATURES (EFh) and SET FEATURES by LUN (D5h) commands are permitted during program suspend.

Cache read operations and Read Retry options that have a longer ^{t}R time are not premitted to be issued to a LUN that is in the program suspend state.

While a program is suspended on a LUN, if host issues a program (80h/81h-10h, 80h/81h-15h, 85h-10h) based command (regardless of the address) to the suspended LUN, the program command is not accepted by the LUN (R/B# goes LOW for ^{t}PSPDN) the

LOCK status (SR[7] = 0) is set and the program that was suspended keeps it's suspend state and can still be resumed. If a program based command is issued to a different LUN on the shared target then the program is performed on the selected page and the program that was suspended keeps its suspend state.

While a program is suspended, if host issues a read (00h-30h, 00h-31h, 00h-35h, 31h, 3Fh) based command to the page address (or shared WL) of the suspended program the read will be performed with data output being undefined and the program that was suspended keeps its suspend state. If host issues read command to block or LUN address other than the suspended page address then the read is performed and the program that was suspended keeps it's suspend state.

If the host issues a PROGRAM SUSPEND (84h) while there is no program operation ongoing the command should be ignored (i.e. ^{t}PSPD = 0). If the host issues a PROGRAM RESUME (13h) while there is no program operation ongoing or no program suspended, the NAND will respond with a ^{t}PSPDN busy time. If the host issues a PROGRAM SUSPEND (84h) to a LUN already in program suspend state the NAND will respond within ^{t}PSPDN busy time and the program that was suspended will stay in the program suspend state.

There are special circumstances if a PROGRAM SUSPEND (84h) is issued during CACHE PROGRAM operation. In order to prevent loss of data that is currently stored in the NAND cache register a longer ^{t}PSPD may result when the suspend command is issued. A CACHE PROGRAM operation allows data entry of the next page data during array programming. The NAND must wait until the current array program operation has resources available to store the data in the cache register. A longer ^{t}PSPD may result as the NAND completes the array program to ensure the resources are available to store the cache register contents. This allows the host to continue cache programming upon issuing the PROGRAM RESUME (13h) command with no data loss or additional data entry required.

Program suspend operations are only supported in the default mode of operation (i.e. not in the OTP mode of operation).

Figure 85: PROGRAM SUSPEND (84h) Operation

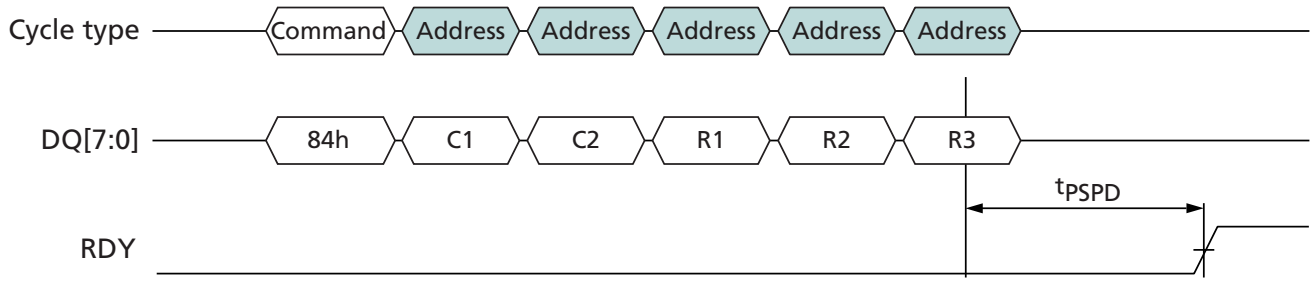
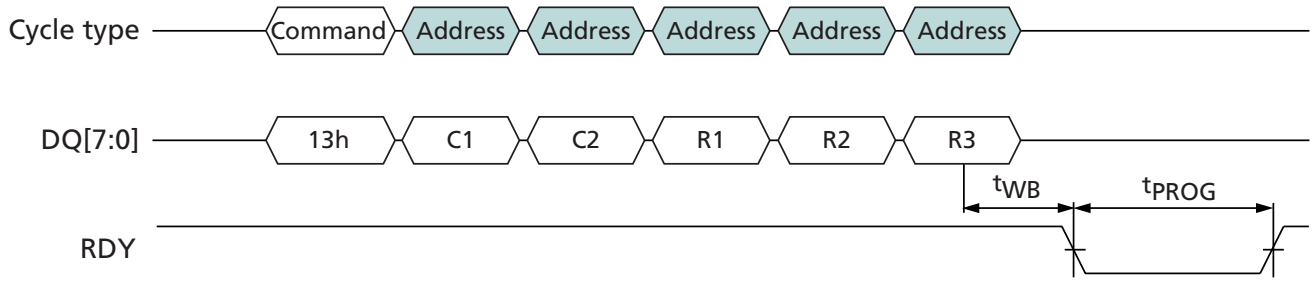


Figure 86: PROGRAM RESUME (13h) Operation



Erase Operations

Erase operations are used to clear the contents of a block in the NAND Flash array to prepare its pages for program operations.

Erase Operations

The ERASE BLOCK (60h-D0h) command, when not preceded by the ERASE BLOCK MULTI-PLANE (60h-D1h) command, erases one block in the NAND Flash array. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

MULTI-PLANE ERASE Operations

The ERASE BLOCK MULTI-PLANE (60h-D1h) command can be used to further system performance of erase operations by allowing more than one block to be erased in the NAND array. This is done by prepending one or more ERASE BLOCK MULTI-PLANE (60h-D1h) commands in front of the ERASE BLOCK (60h-D0h) command. See Multi-Plane Operations for details.

ERASE BLOCK (60h-D0h)

The ERASE BLOCK (60h-D0h) command erases the specified block in the NAND Flash array. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

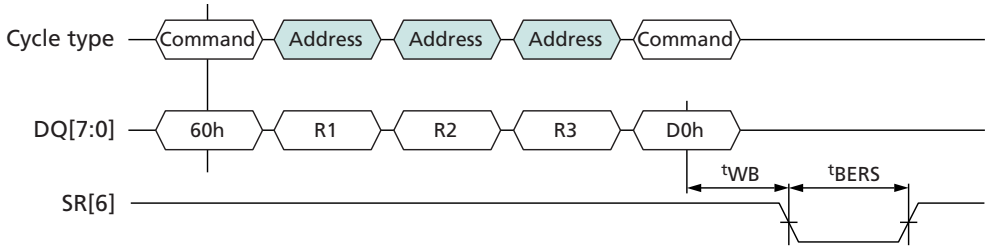
To erase a block, write 60h to the command register. Then write three address cycles containing the row address; the page address is ignored. Conclude by writing D0h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}BERS while the block is erased.

To determine the progress of an ERASE operation, the host can monitor the target's R/B# signal, or alternatively, the status operations (70h, 78h) can be used. When the die (LUN) is ready (RDY = 1, ARDY = 1) the host should check the status of the FAIL bit.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

The ERASE BLOCK (60h-D0h) command is used as the final command of a MULTI-PLANE ERASE operation. It is preceded by one or more ERASE BLOCK MULTI-PLANE (60h-D1h) commands. All of blocks in the addressed planes are erased. The host should check the status of the operation by using the status operations (70h, 78h). See Multi-Plane Operations for multi-plane addressing requirements.

Figure 87: ERASE BLOCK (60h-D0h) Operation



ERASE BLOCK MULTI-PLANE (60h-D1h)

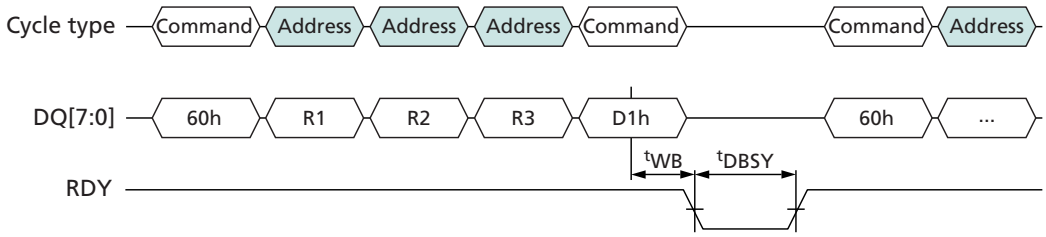
The ERASE BLOCK MULTI-PLANE (60h-D1h) command queues a block in the specified plane to be erased in the NAND Flash array. This command can be issued one or more times. Each time a new plane address is specified, that plane is also queued for a block to be erased. To specify the final block to be erased and to begin the ERASE operation for all previously queued planes, issue the ERASE BLOCK (60h-D0h) command. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

To queue a block to be erased, write 60h to the command register, then write three address cycles containing the row address; the page address is ignored. Conclude by writing D1h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}DBSY.

To determine the progress of ^{t}DBSY, the host can monitor the target's R/B# signal, or alternatively, the status operations (70h, 78h) can be used. When the LUN's status shows that it is ready (RDY = 1, ARDY = 1), additional ERASE BLOCK MULTI-PLANE (60h-D1h) commands can be issued to queue additional planes for erase. Alternatively, the ERASE BLOCK (60h-D0h) command can be issued to erase all of the queued blocks.

For multi-plane addressing requirements for the ERASE BLOCK MULTI-PLANE (60h-D1h) and ERASE BLOCK (60h-D0h) commands, see Multi-Plane Operations.

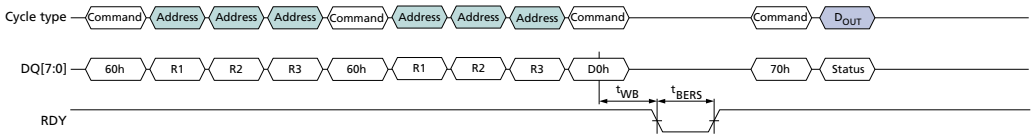
Figure 88: ERASE BLOCK MULTI-PLANE (60h–D1h) Operation



ERASE BLOCK MULTI-PLANE (60h-60h-D0h)

This operation behaves the same as the ERASE BLOCK MULTI-PLANE (60h-D1h) command followed by a ERASE BLOCK (60h-D0h) command.

Figure 89: ERASE BLOCK MULTI-PLANE (60h–60h-D0h) Operation



ERASE SUSPEND (61h) and ERASE RESUME (D2h)

The ERASE SUSPEND (61h) command is used to pause an erase in execution for the LUN specified (RDY =0, ARDY = 0). If ERASE SUSPEND (61h) is issued when ARDY = 1 or 0 and LUN is not performing an erase operation then the ERASE SUSPEND (61h) command should be ignored (i.e. ^{t}ESPD = 0). If an interleaved erase is executing (erase operations on more than one LUN on a target), the erase for the addressed LUN with the ERASE SUSPEND (61h) command is paused. The LUN shall make forward progress for the erase prior to suspending (e.g. complete an erase pulse). Since the erase is resumed

from where it left off, an ERASE RESUME (D2h) on suspended block will count as one erase cycle. For example, if an erase is suspended and resumed twice it will count as three P/E cycles.

FAIL (SR[0]) and SUSPEND (SR[2]) of the status register are valid for this command after RDY transitions from zero to one until the next transition of RDY to zero. SR[2] shall be set to one if an erase was suspended successfully, in this case SR[0] shall be cleared to zero. SR[2] shall be cleared to zero if the erase was completed, in this case SR[0] reflects whether the erase was successful.

To suspend a ongoing erase operation to a LUN, write 61h to the command register, then write three address cycles containing the row address; the page address is ignored. The selected LUN status will be reflected in the status bits FAIL (SR[0]) and SUSPEND (SR[2]) in the status register after the status bit RDY (SR[6]) is set to one.

Table 45: ERASE SUSPEND (61h) Status Details

Description	SR[2]	SR[0]
ERASE completed with successful status	0	0
ERASE completed with fail status	0	1
ERASE suspended	1	0
Reserved	1	1

For multi-plane addressing requirements for the ERASE BLOCK MULTI-PLANE (60h-D1h) and ERASE BLOCK (60h-D0h) commands, see Multi-Plane Operations.

To resume a suspended erase operation issue the ERASE RESUME (D2h) command to the command register for the target (CE#) which has had an erase operation suspended. The suspended erase operation will then resume and finish within ^{t}BERS. In the case of Multi-LUN erase operations that have been suspended, the ERASE RESUME (D2h) command will cause all LUNs on a target (CE#) to resume any suspended erase operations.

While an erase is suspended, if the host issues a RESET (FFh, FCh, FAh) command for the affected LUN then the erase that was suspended is canceled and status is cleared. All commands are accepted during suspended state (some with limitations listed in subsequent paragraphs).

While an erase is suspended, if host issues a ERASE BLOCK (60h-D0h) command to the suspended block the suspended erase will be resumed (not restarted) and the erase that was suspended is canceled and status is cleared. If block erase is issued to different block address than suspended block then the erase is performed on the selected block and the erase that was suspended is canceled and status is cleared. If an erase is issued to a different LUN on the shared target then the erase is performed on the selected block and the erase that was suspended keeps it's suspend state.

Table 46: ERASE SUSPEND (61h) behavior for ERASE operations

Description	Command Issued	Next State
Block A erase operation suspended	ERASE BLOCK to Block A	Resume erase operation to Block A
	ERASE BLOCK to Block B	Start normal erase to Block B and suspend to Block A is canceled
	ERASE BLOCK MULTI-PLANE to Block A and B	Start normal erase to Block A and B
ERASE BLOCK MULTI-PLANE to Block A and B suspended	ERASE BLOCK to Block A	Resume erase operation to Block A and B
	ERASE BLOCK to Block B	Resume erase operation to Block A and B
	ERASE BLOCK MULTI-PLANE to Block A and B	Resume erase operation to Block A and B
	ERASE BLOCK MULTI-PLANE to Block A and D	Start normal erase to block A and D. Suspend to Block B is canceled
	ERASE BLOCK MULTI-PLANE to Block C and B	Start normal erase to block C and B. Suspend to Block A is canceled

While an erase is suspended, if host issues a program command to the suspended block or in the case of multi-plane program, if at least one of the blocks addressed has a suspended erase, the program is aborted with short busy time (^{t}ESPDN) and the LOCK status (SR[7] = 0) is set. In this case, the erase that was suspended keeps it's suspend state and can still be resumed. If host issues a program command to a block or LUN address other than the suspended block, also in case of a multi-plane program operation, as long as the suspended block is not one of the addressed blocks, then the program is performed and the erase that was suspended keeps it's suspend state. The program operation is not allowed to be suspended while there is a erase suspended for a given LUN that is in the erase suspend state.

While an erase is suspended, if host issues a read command to the suspended block the read will be performed (undefined data read out) and the erase that was suspended keeps it's suspend state. If host issues read command to block or LUN address other than the suspended block then the read is performed and the erase that was suspended keeps it's suspend state.

If the host issues an ERASE SUSPEND (61h) command while there is no erase operation ongoing the command should be ignored (i.e. ^{t}ESPD = 0). If the host issues an ERASE RESUME (D2h) command while there is no erase operation ongoing or no erase suspended, the NAND will respond with a ^{t}ESPDN busy time. If the host issues an ERASE SUSPEND (61h) to a LUN already in erase suspend state, the command will be ignored and the erase that was suspended will stay in the erase suspend state .

It is recommended for forward progress to occur on a ERASE SUSPEND (61h) operation, the host should not issue two consecutive ERASE SUPSEND (61h) commands within

1ms of each other. If repeated ERASE SUSPEND (61h) commands are issued less than 1ms apart the erase operation may not complete.

Figure 90: ERASE SUSPEND (61h) Operation

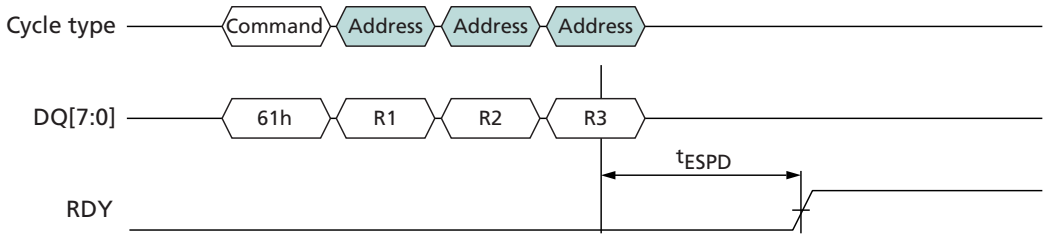
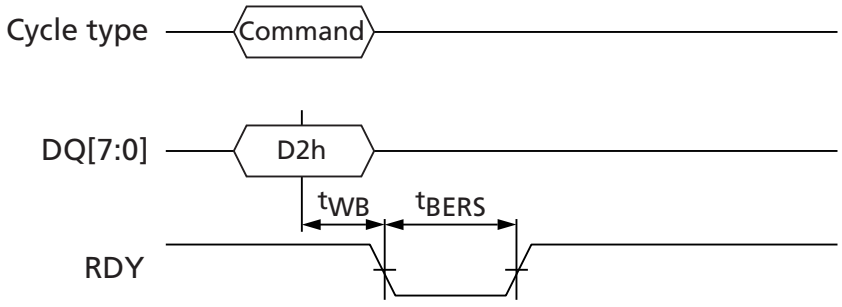


Figure 91: ERASE RESUME (D2h) Operation



Copyback Operations

COPYBACK operations make it possible to transfer data within a plane from one page to another using the cache register. This is particularly useful for block management and wear leveling.

The COPYBACK operation is a two-step process consisting of a COPYBACK READ (00h-35h) and a COPYBACK PROGRAM (85h-10h) command. To move data from one page to another on the same plane, first issue the COPYBACK READ (00h-35h) command. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host can transfer the data to a new page by issuing the COPYBACK PROGRAM (85h-10h) command. When the die (LUN) is again ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

To prevent bit errors from accumulating over multiple COPYBACK operations, it is recommended that the host read the data out of the cache register after the COPYBACK READ (00h-35h) completes prior to issuing the COPYBACK PROGRAM (85h-10h) command. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address. The host should check the data for ECC errors and correct them. When the COPYBACK PROGRAM (85h-10h) command is issued, any corrected data can be input. The CHANGE ROW ADDRESS (85h) command can be used to change the column address.

It is not possible to use the COPYBACK operation to move data from one plane to another or from one die (LUN) to another. Instead, use a READ PAGE (00h-30h) or COPYBACK READ (00h-35h) command to read the data out of the NAND, and then use a PROGRAM PAGE (80h-10h) command with data input to program the data to a new plane or die (LUN).

Between the COPYBACK READ (00h-35h) and COPYBACK PROGRAM (85h-10h) commands, the following commands are supported: status operations (70h, 78h), and column address operations (05h-E0h, 06h-E0h, 85h). Reset operations (FFh, FCh) can be issued after COPYBACK READ (00h-35h), but the contents of the cache registers on the target are not valid.

In devices which have more than one die (LUN) per target, once the COPYBACK READ (00h-35h) is issued, interleaved die (multi-LUN) operations are prohibited until after the COPYBACK PROGRAM (85h-10h) command is issued.

Multi-Plane Copyback Operations

Multi-plane copyback read operations improve read data throughput by copying data simultaneously from more than one plane to the specified cache registers. This is done by prepending one or more READ PAGE MULTI-PLANE (00h-32h) commands in front of the COPYBACK READ (00h-35h) command.

The COPYBACK PROGRAM MULTI-PLANE (85h-11h) command can be used to further system performance of COPYBACK PROGRAM operations by enabling movement of multiple pages from the cache registers to different planes of the NAND Flash array. This is done by prepending one or more COPYBACK PROGRAM (85h-11h) commands in front of the COPYBACK PROGRAM (85h-10h) command. See Multi-Plane Operations for details.

COPYBACK READ (00h-35h)

The COPYBACK READ (00h-35h) command is functionally identical to the READ PAGE (00h-30h) command, except that 35h is written to the command register instead of 30h. See READ PAGE (00h-30h) (page 152) for further details.

Though it is not required, it is recommended that the host read the data out of the device to verify the data prior to issuing the COPYBACK PROGRAM (85h-10h) command to prevent the propagation of data errors.

Figure 92: COPYBACK READ (00h-35h) Operation

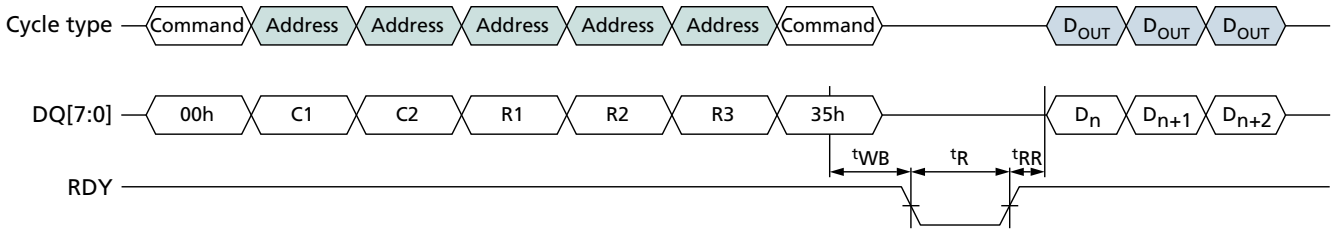
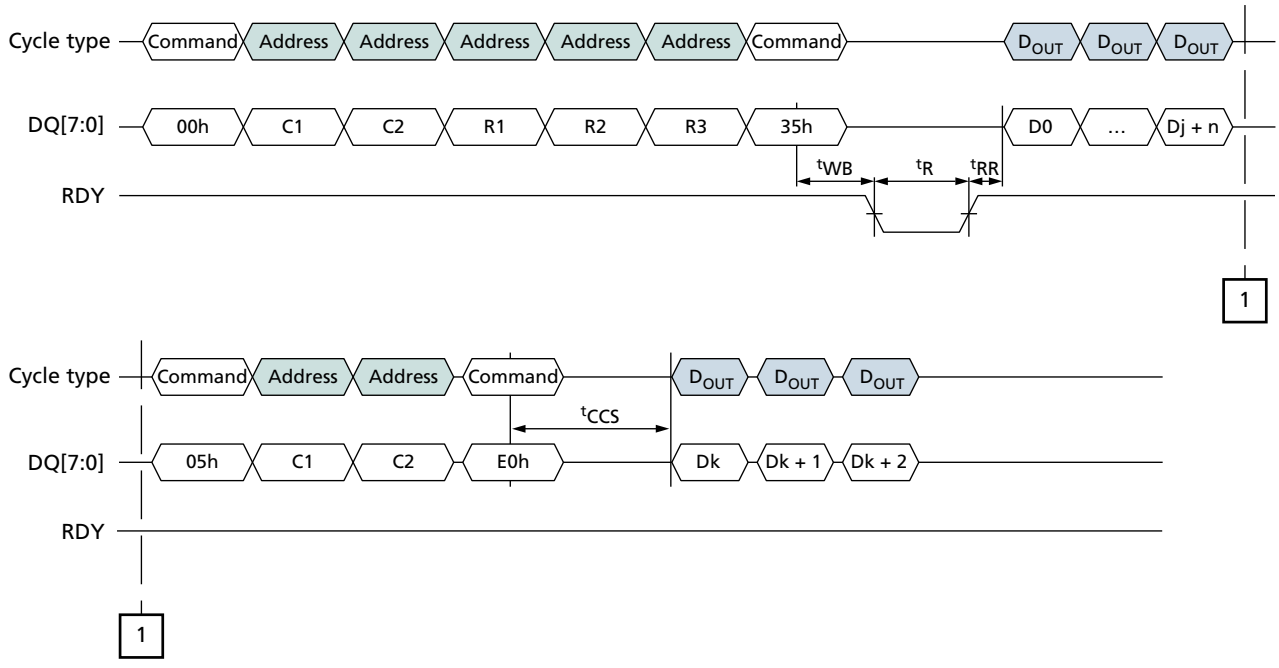


Figure 93: COPYBACK READ (00h–35h) with CHANGE READ COLUMN (05h–E0h) Operation



COPYBACK PROGRAM (85h–10h)

The COPYBACK PROGRAM (85h-10h) command is functionally identical to the PROGRAM PAGE (80h-10h) command, except that when 85h is written to the command register, cache register contents are not cleared. See PROGRAM PAGE (80h-10h) for further details.

Figure 94: COPYBACK PROGRAM (85h–10h) Operation

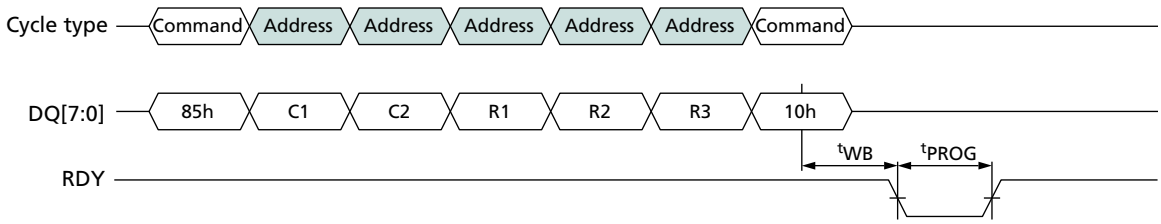
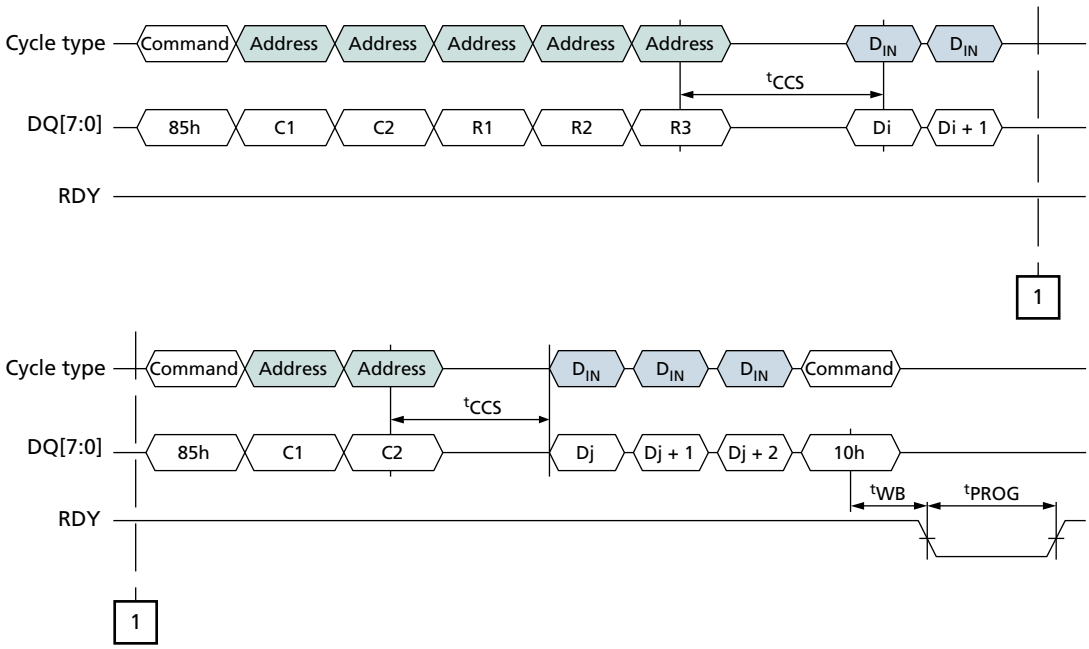


Figure 95: COPYBACK PROGRAM (85h-10h) with CHANGE WRITE COLUMN (85h) Operation



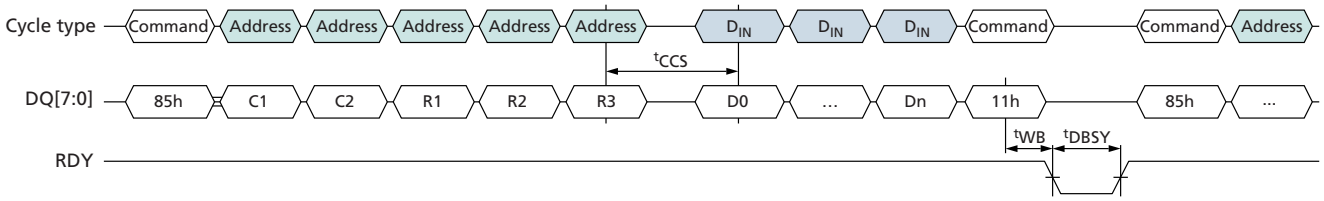
COPYBACK READ MULTI-PLANE (00h-32h)

The COPYBACK READ MULTI-PLANE (00h-32h) command is functionally identical to the READ PAGE MULTI-PLANE (00h-32h) command, except that the 35h command is written as the final command. The complete command sequence for the COPYBACK READ PAGE MULTI-PLANE is 00h-32h-00h-35h. See READ PAGE MULTI-PLANE (00h-32h) (page 157) for further details.

COPYBACK PROGRAM MULTI-PLANE (85h-11h)

The COPYBACK PROGRAM MULTI-PLANE (85h-11h) command is functionally identical to the PROGRAM PAGE MULTI-PLANE (80h-11h) command, except that when 85h is written to the command register, cache register contents are not cleared. See PROGRAM PAGE MULTI-PLANE (80h-11h) for further details.

Figure 96: COPYBACK PROGRAM MULTI-PLANE (85h-11h) Operation



One-Time Programmable (OTP) Operations

This Micron NAND Flash device offers a protected, one-time programmable NAND Flash memory area. Each target has a an OTP area with a range of OTP pages (see Table 47 (page 181)); the entire range is guaranteed to be good. Customers can use the OTP area in any way they desire; typical uses include programming serial numbers or other data for permanent storage.

The OTP area leaves the factory in an erased state (all bits are 1). Programming an OTP page changes bits that are 1 to 0, but cannot change bits that are 0 to 1. The OTP area cannot be erased, even if it is not protected. Protecting the OTP area prevents further programming of the pages in the OTP area.

Enabling the OTP Operation Mode

The OTP area is accessible while the OTP operation mode is enabled. To enable OTP operation mode, issue the SET FEATURES (EFh) command to feature address 90h and write 01h to P1, followed by three cycles of 00h to P2 through P4.

When the target is in OTP operation mode, all subsequent PAGE READ (00h-30h) and PROGRAM PAGE (80h-10h) commands are applied to the OTP area.

ERASE commands are not valid while the target is in OTP operation mode.

Programming OTP Pages

Each page in the OTP area is programming using the PROGRAM OTP PAGE (80h-10h) command. Each page can be programmed more than once, in sections, up to the maximum number allowed (see NOP in Table 47 (page 181)). The pages in the OTP area must be programmed in ascending order.

If the host issues a PAGE PROGRAM (80h-10h) command to an address beyond the maximum page-address range, the target will be busy for ^{t}OBSY and the WP# status register bit will be 0, meaning that the page is write-protected.

Protecting the OTP Area

To protect the OTP area, issue the OTP PROTECT (80h-10h) command to the OTP Protect Page. When the OTP area is protected it cannot be programmed further. It is not possible to unprotect the OTP area after it has been protected.

Reading OTP Pages

To read pages in the OTP area, whether the OTP area is protected or not, issue the PAGE READ (00h-30h) command.

If the host issues the PAGE READ (00h-30h) command to an address beyond the maximum page-address range, the data output will not be valid. To determine whether the target is busy during an OTP operation, either monitor R/B# or use the READ STATUS (70h) command. Use of the READ STATUS ENHANCED (78h) command is prohibited while the OTP operation is in progress.

Returning to Normal Array Operation Mode

To exit OTP operation mode and return to normal array operation mode, issue the SET FEATURES (EFh) command to feature address 90h and write 00h to P1 through P4.

If the RESET (FFh) command is issued while in OTP operation mode, the target will exit OTP operation mode and enter normal operating mode. If the synchronous interface is active, the target will exit OTP operation and enable the asynchronous interface.

If the SYNCHRONOUS RESET (FCh) command is issued while in the OTP operation mode, the target will exit OTP operation mode and the synchronous interface remains active.

Table 47: OTP Area Details

Description	Value
Number of OTP pages	28
OTP protect page address	01h
OTP start page address	03h
Number of partial page programs (NOP) to each OTP page	2

PROGRAM OTP PAGE (80h-10h)

The PROGRAM OTP PAGE (80h-10h) command is used to write data to the pages within the OTP area. To program data in the OTP area, the target must be in OTP operation mode.

To use the PROGRAM OTP PAGE (80h-10h) command, issue the 80h command. Issue five address cycles including the column address, the page address within the OTP page range, and a block address of 0. Next, write the data to the cache register using data input cycles. After data input is complete, issue the 10h command.

R/B# goes LOW for the duration of the array programming time, ^{t}PROG. The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. The RDY bit of the status register will reflect the state of R/B#. Use of the READ STATUS ENHANCED (78h) command is prohibited.

When the target is ready, read the FAIL bit of the status register to determine whether the operation passed or failed (see Status Operations).

The PROGRAM OTP PAGE (80h-10h) command also accepts the CHANGE WRITE COLUMN (85h) command during data input.

If a PROGRAM PAGE command is issued to the OTP area after the area has been protected, then R/B# goes LOW for ^{t}OBSY. After ^{t}OBSY, the status register is set to 60h.

Figure 97: PROGRAM OTP PAGE (80h-10h) Operation

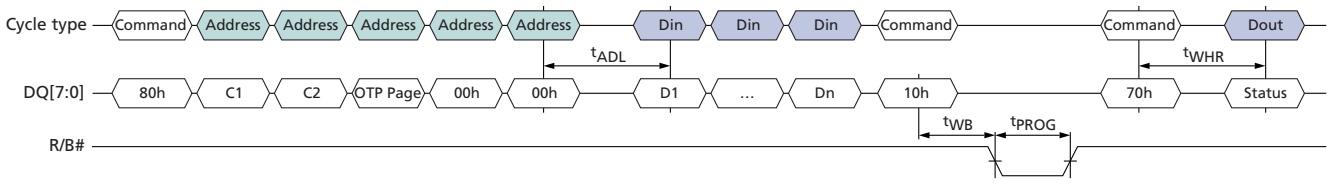
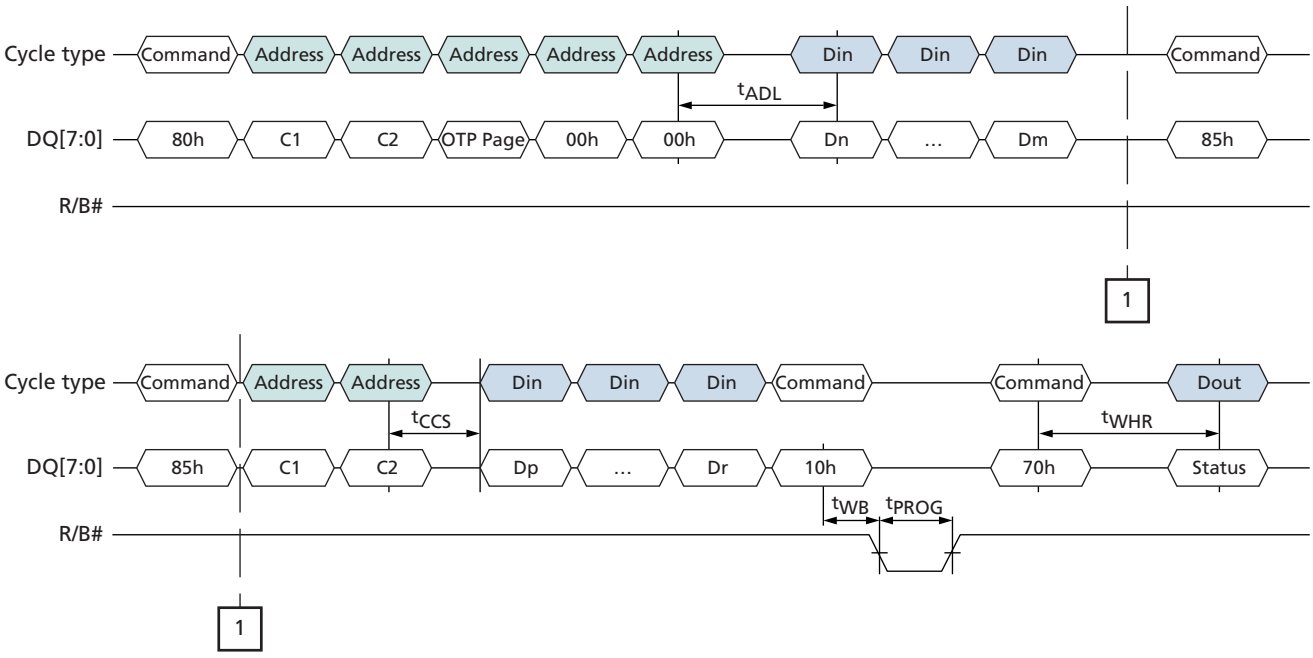


Figure 98: PROGRAM OTP PAGE (80h-10h) with CHANGE WRITE COLUMN (85h) Operation



PROTECT OTP AREA (80h-10h)

The PROTECT OTP AREA (80h-10h) command is used to prevent further programming of the pages in the OTP area. The protect the OTP area, the target must be in OTP operation mode.

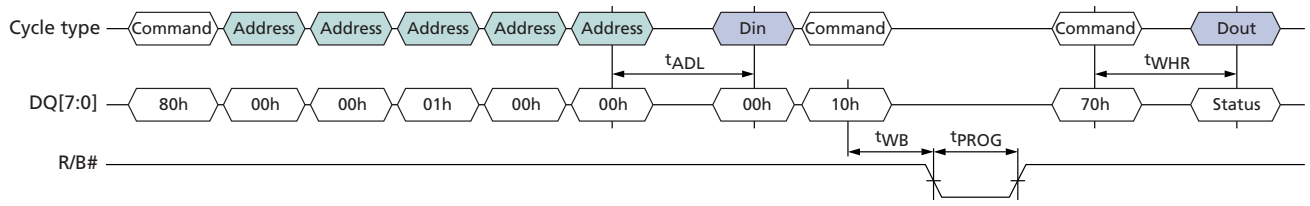
To protect all data in the OTP area, issue the 80h command. Issue five address cycles including the column address, OTP protect page address and block address; the column and block addresses are fixed to 0. Next, write 00h data for the first byte location and issue the 10h command.

R/B# goes LOW for the duration of the array programming time, ^{t}PROG. The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. The RDY bit of the status register will reflect the state of R/B#. Use of the READ STATUS ENHANCED (78h) command is prohibited.

When the target is ready, read the FAIL bit of the status register to determine if the operation passed or failed (see Status Operations).

If the PROTECT OTP AREA (80h-10h) command is issued after the OTP area has already been protected, R/B# goes LOW for ^{t}OBSY. After ^{t}OBSY, the status register is set to 60h.

Figure 99: PROTECT OTP AREA (80h-10h) Operation



Note: 1. OTP data is protected following a status confirmation.

READ OTP PAGE (00h-30h)

The READ OTP PAGE (00h-30h) command is used to read data from the pages in the OTP area. To read data in the OTP area, the target must be in OTP operation mode.

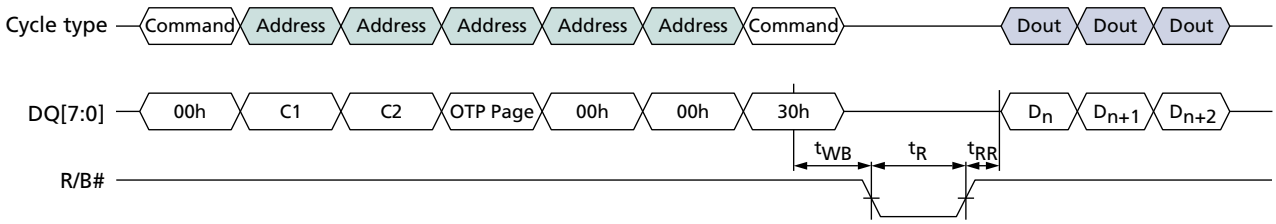
To use the READ OTP PAGE (00h-30h) command, issue the 00h command. Issue five address cycles including the column address, the page address within the OTP page range, and a block address of 0. Next, issue the 30h command. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for tR as data is transferred.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal, or alternatively the READ STATUS (70h) command can be used. If the status operations are used to monitor the die's (LUN's) status, when the die (LUN) is ready (RDY = 1, ARDY = 1) the host disables status output and enables data output by issuing the READ MODE (00h) command. When the host requests data output, it begins at the column address specified.

Additional pages within the OTP area can be read by repeating the READ OTP PAGE (00h-30h) command.

The READ OTP PAGE (00h-30h) command is compatible with the CHANGE READ COLUMN (05h-E0h) command. Use of the READ STATUS ENHANCED (78h) and CHANGE READ COLUMN ENHANCED (06h-E0h) commands are prohibited.

Figure 100: READ OTP PAGE (00h-30h) Operation



Multi-Plane Operations

Each NAND Flash logical unit (LUN) is divided into multiple physical planes. Each plane contains a cache register and a data register independent of the other planes. The planes are addressed via the low-order block address bits. Specific details are provided in Device and Array Organization.

Multi-plane operations make better use of the NAND Flash arrays on these physical planes by performing concurrent READ, PROGRAM, or ERASE operations on multiple planes, significantly improving system performance. Multi-plane operations must be of the same type across the planes; for example, it is not possible to perform a PROGRAM operation on one plane with an ERASE operation on another.

When issuing MULTI-PLANE PROGRAM operations, use the READ STATUS (70h) command and check whether the previous operation(s) failed. If the READ STATUS (70h) command indicates that an error occurred (FAIL = 1 and/or FAILC = 1), use the READ STATUS ENHANCED (78h) command—time for each plane—to determine which plane operation failed.

When issuing MULTI-PLANE ERASE operations, use the READ STATUS (70h) command and check whether the previous operation(s) failed. If the READ STATUS (70h) command indicates that an error occurred (FAIL = 1), use the READ STATUS ENHANCED (78h) command—time for each plane—to determine which plane operation failed.

Multi-Plane Addressing

Multi-plane commands require an address per operational plane. For a given multi-plane operation, these addresses are subject to the following requirements.

- The LUN address bit must be identical for all of the issued addresses.
- The plane select bits, BA[11] and BA[10], must be different for each issued address.
- The page address bits, PA[9:0], must be identical for each issued address.

The READ STATUS (70h) command should be used following MULTI-PLANE PROGRAM PAGE and ERASE BLOCK operations on a single die (LUN).

Interleaved Die (Multi-LUN) Operations

In devices that have more than one die (LUN) per target, it is possible to improve performance by interleaving operations between the die (LUNs). An interleaved die (multi-LUN) operation is one that individual die (LUNs) involved may be in any combination of busy or ready status during operations.

Interleaved die (multi-LUN) operations are prohibited following RESET (FFh, FCh), identification (90h, ECh, EDh), and configuration (EEh, EFh) operations until ARDY =1 for all of the die (LUNs) on the target.

During an interleaved die (multi-LUN) operation, there are two methods to determine operation completion. The R/B# signal indicates when all of the die (LUNs) have finished their operations. R/B# remains LOW while any die (LUN) is busy. When R/B# goes HIGH, all of the die (LUNs) are idle and the operations are complete. Alternatively, the READ STATUS ENHANCED (78h) command can report the status of each die (LUN) individually.

If a die (LUN) is performing a cache operation, like PROGRAM PAGE CACHE (80h-15h), then the die (LUN) is able to accept the data for another cache operation when status register bit 6 is 1. All operations, including cache operations, are complete on a die when status register bit 5 is 1.

Use the READ STATUS ENHANCED (78h) command to monitor status for the addressed die (LUN). When multi-plane commands are used with interleaved die (multi-LUN) operations, the multi-plane commands must also meet the requirements, see Multi-Plane Operations for details. After the READ STATUS ENHANCED (78h) command has been issued, the READ STATUS (70h) command may be issued for the previously addressed die (LUN).

See Command Definitions for the list of commands that can be issued while other die (LUNs) are busy.

During an interleaved die (multi-LUN) operation that involves a PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operation and a READ operation, the PROGRAM-series operation must be issued before the READ-series operation. The data from the READ-series operation must be output to the host before the next PROGRAM-series operation is issued. This is because the 80h command clears the cache register contents of all cache registers on all planes.

During a interleaved die (multi-LUN) operation that involves PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operations between multiple die (LUNs) on the same target, after data is inputted to the first die (LUN) addressed in that interleaved die (multi-LUN) sequence, before addressing the next die (LUN) with a PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operation a program confirm command (via 80h-10h, 80-15h) must be issued to begin the array programming of the pervious die (LUN). If this is not done by the host prior to addressing the next die (LUN), data in all the cache registers of the previously die (LUNs) will be cleared by the PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operation to the next die (LUN) in the interleaved die (multi-LUN) sequence. Utilizing the Program Clear functionality in feature address 01h can be utilized to avoid a PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operation from clearing the contents of non-addressed NAND planes.

When issuing combinations of commands to multiple die (LUNs) (e.g. Reads to one die (LUN) and Programs to another die (LUN)) or Reads to one die (LUN) and Reads to another die (LUN)), the host shall issue the READ STATUS ENHANCED (78h) command

before reading data from any LUN. This ensures that only the LUN selected by the READ STATUS ENHANCED (78h) command responds to a data output cycle after being put into data output mode, and thus avoiding bus contention. After the READ STATUS ENHANCED (78h) command is issued to the selected die (LUN) a CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) command shall be issued prior to any data output from the selected die (LUN).

Error Management

Each NAND Flash die (LUN) is specified to have a minimum number of valid blocks (NVB) of the total available blocks. This means the die (LUNs) could have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional blocks can develop with use. However, the total number of available blocks per die (LUN) will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices could contain bad blocks, they can be used quite reliably in systems that provide bad-block management and error-correction algorithms. This type of software environment ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI Factory Defect Mapping requirements. See the following table for the first spare area location and the bad-block mark.

System software should check the first spare area location on the first page of each block prior to performing any PROGRAM or ERASE operations on the NAND Flash device. A bad block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks could be marginal, it may not be possible to recover this information if the block is erased.

Over time, some memory locations may fail to program or erase properly. In order to ensure that data is stored properly over the life of the NAND Flash device, the following precautions are required:

- Always check status after a PROGRAM or ERASE operation
- Under typical conditions, use the minimum required ECC (see table below)
- Use bad-block management and wear-leveling algorithms

The first block (physical block address 00h) for each CE# is guaranteed to be valid with ECC when shipped from the factory.

Table 48: Error Management Details

Description	Requirement
Minimum number of valid blocks (NVB) per LUN	2044
Total available blocks per LUN	2192
First spare area location	Byte 16,384
Bad-block mark	00h
Minimum required ECC	72-bit ECC per 1162 bytes of data

Shared Pages

In MLC NAND Flash devices, each memory cell contains two bits of data. These bits are distributed across two NAND pages. Pages within a NAND block that share the same NAND memory cells are referred to as shared pages. If any program operation is interrupted (e.g. power loss or reset), data in previously programmed shared pages can also be corrupted.

The least significant numbered shared page must be programmed before the most significant numbered page of that pair can be programmed.

Table 49: Shared Pages

Shared Pages		Shared Pages		Shared Pages		Shared Pages	
0	–	1	–	2	–	3	–
4	–	5	–	6	–	7	–
8	–	9	–	10	–	11	–
12	–	13	–	14	–	15	–
16	–	17	–	18	–	19	–
20	–	21	–	22	–	23	–
24	–	25	–	26	–	27	–
28	–	29	–	30	–	31	–
32	64	33	66	34	68	35	70
36	72	37	74	38	76	39	78
40	80	41	82	42	84	43	86
44	88	45	90	46	92	47	94
48	96	49	98	50	100	51	102
52	104	53	106	54	108	55	110
56	112	57	114	58	116	59	118
60	120	61	122	62	124	63	126
65	128	67	130	69	132	71	134
73	136	75	138	77	140	79	142
81	144	83	146	85	148	87	150
89	152	91	154	93	156	95	158
97	160	99	162	101	164	103	166
105	168	107	170	109	172	111	174
113	176	115	178	117	180	119	182
121	184	123	186	125	188	127	190
129	192	131	194	133	196	135	198
137	200	139	202	141	204	143	206
145	208	147	210	149	212	151	214
153	216	155	218	157	220	159	222
161	224	163	226	165	228	167	230
169	232	171	234	173	236	175	238

Table 49: Shared Pages (Continued)

Shared Pages		Shared Pages		Shared Pages		Shared Pages	
177	240	179	242	181	244	183	246
185	248	187	250	189	252	191	254
193	256	195	258	197	260	199	262
201	264	203	266	205	268	207	270
209	272	211	274	213	276	215	278
217	280	219	282	221	284	223	286
225	288	227	290	229	292	231	294
233	296	235	298	237	300	239	302
241	304	243	306	245	308	247	310
249	312	251	314	253	316	255	318
257	320	259	322	261	324	263	326
265	328	267	330	269	332	271	334
273	336	275	338	277	340	279	342
281	344	283	346	285	348	287	350
289	352	291	354	293	356	295	358
297	360	299	362	301	364	303	366
305	368	307	370	309	372	311	374
313	376	315	378	317	380	319	382
321	384	323	386	325	388	327	390
329	392	331	394	333	396	335	398
337	400	339	402	341	404	343	406
345	408	347	410	349	412	351	414
353	416	355	418	357	420	359	422
361	424	363	426	365	428	367	430
369	432	371	434	373	436	375	438
377	440	379	442	381	444	383	446
385	448	387	450	389	452	391	454
393	456	395	458	397	460	399	462
401	464	403	466	405	468	407	470
409	472	411	474	413	476	415	478
417	480	419	482	421	484	423	486
425	488	427	490	429	492	431	494
433	496	435	498	437	500	439	502
441	504	443	506	445	508	447	510
449	512	451	514	453	516	455	518
457	520	459	522	461	524	463	526
465	528	467	530	469	532	471	534
473	536	475	538	477	540	479	542

Table 49: Shared Pages (Continued)

Shared Pages		Shared Pages		Shared Pages		Shared Pages	
481	544	483	546	485	548	487	550
489	552	491	554	493	556	495	558
497	560	499	562	501	564	503	566
505	568	507	570	509	572	511	574
513	576	515	578	517	580	519	582
521	584	523	586	525	588	527	590
529	592	531	594	533	596	535	598
537	600	539	602	541	604	543	606
545	608	547	610	549	612	551	614
553	616	555	618	557	620	559	622
561	624	563	626	565	628	567	630
569	632	571	634	573	636	575	638
577	640	579	642	581	644	583	646
585	648	587	650	589	652	591	654
593	656	595	658	597	660	599	662
601	664	603	666	605	668	607	670
609	672	611	674	613	676	615	678
617	680	619	682	621	684	623	686
625	688	627	690	629	692	631	694
633	696	635	698	637	700	639	702
641	704	643	706	645	708	647	710
649	712	651	714	653	716	655	718
657	720	659	722	661	724	663	726
665	728	667	730	669	732	671	734
673	736	675	738	677	740	679	742
681	744	683	746	685	748	687	750
689	752	691	754	693	756	695	758
697	760	699	762	701	764	703	766
705	768	707	770	709	772	711	774
713	776	715	778	717	780	719	782
721	784	723	786	725	788	727	790
729	792	731	794	733	796	735	798
737	800	739	802	741	804	743	806
745	808	747	810	749	812	751	814
753	816	755	818	757	820	759	822
761	824	763	826	765	828	767	830
769	832	771	834	773	836	775	838
777	840	779	842	781	844	783	846

Table 49: Shared Pages (Continued)

Shared Pages		Shared Pages		Shared Pages		Shared Pages	
785	848	787	850	789	852	791	854
793	856	795	858	797	860	799	862
801	864	803	866	805	868	807	870
809	872	811	874	813	876	815	878
817	880	819	882	821	884	823	886
825	888	827	890	829	892	831	894
833	896	835	898	837	900	839	902
841	904	843	906	845	908	847	910
849	912	851	914	853	916	855	918
857	920	859	922	861	924	863	926
865	928	867	930	869	932	871	934
873	936	875	938	877	940	879	942
881	944	883	946	885	948	887	950
889	952	891	954	893	956	895	958
897	960	899	962	901	964	903	966
905	968	907	970	909	972	911	974
913	976	915	978	917	980	919	982
921	984	923	986	925	988	927	990
929	992	931	994	933	996	935	998
937	1000	939	1002	941	1004	943	1006
945	1008	947	1010	949	1012	951	1014
953	1016	955	1018	957	1020	959	1022
961	–	963	–	965	–	967	–
969	–	971	–	973	–	975	–
977	–	979	–	981	–	983	–
985	–	987	–	989	–	991	–
993	–	995	–	997	–	999	–
1001	–	1003	–	1005	–	1007	–
1009	–	1011	–	1013	–	1015	–
1017	–	1019	–	1021	–	1023	–

Output Drive Impedance

Because NAND Flash is designed for use in systems that are typically point-to-point connections, an option to control the drive strength of the output buffers is provided. Drive strength should be selected based on the expected loading of the memory bus. The three supported settings for the output drivers for the Asynchronous, NV-DDR, and NV-DDR2 interfaces are: 25 ohms, 35 ohms, and 50 ohms. The two supported settings for the output drivers for the NV-DDR3 interface are: 35 ohms and 50 ohms.

The 35 ohm output drive strength setting is the power-on default value in the Asynchronous, NV-DDR, and NV-DDR2 interfaces. The 35 ohm output drive strength setting is the power-on default value in the NV-DDR3 interface. The host can select a different drive strength setting using the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command.

The output impedance range from minimum to maximum covers process, voltage, and temperature variations. Devices are not guaranteed to be at the nominal line.

Table 50: Output Drive Strength Conditions (V_{CCQ} = 1.7–1.95V)

Range	Process	Voltage	Temperature
Minimum	Slow-Slow	1.7V	T_{OPER} (MAX)
Nominal	Typical-Typical	1.8V	+25°C
Maximum	Fast-Fast	1.95V	T_{OPER} (MIN)

Table 51: Output Drive Strength Impedance Values without ZQ Calibration (V_{CCQ} = 1.7–1.95V)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
25 Ohms	Rpd	V_{CCQ} × 0.2	11.4	25.0	44.0	ohms
		V_{CCQ} × 0.5	15.0	25.0	44.0	ohms
		V_{CCQ} × 0.8	15.0	25.0	61.0	ohms
	Rpu	V_{CCQ} × 0.2	15.0	25.0	61.0	ohms
		V_{CCQ} × 0.5	15.0	25.0	44.0	ohms
		V_{CCQ} × 0.8	11.4	25.0	44.0	ohms
35 Ohms	Rpd	V_{CCQ} × 0.2	16.0	35.0	61.0	ohms
		V_{CCQ} × 0.5	21.0	35.0	61.0	ohms
		V_{CCQ} × 0.8	21.0	35.0	85.3	ohms
	Rpu	V_{CCQ} × 0.2	21.0	35.0	85.3	ohms
		V_{CCQ} × 0.5	21.0	35.0	61.0	ohms
		V_{CCQ} × 0.8	16.0	35.0	61.0	ohms

Table 51: Output Drive Strength Impedance Values without ZQ Calibration (V_{CCQ} = 1.7–1.95V) (Continued)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
50 Ohms	Rpd	V_{CCQ} × 0.2	24.0	50.0	87.0	ohms
		V_{CCQ} × 0.5	30.0	50.0	87.0	ohms
		V_{CCQ} × 0.8	30.0	50.0	122.0	ohms
	Rpu	V_{CCQ} × 0.2	30.0	50.0	122.0	ohms
		V_{CCQ} × 0.5	30.0	50.0	87.0	ohms
		V_{CCQ} × 0.8	24.0	50.0	87.0	ohms

Table 52: Output Drive Strength Impedance Values with ZQ Calibration (V_{CCQ} = 1.7–1.95V)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maxi-mum	Unit	Note
25 Ohms	Rpd	V_{CCQ} × 0.2	11.4	20.0	32.0	ohms	1
		V_{CCQ} × 0.5	16.3	25.0	33.7	ohms	
		V_{CCQ} × 0.8	20.0	31.0	49.0	ohms	
	Rpu	V_{CCQ} × 0.2	20.0	31.0	49.0	ohms	
		V_{CCQ} × 0.5	16.3	25.0	33.7	ohms	
		V_{CCQ} × 0.8	11.4	20.0	32.0	ohms	
35 Ohms	Rpd	V_{CCQ} × 0.2	0.57	1	1.15	R_{ZQ} / 8.5	
		V_{CCQ} × 0.5	0.85	1	1.15	R_{ZQ} / 8.5	
		V_{CCQ} × 0.8	0.85	1	1.47	R_{ZQ} / 8.5	
	Rpu	V_{CCQ} × 0.2	0.85	1	1.47	R_{ZQ} / 8.5	
		V_{CCQ} × 0.5	0.85	1	1.15	R_{ZQ} / 8.5	
		V_{CCQ} × 0.8	0.57	1	1.15	R_{ZQ} / 8.5	
50 Ohms	Rpd	V_{CCQ} × 0.2	0.57	1	1.15	R_{ZQ} / 6	
		V_{CCQ} × 0.5	0.85	1	1.15	R_{ZQ} / 6	
		V_{CCQ} × 0.8	0.85	1	1.47	R_{ZQ} / 6	
	Rpu	V_{CCQ} × 0.2	0.85	1	1.47	R_{ZQ} / 6	
		V_{CCQ} × 0.5	0.85	1	1.15	R_{ZQ} / 6	
		V_{CCQ} × 0.8	0.57	1	1.15	R_{ZQ} / 6	

Notes:
1. The 25 Ohm drive strength does not support ZQ Calibration operations. If ZQ Calibration operations are used when the 25 Ohm drive strength is selected, the defaut NAND drive strength settings are still used.
2. Tolerance limits assume R_{ZQ} of 300 ohms +/- 1% and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage.
3. Refer to Output Driver Sensitivity if either the temperature or the voltage changes after calibration.
4. The minimum values are derated by 6% when the device operates between -40°C and 0°C.

Table 53: Output Drive Strength Conditions (V_{CCQ} = 1.14–1.26V)

Range	Process	Voltage	Temperature
Minimum	Slow-Slow	1.14V	T_{OPER} (MAX)
Nominal	Typical-Typical	1.2V	+25°C
Maximum	Fast-Fast	1.26V	T_{OPER} (MIN)

Table 54: Output Drive Strength Impedance Values without ZQ Calibration (V_{CCQ} = 1.14–1.26V)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
35 Ohms	Rpd	V_{CCQ} × 0.2	16.0	35.0	61.0	Ohms
		V_{CCQ} × 0.5	21.0	35.0	61.0	Ohms
		V_{CCQ} × 0.8	21.0	35.0	85.3	Ohms
	Rpu	V_{CCQ} × 0.2	21.0	35.0	85.3	Ohms
		V_{CCQ} × 0.5	21.0	35.0	61.0	Ohms
		V_{CCQ} × 0.8	16.0	35.0	61.0	Ohms
50 Ohms	Rpd	V_{CCQ} × 0.2	24.0	50.0	87.0	Ohms
		V_{CCQ} × 0.5	30.0	50.0	87.0	Ohms
		V_{CCQ} × 0.8	30.0	50.0	122.0	Ohms
	Rpu	V_{CCQ} × 0.2	30.0	50.0	122.0	Ohms
		V_{CCQ} × 0.5	30.0	50.0	87.0	Ohms
		V_{CCQ} × 0.8	24.0	50.0	87.0	Ohms

Table 55: Output Drive Strength Impedance Values with ZQ Calibration (V_{CCQ} = 1.14–1.26V)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
35 Ohms	Rpd	V_{CCQ} × 0.2	0.57	1	1.15	R_{ZQ}/8.5
		V_{CCQ} × 0.5	0.85	1	1.15	R_{ZQ}/8.5
		V_{CCQ} × 0.8	0.85	1	1.47	R_{ZQ}/8.5
	Rpu	V_{CCQ} × 0.2	0.85	1	1.47	R_{ZQ}/8.5
		V_{CCQ} × 0.5	0.85	1	1.15	R_{ZQ}/8.5
		V_{CCQ} × 0.8	0.57	1	1.15	R_{ZQ}/8.5

Table 55: Output Drive Strength Impedance Values with ZQ Calibration (V_{CCQ} = 1.14–1.26V) (Continued)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
50 Ohms	Rpd	V_{CCQ} × 0.2	0.57	1	1.15	$R_{ZQ}/6$
		V_{CCQ} × 0.5	0.85	1	1.15	$R_{ZQ}/6$
		V_{CCQ} × 0.8	0.85	1	1.47	$R_{ZQ}/6$
	Rpu	V_{CCQ} × 0.2	0.85	1	1.47	$R_{ZQ}/6$
		V_{CCQ} × 0.5	0.85	1	1.15	$R_{ZQ}/6$
		V_{CCQ} × 0.8	0.57	1	1.15	$R_{ZQ}/6$

Notes:
1. Tolerance limits assume R_{ZQ} of 300 ohms +/- 1% and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage.
2. Refer to Output Driver Sensitivity if either the temperature or the voltage changes after calibration.
3. The minimum values are derated by 6% when the device operates between -40°C and 0°C.

If either the temperature or the voltage changes after the ZQ calibration operation, then output drive strength impedance tolerance limits can be expected to widen according to Table 56 (page 195) and Table 57 (page 196).

Table 56: Output Drive Sensitivity with ZQ Calibration

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Maximum	Unit
35 Ohms	Rpd	V_{CCQ} × 0.2	0.57 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.15 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/8.5$
		V_{CCQ} × 0.5	0.85 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.15 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/8.5$
		V_{CCQ} × 0.8	0.85 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.47 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/8.5$
	Rpu	V_{CCQ} × 0.2	0.85 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.47 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/8.5$
		V_{CCQ} × 0.5	0.85 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.15 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/8.5$
		V_{CCQ} × 0.8	0.57 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.15 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/8.5$

Table 56: Output Drive Sensitivity with ZQ Calibration (Continued)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Maximum	Unit
50 Ohms	Rpd	V_{CCQ} × 0.2	0.57 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.15 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/6$
		V_{CCQ} × 0.5	0.85 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.15 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/6$
		V_{CCQ} × 0.8	0.85 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.47 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/6$
	Rpu	V_{CCQ} × 0.2	0.85 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.47 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/6$
		V_{CCQ} × 0.5	0.85 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.15 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/6$
		V_{CCQ} × 0.8	0.57 - $dR_{ON}dT$ x ΔT - $dR_{ON}dV$ x ΔV	1.15 + $dR_{ON}dT$ x ΔT + $dR_{ON}dV$ x ΔV	$R_{ZQ}/6$

Table 57: Output Driver Voltage and Temperature Sensitivity with ZQ Calibration

Chnage	Minimum	Maximum	Unit
$dR_{ON}dT$	0.5	0	% / °C
$dR_{ON}dV$	0.2	0	% / mV

Table 58: Pull-Up and Pull-Down Output Impedance Mismatch without ZQ Calibration for Asynchronous, NV-DDR and NV-DDR2

Drive Strength	Minimum	Maximum	Unit	Notes
25 Ohms	0	4.4	ohms	1, 2
35 Ohms	0	6.2	ohms	1, 2
50 Ohms	0	8.8	ohms	1, 2

Notes:
1. Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.
2. Test conditions: $V_{CCQ} = V_{CCQ}$ (MIN), $V_{OUT} = V_{CCQ} \times 0.5$, T_{OPER}.

Table 59: Pull-Up and Pull-Down Output Impedance Mismatch with ZQ Calibration for NV-DDR2

Drive Strength	Minimum	Maximum	Unit	Notes
25 Ohms	0	3.75	ohms	1, 2, 3
35 Ohms	0	5.25	ohms	2, 3
50 Ohms	0	7.5	ohms	2, 3

Notes:
1. The 25 Ohm drive strength does not support ZQ Calibration operations. If ZQ Calibration operations are used when the 25 Ohm drive strength is selected, the defaut NAND drive strength settings are still used.

2. Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.
3. Test conditions: $V_{CCQ} = V_{CCQ}$ (MIN), $V_{OUT} = V_{CCQ} \times 0.5$, T_{OPER}.

Table 60: Pull-Up and Pull-Down Output Impedance Mismatch without ZQ calibration for NV-DDR3

Drive Strength	Minimum	Maximum	Unit	Notes
35 Ohms	0	6.2	ohms	on page , on page
50 Ohms	0	8.8	ohms	on page , on page

Notes:
1. Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.
2. Test conditions: $V_{CCQ} = V_{CCQ}$ (MIN), $V_{OUT} = V_{CCQ} \times 0.5$, T_{OPER}.

Table 61: Pull-Up and Pull-Down Output Impedance Mismatch with ZQ calibration for NV-DDR3

Drive Strength	Minimum	Maximum	Unit	Notes
35 Ohms	0	5.25	ohms	on page , on page
50 Ohms	0	7.5	ohms	on page , on page

Notes:
1. Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.
2. Test conditions: $V_{CCQ} = V_{CCQ}$ (MIN), $V_{OUT} = V_{CCQ} \times 0.5$, T_{OPER}.

AC Overshoot/Undershoot Specifications

The supported AC overshoot and undershoot area depends on the timing mode selected by the host. NAND devices may have different maximum amplitude requirements for overshoot and undershoot than the host controller. If the host controller has more stringent requirements, termination or other means of reducing overshoot or undershoot may be required beyond the NAND requirements.

Table 62: Aynchronous Overshoot/Undershoot Parameters

Parameter	Timing Mode						Unit
	0	1	2	3	4	5	
Maximum peak amplitude provided for overshoot area	1	1	1	1	1	1	V
Maximum peak amplitude provided for undershoot area	1	1	1	1	1	1	V
Maximum overshoot area above V_{CCQ}	3	3	3	3	3	3	V-ns
Maximum undershoot area below V_{SSQ}	3	3	3	3	3	3	V-ns

Table 63: NV-DDR Overshoot/Undershoot Parameters

Parameter	Timing Mode						Unit
	0	1	2	3	4	5	
Maximum peak amplitude provided for overshoot area	1	1	1	1	1	1	V
Maximum peak amplitude provided for undershoot area	1	1	1	1	1	1	V
Maximum overshoot area above V_{CCQ}	3	3	3	2.25	1.8	1.5	V-ns
Maximum undershoot area below V_{SSQ}	3	3	3	2.25	1.8	1.5	V-ns

Table 64: NV-DDR2 Overshoot/Undershoot Parameters

Parameter	Signals	Timing Mode									Unit
		0	1	2	3	4	5	6	7	8	
Maximum peak amplitude provided for overshoot area	-	1	1	1	1	1	1	1	1	1	V
Maximum peak amplitude provided for undershoot area	-	1	1	1	1	1	1	1	1	1	V
Maximum overshoot area above V_{CCQ}	DQ[7:0], DQS, RE#	3	3	2.25	1.8	1.5	1.1	0.9	0.75	0.56	V-ns
	ALE, CLE, WE#	3	3	3	3	3	3	3	3	3	
Maximum undershoot area below V_{SSQ}	DQ[7:0], DQS, RE#	3	3	2.25	1.8	1.5	1.1	0.9	0.75	0.56	V-ns
	ALE, CLE, WE#	3	3	3	3	3	3	3	3	3	

Table 65: NV-DDR3 Overshoot/Undershoot Parameters

Parameter	Signals	Timing Mode											Unit
		0	1	2	3	4	5	6	7	8	9	10	
Maximum peak amplitude provided for overshoot area	-	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	V
Maximum peak amplitude provided for undershoot area	-	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	V
Maximum overshoot area above V_{CCQ}	DQ[7:0], DQS, RE#	3	3	2.25	1.8	1.5	1.1	0.9	0.75	0.56	0.45	0.38	V-ns
	ALE, CLE, WE#	3	3	3	3	3	3	3	3	3	3	3	
Maximum undershoot area below V_{SSQ}	DQ[7:0], DQS, RE#	3	3	2.25	1.8	1.5	1.1	0.9	0.75	0.56	0.45	0.38	V-ns
	ALE, CLE, WE#	3	3	3	3	3	3	3	3	3	3	3	

Figure 101: Overshoot

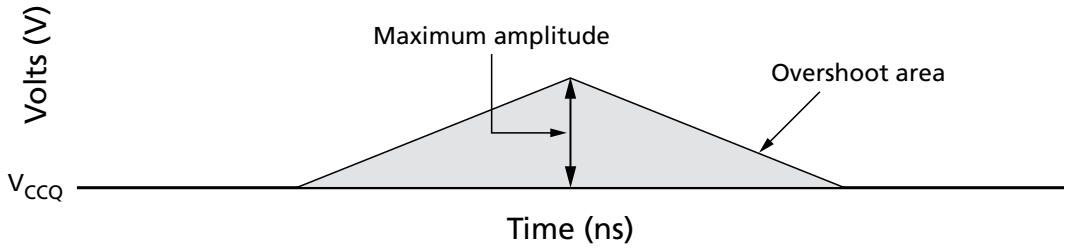
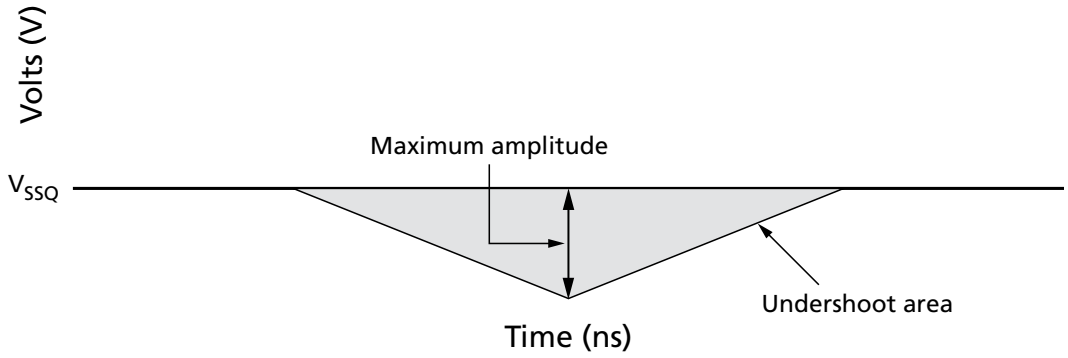


Figure 102: Undershoot



Input Slew Rate

Though all AC timing parameters are tested with a nominal input slew rate of 1 V/ns, it is possible to run the device at a slower slew rate. The input slew rates shown below are sampled, and not 100% tested. When using slew rates slower than the minimum values, timing must be derated by the host.

Table 66: Test Conditions for Input Slew Rate

Parameter	Value
Rising edge for setups	$V_{IL(DC)}$ To $V_{IH(AC)}$ for NV-DDR
	The last crossing of $V_{REFQ(DC)}$ and the first crossing of $V_{IH(AC)}$ min for NV-DDR2 and NV-DDR3
Falling edge for setups	$V_{IH(DC)}$ To $V_{IL(AC)}$ for NV-DDR
	The last crossing of $V_{REFQ(DC)}$ and the first crossing of $V_{IL(AC)}$ max for NV-DDR2 and NV-DDR3
Rising edge for holds	$V_{IL(DC)}$ To $V_{IH(AC)}$ for NV-DDR
	The first crossing of $V_{IL(DC)}$ max and the first crossing of $V_{REFQ(DC)}$ for NV-DDR2 and NV-DDR3
Falling edge for holds	$V_{IH(DC)}$ To $V_{IL(AC)}$ for NV-DDR
	The first crossing of $V_{IH(DC)}$ min and the first crossing of $V_{REFQ(DC)}$ for NV-DDR2 and NV-DDR3
Temperature range	T_{OPER}

The minimum and maximum input slew rate requirements that the device shall comply with below for NV-DDR operations. If the input slew rate falls below the minimum value, then derating shall be applied.

Table 67: NV-DDR Maximum and Minimum Input Slew Rate

Description	Timing Modes 0-5	Unit
Input slew rate (min)	0.5	V/ns
Input slew rate (max)	4.5	V/ns

Table 68: Input Slew Rate derating for NV-DDR (V_{CCQ} = 1.7–1.95V)

Command/ Address and DQ V/ns	CLK/DQS Slew Rate Derating $V_{IH(AC)}/V_{IL(AC)}$= 540mV, $V_{IH(DC)}/V_{IL(DC)}$= 360mV																Unit
	1		0.9		0.8		0.7		0.6		0.5		0.4		0.3		
	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	
1	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	ps
0.9	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	ps
0.8	-	-	0	0	0	0	0	0	-	-	-	-	-	-	-	-	ps

Table 68: Input Slew Rate derating for NV-DDR (V_{CCQ} = 1.7–1.95V) (Continued)

Command/ Address and DQ V/ns	CLK/DQS Slew Rate Derating $V_{IH(AC)}/V_{IL(AC)}$= 540mV, $V_{IH(DC)}/V_{IL(DC)}$= 360mV																Unit
	1		0.9		0.8		0.7		0.6		0.5		0.4		0.3		
	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	
0.7	-	-	-	-	0	0	0	0	0	0	-	-	-	-	-	-	ps
0.6	-	-	-	-	-	-	0	0	0	0	0	0	-	-	-	-	ps
0.5	-	-	-	-	-	-	-	-	0	0	0	0	180	180	-	-	ps
0.4	-	-	-	-	-	-	-	-	-	-	180	180	360	360	660	660	ps
0.3	-	-	-	-	-	-	-	-	-	-	-	-	660	660	920	920	ps

The minimum and maximum input slew rate requirements that the device shall comply with below for NV-DDR2 and NV-DDR3 operations. If the input slew rate falls below the minimum value, then derating shall be applied.

Table 69: NV-DDR2/NV-DDR3 Maximum and Minimum Input Slew Rate

Description	Single Ended	Differential	Unit
	Timing Modes 0-7	Timing Modes 0-7	
Input slew rate (min)	1.0	2.0	V/ns
Input slew rate (max)	4.5	9.0	V/ns

For DQ signals when used for input, the total data setup time (^{t}DS) and data hold time (^{t}DH) required is calculated by adding a derating value to the ^{t}DS and ^{t}DH values indicated for the timing mode. To calculate the total data setup time, ^{t}DS is incremented by the appropriate Δset derating value. To calculate the total data hold time, ^{t}DH is incremented by the appropriate Δhold derating value. Table 70 (page 202) and Table 72 (page 203) provides the derating values when single-ended DQS is used. Table 71 (page 202) and Table 73 (page 203) provides the derating values when differential DQS (DQS_t/DQS_c) is used.

The setup nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REFQ(DC)}$ and the first crossing of $V_{IH(AC)}$ min. The setup nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REFQ(DC)}$ and the first crossing of $V_{IL(AC)}$ max. If the actual signal is always earlier than the nominal slew rate line between the shaded '$V_{REFQ(DC)}$ to AC region', then the derating value uses the nominal slew rate shown in Figure 103 (page 204). If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REFQ(DC)}$ to AC region', then the derating value uses the slew rate of a tangent line to the actual signal from the AC level to the DC level shown in Figure 104 (page 205).

The hold nominal slew rate for a rising signal is defined as the slew rate between the first crossing of $V_{IL(DC)}$ max and the first crossing of $V_{REFQ(DC)}$. The hold nominal slew rate for a falling signal is defined as the slew rate between the first crossing of $V_{IH(DC)}$ min and the first crossing of $V_{REFQ(DC)}$. If the actual signal is always later than the nominal slew rate line between shaded 'DC to $V_{REFQ(DC)}$ region', then the derating value uses the nominal slew rate shown in Figure 105 (page 206). If the actual signal is earlier than the nominal slew rate line anywhere between the shaded 'DC to $V_{REFQ(DC)}$ region', then the derating value uses the slew rate of a tangent line to the actual signal from the DC level to the $V_{REFQ(DC)}$ level shown in Figure 106 (page 207).

If the tangent line is used for derating, the setup and hold values shall be derated from where the tangent line crosses $V_{REFQ(DC)}$, not the actual signal (refer to Figure 104 (page 205) and Figure 106 (page 207)).

For slew rates not explicitly listed in Table 70 (page 202) and Table 71 (page 202), the derating values should be obtained by linear interpolation. These values are typically not subject to production test; the values are verified by design and characterization.

Table 70: Input Slew Rate derating for NV-DDR2 single-ended (V_{CCQ} = 1.7–1.95V)

DQ	Δ DQS Slew Rate Derating $V_{IH(AC)}/V_{IL(AC)}$= 250mV, $V_{IH(DC)}/V_{IL(DC)}$= 125mV																				
	2		1.5		1		0.9		0.8		0.7		0.6		0.5		0.4		0.3		
V/ns	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	Unit
2	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ps
1.5	0	0	0	0	0	0	14	0	-	-	-	-	-	-	-	-	-	-	-	-	ps
1	0	0	0	0	0	0	14	0	31	0	-	-	-	-	-	-	-	-	-	-	ps
0.9	-	-	14	0	14	0	28	0	45	0	67	0	-	-	-	-	-	-	-	-	ps
0.8	-	-	-	-	31	0	45	0	63	0	85	0	115	0	-	-	-	-	-	-	ps
0.7	-	-	-	-	-	-	67	0	85	0	107	0	137	0	179	0	-	-	-	-	ps
0.6	-	-	-	-	-	-	-	-	115	0	137	0	167	0	208	0	271	0	-	-	ps
0.5	-	-	-	-	-	-	-	-	-	-	179	0	208	0	250	0	313	0	418	0	ps
0.4	-	-	-	-	-	-	-	-	-	-	-	-	271	0	313	0	375	0	480	0	ps
0.3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	418	0	480	0	594	0	ps

Table 71: Input Slew Rate derating for NV-DDR2 differential (V_{CCQ} = 1.7–1.95V)

DQ V/ns	Δ DQS_t/DQS_c Slew Rate Derating $V_{IH(AC)}/V_{IL(AC)}$= 250mV, $V_{IH(DC)}/V_{IL(DC)}$= 125mV																Unit
	2		1.8		1.6		1.4		1.2		1		0.8		0.6		
	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	
2	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ps
1.5	0	0	7	0	-	-	-	-	-	-	-	-	-	-	-	-	ps
1	0	0	7	0	16	0	-	-	-	-	-	-	-	-	-	-	ps
0.9	14	0	21	0	30	0	41	0	-	-	-	-	-	-	-	-	ps
0.8	31	0	38	0	47	0	58	0	73	0	-	-	-	-	-	-	ps
0.7	-	-	61	0	69	0	80	0	95	0	116	0	-	-	-	-	ps
0.6	-	-	-	-	99	0	110	0	125	0	146	0	176	0	-	-	ps
0.5	-	-	-	-	-	-	152	0	167	0	188	0	218	0	269	0	ps
0.4	-	-	-	-	-	-	-	-	229	0	250	0	282	0	333	0	ps
0.3	-	-	-	-	-	-	-	-	-	-	355	0	385	0	436	0	ps

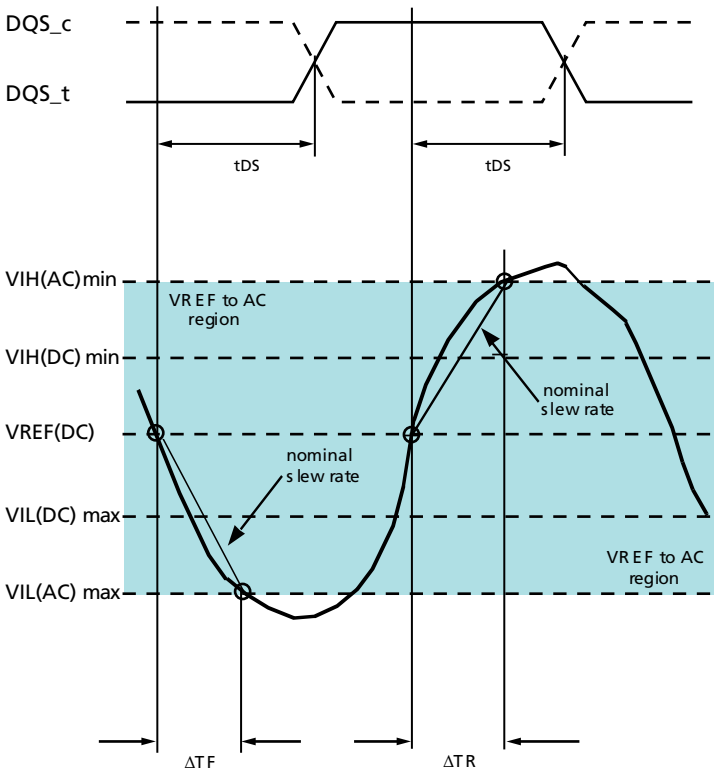
Table 72: Input Slew Rate derating for NV-DDR3 single-ended (V_{CCQ} = 1.14–1.26V)

DQ	Δ DQS Slew Rate Derating $V_{IH(AC)}/V_{IL(AC)}$= 150mV, $V_{IH(DC)}/V_{IL(DC)}$= 100mV																				
	2		1.5		1		0.9		0.8		0.7		0.6		0.5		0.4		0.3		
V/ns	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	Unit
2	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ps
1.5	0	0	0	0	0	0	11	0	-	-	-	-	-	-	-	-	-	-	-	-	ps
1	0	0	0	0	0	0	11	0	25	0	-	-	-	-	-	-	-	-	-	-	ps
0.9	-	-	0	0	11	0	22	0	36	0	54	0	-	-	-	-	-	-	-	-	ps
0.8	-	-	-	-	25	0	39	0	50	0	68	0	92	0	-	-	-	-	-	-	ps
0.7	-	-	-	-	-	-	54	0	68	0	86	0	110	0	143	0	-	-	-	-	ps
0.6	-	-	-	-	-	-	-	-	92	0	110	0	133	0	167	0	217	0	-	-	ps
0.5	-	-	-	-	-	-	-	-	-	-	143	0	167	0	200	0	250	0	333	0	ps
0.4	-	-	-	-	-	-	-	-	-	-	-	-	217	0	250	0	300	0	383	0	ps
0.3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	333	0	383	0	467	0	ps

Table 73: Input Slew Rate derating for NV-DDR3 differential (V_{CCQ} = 1.14–1.26V)

	Δ DQS_t/DQS_c Slew Rate Derating $V_{IH(AC)}/V_{IL(AC)}$= 150mV, $V_{IH(DC)}/V_{IL(DC)}$= 100mV																
	2		1.8		1.6		1.4		1.2		1		0.8		0.6		
DQ V/ns	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	set	hold	Unit
2	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ps
1.5	0	0	6	0	-	-	-	-	-	-	-	-	-	-	-	-	ps
1	0	0	6	0	13	0	-	-	-	-	-	-	-	-	-	-	ps
0.9	11	0	17	0	24	0	33	0	-	-	-	-	-	-	-	-	ps
0.8	25	0	31	0	38	0	46	0	58	0	-	-	-	-	-	-	ps
0.7	-	-	48	0	55	0	64	0	76	0	93	0	-	-	-	-	ps
0.6	-	-	-	-	79	0	88	0	100	0	117	0	142	0	-	-	ps
0.5	-	-	-	-	-	-	121	0	133	0	150	0	175	0	217	0	ps
0.4	-	-	-	-	-	-	-	-	183	0	200	0	225	0	267	0	ps
0.3	-	-	-	-	-	-	-	-	-	-	282	0	308	0	350	0	ps

Figure 103: Nominal Slew Rate for Data Setup Time (^{t}DS), NV-DDR2/NV-DDR3 only



$$\text{Setup Slew Rate Falling Signal} = \frac{\text{VREF(DC)} - \text{VIL(AC) max}}{\Delta TF} \qquad \text{Setup Slew Rate Rising Signal} = \frac{\text{VIL(AC) min} - \text{VREF(DC)}}{\Delta TR}$$

Illustration of nominal slew rate for setup time ^{t}DS

Figure 104: Tangent Line for Data Setup Time (^{t}DS), NV-DDR2/NV-DDR3 only

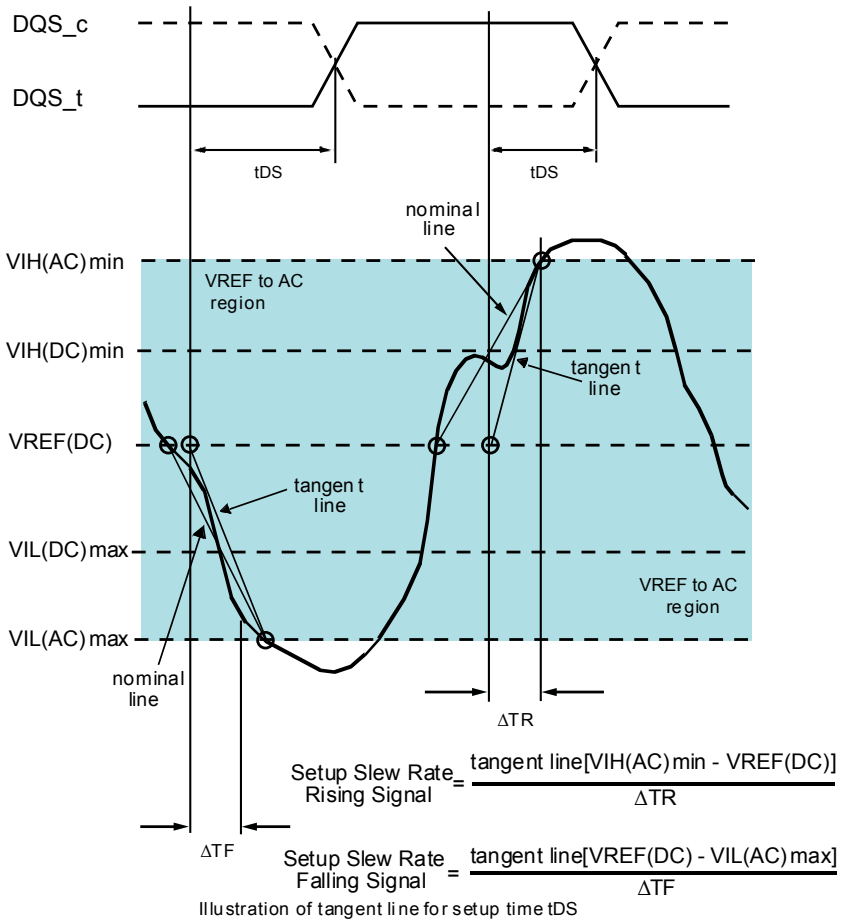


Illustration of tangent line for setup time tDS

Figure 105: Nominal Slew Rate for Data Hold Time (^{t}DH), NV-DDR2/NV-DDR3 only

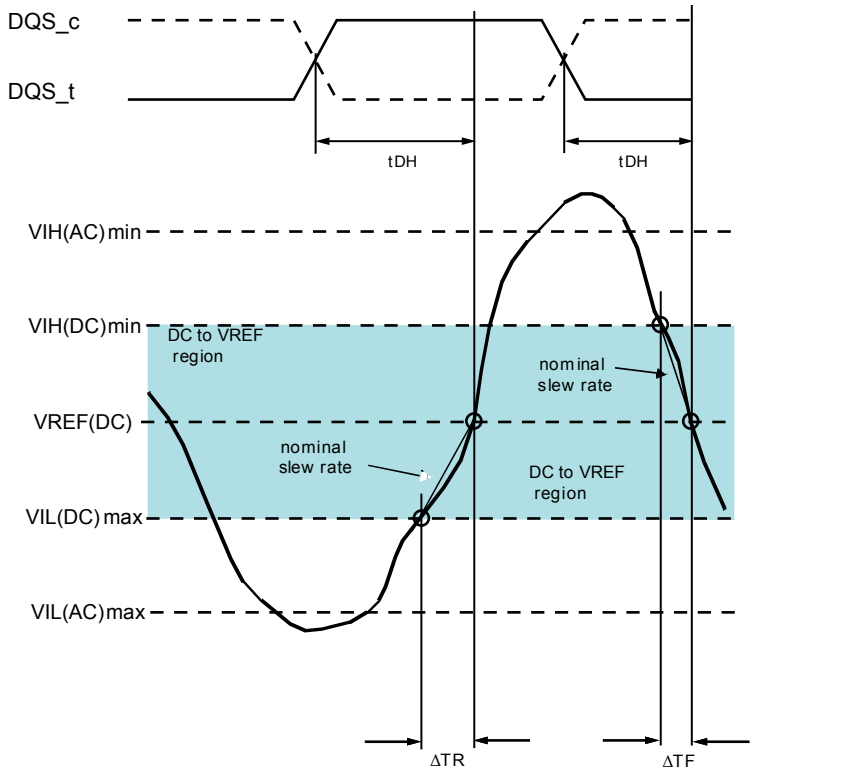
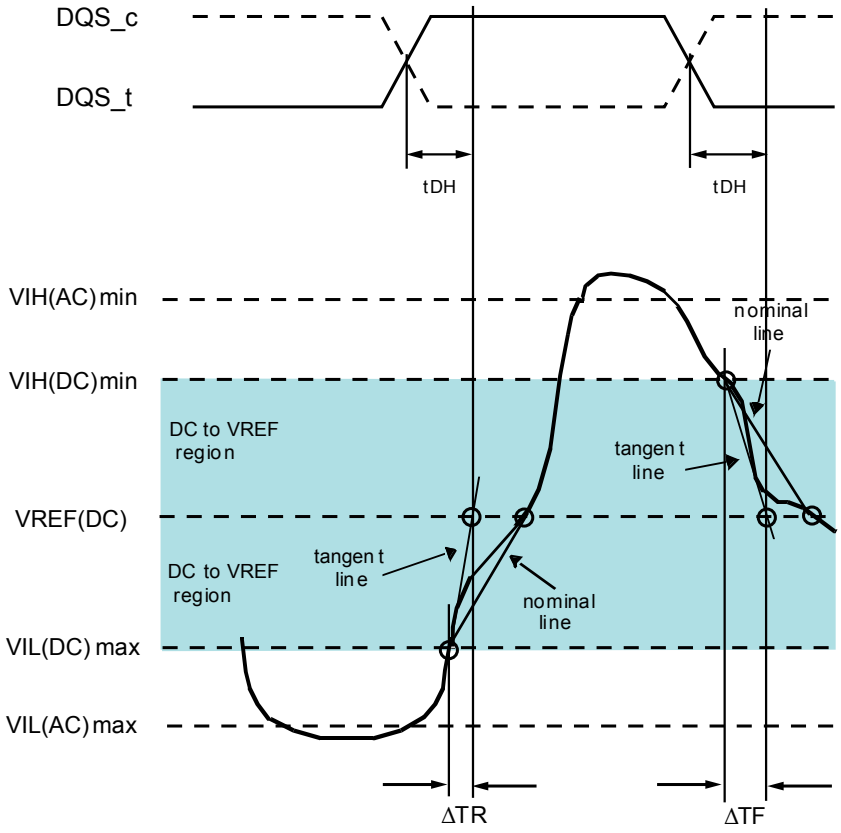


Illustration of nominal slew rate for hold time tDH

Figure 106: Tangent Line for Data Hold Time (^{t}DH), NV-DDR2/NV-DDR3 only



$$\text{Hold Slew Rate}_{\text{Rising Signal}} = \frac{\text{tangent line [VREF(DC) - VIL(DC)max]}}{\Delta TR}$$

$$\text{Hold Slew Rate}_{\text{Falling Signal}} = \frac{\text{tangent line [VIH(DC)min - VREF(DC)]}}{\Delta TF}$$

Illustration of tangent line for for hold time tDH

Output Slew Rate

The output slew rate is tested using the following setup with only one die per DQ channel.

Table 74: Test Conditions for Output Slew Rate

Parameter	Asynchronous/NV-DDR Interface[1]	NV-DDR2/NV-DDR3 Single-Ended[1,2]	NV-DDR2/NV-DDR3 Differential[1,2]
$V_{OL(DC)}$	0.4 × V_{CCQ}	-	-
$V_{OH(DC)}$	0.6 × V_{CCQ}	-	-
$V_{OL(AC)}$[3]	0.3 × V_{CCQ}	V_{TT} - (V_{CCQ} * 0.10)	-
$V_{OH(AC)}$[3]	0.7 × V_{CCQ}	V_{TT} + (V_{CCQ} * 0.10)	-
$V_{OLdiff(AC)}$	-	-	-0.2 * V_{CCQ}
$V_{OHdiff(AC)}$	-	-	0.2 * V_{CCQ}
Rising edge (^{t}RISE)	$V_{OL(DC)}$ to $V_{OH(AC)}$	$V_{OL(AC)}$ to $V_{OH(AC)}$	-
Falling edge (^{t}FALL)	$V_{OH(DC)}$ to $V_{OL(AC)}$	$V_{OH(AC)}$ to $V_{OL(AC)}$	-
Differential rising edge (^{t}RISEdiff)	-	-	$V_{OLdiff(AC)}$ to $V_{OHdiff(AC)}$
Differential falling edge (^{t}FALLdiff)	-	-	$V_{OHdiff(AC)}$ to $V_{OLdiff(AC)}$
Output slew rate rising edge	[$V_{OH(AC)}$ - $V_{OL(DC)}$] / ^{t}RISE	[$V_{OH(AC)}$ - $V_{OL(AC)}$] / ^{t}RISE	[$V_{OHdiff(AC)}$ - $V_{OLdiff(AC)}$] / ^{t}RISEdiff
Output slew rate falling edge	[$V_{OH(DC)}$ - $V_{OL(AC)}$] / ^{t}FALL	[$V_{OH(AC)}$ - $V_{OL(AC)}$] / ^{t}FALL	[$V_{OHdiff(AC)}$ - $V_{OLdiff(AC)}$] / ^{t}FALLdiff
Output reference load on page			5pf to V_{SS}
Temperature range	T_{OPER}	T_{OPER}	T_{OPER}

Notes:
1. 1.8V V_{CCQ} is required for Asynchronous, NV-DDR, and NV-DDR2 operations.
2. 1.2V V_{CCQ} is required for NV-DDR3 operations.
3. V_{TT} is 0.5 x V_{CCQ}.

Table 75: Output Slew Rate for Single-Ended Asynchronous, NV-DDR, or NV-DDR2 (V_{CCQ} = 1.7–1.95V) without ZQ Calibration

Output Drive Strength	Min	Max	Unit
25 Ohms	0.85	5	V/ns
35 Ohms	0.75	4	V/ns
50 Ohms	0.6	4	V/ns

Table 76: Output Slew Rate for Differential NV-DDR2 (V_{CCQ} = 1.7-1.95) without ZQ Calibration

Output Drive Strength	Min	Max	Unit
25 Ohms	1.7	10.0	V/ns
35 Ohms	1.5	8.0	V/ns

Table 76: Output Slew Rate for Differential NV-DDR2 (V_{CCQ} = 1.7-1.95) without ZQ Calibration (Continued)

Output Drive Strength	Min	Max	Unit
50 Ohms	1.2	8.0	V/ns

Table 77: Output Slew Rate for Differential NV-DDR2 (V_{CCQ} = 1.7-1.95) with ZQ Calibration

Output Drive Strength	Min	Max	Unit
25 Ohms	2.4	10.0	V/ns
35 Ohms	2.16	8.0	V/ns
50 Ohms	1.8	7.0	V/ns

Table 78: Output Slew Rate Matching Ratio for NV-DDR2/NV-DDR3 without ZQ Calibration

Drive Strength	Minimum	Maximum
Output Slew Rate matching ratio (pull-up to pull-down)	0.7	1.4

Notes:
1. The output slew rate mismatch is determined by the ratio of fast slew rate and slow slew rate. If the rising edge is faster than the falling edge, then divide the rising slew rate by the falling slew rate. If the falling edge is faster than the rising edge, then divide the falling slew rate by the rising slew rate.
2. The output slew rate mismatch is verified by design and characterization; it may not be subject to production testing.

Table 79: Output Slew Rate for Single-Ended NV-DDR3 (V_{CCQ} = 1.14–1.26V) with ZQ Calibration

Output Drive Strength	Min	Max	Unit
35 Ohms	0.72	4	V/ns
50 Ohms	0.6	3.5	V/ns

Table 80: Output Slew Rate for Differential NV-DDR3 (V_{CCQ} = 1.14-1.26) with ZQ Calibration

Output Drive Strength	Min	Max	Unit
35 Ohms	1.44	8.0	V/ns
50 Ohms	1.2	7.0	V/ns

Table 81: Output Slew Rate Matching Ratio for NV-DDR2/NV-DDR3 with ZQ Calibration

Drive Strength	Minimum	Maximum
Output Slew Rate matching ratio (pull-up to pull-down)	0.7	1.3

Notes:
1. The output slew rate mismatch is determined by the ratio of fast slew rate and slow slew rate. If the rising edge is faster than the falling edge, then divide the rising slew rate by the falling slew rate. If the falling edge is faster than the rising edge, then divide the falling slew rate by the rising slew rate.
2. The output slew rate mismatch is verified by design and characterization; it may not be subject to production testing.

Slew rates are measured under normal SSO conditions, with half of the DQ signals per data byte driving high and half of the DQ signals per data byte driving low. The output slew rate is measured per individual DQ signal.

Power Cycle and Ramp Requirements

Upon power-down the NAND device requires a maximum voltage and minimum time that the host must hold V_{CC} and V_{CCQ} below the voltage prior to power-on.

Table 82: Power Cycle Requirements

Parameter	Value	Unit
Maximum V_{CC}/V_{CCQ}	100	mV
Minimum time below maximum voltage	100	ns

The NAND device will successfully power-up over the range of V_{CC}/V_{CCQ} slew rates for the following range:

Power supply voltage = 3.3v/35ms : 0.094mV/µs to 100mV/µs

Power supply voltage = 1.8v/25ms: 0.072mV/µs to 100mV/µs

Power supply voltage = 1.2v/20ms: 0.060mV/µs to 100mV/µs

Electrical Specifications

Stresses greater than those listed can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods can affect reliability.

Table 83: Absolute Maximum DC Ratings by Device

Parameter	Symbol	Min[1]	Max[1]	Unit
Voltage input	V_{IN}	-0.45	2.4	V
V_{CC} supply voltage	V_{CC}	-0.6	4.6	V
V_{CCQ} supply voltage	V_{CCQ}	-0.45	2.4	V
V_{PP} supply voltage	V_{PP}	-0.6	16	V
V_{REFQ} supply voltage	V_{REFQ}	-0.45	2.4	V
Storage temperature	T_{STG}	-65	+150	°C

Note: 1. Voltage on any pin relative to V_{SS}.

Table 84: Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Unit
Operating temperature[1]	Commercial	T_{OPER}	0	–	+70	°C
	Industrial		-40	–	+85	
V_{CC} supply voltage [2]		V_{CC}	2.7	3.3	3.6	V
V_{CCQ} supply voltage (1.8V) [2]		V_{CCQ}	1.7	1.8	1.95	V
V_{CCQ} supply voltage (1.2V) [2]			1.14	1.2	1.26	
V_{PP} supply voltage		V_{PP}	10.8	12.0	13.2	V
V_{REFQ} supply voltage		V_{REFQ}	0.49 x V_{CCQ}	0.5 x V_{CCQ}	0.51 x V_{CCQ}	V
V_{SS} ground voltage		V_{SS}	0	0	0	V

Notes:
1. Operating temperature (T_{OPER}) is the case surface temperature on the center/top of the NAND
2. AC Noise on the supply voltages shall not exceed +/- 3% (10kHz to 800MHz). AC and DC noise together shall stay within the Min-Max range specified in this table.

Table 85: Valid Blocks per LUN

Parameter	Symbol	Min	Max	Unit	Notes
Valid block number	NVB	2044	2192	Blocks	1

Note: 1. Invalid blocks are blocks that contain one or more bad bits beyond ECC. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below NVB during the endurance life of the device. Do not erase or program blocks marked invalid from the factory.

Package Electrical Specification and Pad Capacitance

Z_{IO} applies to DQ[7:0]. DQS_t, DQS_c, RE_t and RE_c. $Td_{IO\ RE}$ applies to RE_t and RE_c. Td_{IO} and $Td_{IO\ Mismatch}$ apply to DQ[7:0], DQS_t and DQS_c. Mismatch and Delta values are required to be met across same data bus on given package (i.e. package channel), but not required across all channels on a given package. All other pins only need meet requirements in on page .

Table 86: Package Electrical Specifications

Description	Symbol	<= 400 MT/s			533 MT/s			667 MT/s			Unit	Notes
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input/Output Z_{PKG}	Z_{IO}	40	–	90	40	–	90	40	–	90	Ohms	1
Delta Z_{PKG} for DQS_t and DQS_c	$DZ_{IO\ DQS}$	–	–	10	–	–	10	–	–	10	Ohms	7
Input/Output Package delay	Td_{IO}	–	–	160	–	–	160	–	–	145	ps	1
RE# Package delay	$Td_{IO\ RE}$	–	–	160	–	–	160	–	–	160	ps	
Input/Output Package delay mismatch	$Td_{IO\ Mismatch}$	–	–	50	–	–	40	–	–	40	ps	5
Delta package delay for DQS_t and DQS_c	$DZd_{IO\ DQS}$	–	–	10	–	–	10	–	–	10	ps	
Delta Z_{PKG} for RE_t and RE_c	$DZ_{IO\ RE}$	–	–	10	–	–	10	–	–	10	Ohms	
Delta package delay for RE_t and RE_c	DC_{IO}	–	–	10	–	–	10	–	–	10	ps	

Notes:
1. Z_{IO} and Td_{IO} apply to DQ[7:0]. DQS_t, DQS_c, RE_t and RE_c. All other pins only need meet ONFI 3.0 requirements.
2. Test conditions: T_A = 25°C, f = 100 MHz, V_{IN} = 0V.
3. Verified in device characterization; not 100% tested. The package parasitic (L & C) are validated using package only samples. The capacitance is measured with V_{CC}, V_{CCQ}, V_{SS}, V_{SSQ} shorted with all other signal pins floating. The inductance is measured with V_{CC}, V_{CCQ}, V_{SS}, and V_{SSQ} shorted and all other signal pins shorted at the die side (not pin).
4. Package only impedance (Z_{PKG}) is calculated based on the L_{PKG} and C_{PKG} total for a given pin where: Z_{PKG} (total per pin) = SQRT(L_{PKG}/C_{PKG}).
5. Mismatch for Td_{IO} ($Td_{IO\ Mismatch}$) is calculated based on L_{PKG} and C_{PKG} total for a given pin where: Td_{PKG}(total per pin) = SQRT(L_{PKG} * C_{PKG}).
6. Package only delay (T_{PKG}) is calculated based on L_{PKG} and C_{PKG} total for a given pin where: Td_{PKG}(total per pin) = SQRT(L_{PKG}*C_{PKG}).
7. Delta for DQS is Absolute value of Z_{IO}(DQS_t - Z_{IO}(DQS_c)) for impedance (Z) or absolute value of Td_{IO}(DQS_t) - Td_{IO}(DQS_c) for delay (Td).
8. Delta for RE is Absolute value of Z_{IO}(RE_t - Z_{IO}(RE_c)) for impedance (Z) or absolute value of Td_{IO}(RE_t) - Td_{IO}(RE_c) for delay (Td).

Table 87: LUN Pad Specifications

Description	Symbol	<= 400 MT/s			533 MT/s			667 MT/s			Unit	Notes
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input/Output Pad capacitance	C_Pad_{IO}	–	–	1.6	–	–	1.6	–	–	1.6	pF	1
ZQ Pad capacitance	C_Pad_{ZQ}	–	–	1.84	–	–	1.84	–	–	1.84	pF	1
Delta Input/Output Pad capacitance for DQS_t and DQS_c	$D\_C\_Pad_{IO\ DQS}$	0	–	0.2	0	–	0.2	0	–	0.2	pF	4
Delta Input/Output Pad capacitance for RE_t and RE_c	$D\_C\_Pad_{IO\ RE}$	0	–	0.2	0	–	0.2	0	–	0.2	pF	5

Notes:
1. LUN Pad capacitances apply to DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c. All other LUN pads only need to meet ONFI legacy capacitance requirements.
2. Verified in device characterization; not 100% tested. These parameters are not subject to a production test. They are verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with V_{CC}, V_{CCQ}, V_{SS}, and V_{SSQ} applied and all other pins floating (except the pin under test). V_{CCQ} = 1.2V, VBIAS = V_{CCQ}/2 and on-die termination off.
3. These parameters apply to monolithic LUN, obtained by de-embedding the package L & C parasitics.
4. Delta for DQS is Absolute value of C_PAD_{IO}(DQS_t) - C_PAD_{IO}(DQS_c).
5. Delta for RE is Absolute value of C_PAD_{IO}(RE_t) - C_PAD_{IO}(RE_c).

Table 88: Test Conditions

Parameter	Asynchronous and NV-DDR	NV-DDR2/NV-DDR3 single-ended	NV-DDR2/NV-DDR3 differential	Notes
Rising input transition	$V_{IL(DC)}$ to $V_{IH(AC)}$	$V_{IL(DC)}$ to $V_{IH(AC)}$	$V_{ILdiff(DC)}$ max to $V_{IH-diff(AC)}$min	1
Falling input transition	$V_{IH(DC)}$ to $V_{IL(AC)}$	$V_{IH(DC)}$ to $V_{IL(AC)}$	$V_{IHdiff(DC)}$ max to $V_{IL-diff(AC)}$max	1
Input rise and fall slew rates	1 V/ns	1 V/ns	2 V/ns	–
Input timing levels	V_{CCQ}/2	V_{REFQ}	cross-point	–
Output timing levels	V_{CCQ}/2	V_{TT}	cross-point	4
Output load: Nominal output drive strength	5pF to V_{SS}	5pF to V_{SS}	5pF to V_{SS}	2, 3

Notes:
1. The receiver will effectively switch as a result of the signal crossing the AC input level; it will remain in that status as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.
2. Transmission line delay is assumed to be very small.
3. This test setup applies to all package configurations.
4. V_{TT} is 0.5 x V_{CCQ}.

Electrical Specifications – DC Characteristics and Operating Conditions (Asynchronous)

Table 89: DC Characteristics and Operating Conditions (Asynchronous Interface) 1.8V V_{CCQ}

Parameter	Conditions	Symbol	Min[1]	Single-plane Typ[1]	Two-plane Typ[1]	Four-plane Typ[1]	Max[1]	Unit
Array read current (active)	V_{PP} is supplied and not enabled	I_{CC1_A}	–	45	51	57	75	mA
	V_{PP} is supplied and enabled	I_{CC1_A}	–	41	46	51	75	
	–	I_{CCQ1_A}	–	1.5			5	
Array program current (active)	V_{PP} is supplied and not enabled	I_{CC2_A}	–	47	56	60	75	mA
	V_{PP} is supplied and enabled	I_{CC2_A}	–	40	48	51	75	
	–	I_{CCQ2_A}	–	2			8	
Erase current (active)	V_{PP} is supplied and not enabled	I_{CC3_A}	–	42	49	55	75	mA
	V_{PP} is supplied and enabled	I_{CC3_A}	–	37	44	49	75	
	–	I_{CCQ3_A}	–	1.5			5	
I/O burst read current	$^{t}RC = {}^{t}RC$ (MIN); I_{OUT}= 0mA	I_{CC4R_A}	–	8			10	mA
		I_{CCQ4R_A}	–	6			10	
I/O burst write current	$^{t}WC = {}^{t}WC$ (MIN)	I_{CC4w_A}	–	10			13	mA
		I_{CCQ4w_A}	–	6			10	
Bus idle current	–	I_{CC5_A}	–	5			7	mA
		I_{CCQ5_A}	–	1			7	mA
Current during first RESET command after power-on	–	I_{CC6}	–	–			10	mA
V_{PP} current (active)	V_{PP} is supplied and enabled during I_{CC1_A}	I_{PPA1}	–	1			5	mA
	V_{PP} is supplied and enabled during during I_{CC2_A}	I_{PPA2}	–	1			5	mA
	V_{PP} is supplied and enabled during during I_{CC3_A}	I_{PPA3}	–	1			5	mA
V_{PP} current (idle)	V_{PP} is supplied and not enabled	I_{PPI}	–	–			10	µA
Power-up peak current (V_{CC})	–	$I_{CC\_Peak\_Up}$	–	–			20	mA
Power-down peak current (V_{CC})	–	$I_{CC\_Peak\_Down}$	–	–			20	mA

Table 89: DC Characteristics and Operating Conditions (Asynchronous Interface) 1.8V V_{CCQ} (Continued)

Parameter	Conditions	Symbol	Min[1]	Single-plane Typ[1]	Two-plane Typ[1]	Four-plane Typ[1]	Max[1]	Unit
Power-up peak current (V_{CCQ})	–	$I_{CCQ\_Peak\_Up}$	–	–			10	mA
Power-down peak current (V_{CCQ})	–	$I_{CCQ\_Peak\_Down}$	–	–			15	mA
Standby current - V_{CC}	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CCQ}	I_{SB}	–	15			75	µA
Standby current - V_{CCQ}	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CCQ}	I_{SBQ}	–	1			50	µA
Staggered power-up current	$^{t}RISE$ = 1ms; C_{LINE} = 0.1uF	I_{ST}	–	–			10	mA

Notes:
1. All values are per die (LUN) unless otherwise specified.
2. During I_{SBQ} testing, DQS_t/DQS_c, RE_t/RE_c, and DQ[7:0] are floating.

Electrical Specifications – DC Characteristics and Operating Conditions (NV-DDR, NV-DDR2, NV-DDR3)

Table 90: DC Characteristics and Operating Conditions (NV-DDR, NV-DDR2 Interface) 1.8V V_{CCQ}

Parameter	Conditions		Symbol	Min[1]	Single-plane Typ[1]	Two-plane Typ[1]	Four-plane Typ[1]	Max[1]	Unit
Array read current (active)	CE# = V_{IL}; ^{t}CK = ^{t}CK (MIN) NV-DDR	V_{PP} is supplied and not enabled	I_{CC1_S}	–	45	51	57	75	mA
		V_{PP} is supplied and enabled	I_{CC1_S}	–	41	46	51	75	
		–	I_{CCQ1_S}	–	1.5			5	
Array program current (active)	CE# = V_{IL}; ^{t}CK = ^{t}CK (MIN) NV-DDR	V_{PP} is supplied and not enabled	I_{CC2_S}	–	47	56	60	75	mA
		V_{PP} is supplied and enabled	I_{CC2_S}	–	40	48	51	75	
		–	I_{CCQ2_S}	–	2			8	
Erase current (active)	^{t}CK = ^{t}CK (MIN) NV-DDR	V_{PP} is supplied and not enabled	I_{CC3_S}	–	42	49	55	75	mA
		V_{PP} is supplied and enabled	I_{CC3_S}	–	37	44	49	75	
		–	I_{CCQ3_S}	–	1.5			5	

Table 90: DC Characteristics and Operating Conditions (NV-DDR, NV-DDR2 Interface) 1.8V V_{CCQ} (Continued)

Parameter	Conditions	Symbol	Min[1]	Single-plane Typ[1]	Two-plane Typ[1]	Four-plane Typ[1]	Max[1]	Unit
I/O burst read current	$^{t}CK = {}^{t}CK$ (MIN) NV-DDR; $^{t}RC = {}^{t}RC$ (MIN) NV-DDR2; I_{OUT}= 0mA	I_{CC4R_S}	–		13[3]		17[3]	mA
					20[4]		26[4]	
					28[5]		37[5]	
		I_{CCQ4R_S}	–		28[3]		37[3]	mA
					55[4]		72[4]	
					75[5]		98[5]	
I/O burst write current	$^{t}CK = {}^{t}CK$ (MIN) NV-DDR; $^{t}DSC = {}^{t}DSC$ (MIN) NV-DDR2	I_{CC4W_S}	–		15[3]		20[3]	mA
					20[4]		26[4]	
					25[5]		33[5]	
		I_{CCQ4W_S}	–		13[3]		17[3]	mA
					19[4]		25[4]	
					25[5]		33[5]	
Bus idle current	$^{t}CK = {}^{t}CK$ (MIN) NV-DDR	I_{CC5_S}	–		5		10	mA
	NV-DDR2	I_{CC5_S}	–		5		7	mA
	–	I_{CCQ5_S}	–		5		7	mA
Power-up peak current (V_{CC})	–	$I_{CC\_Peak\_Up}$	–		–		20	mA
Power-up peak current (V_{CCQ})	–	$I_{CCQ\_Peak\_Up}$	–		–		10	mA
Power-down peak current (V_{CC})	–	$I_{CC\_Peak\_Down}$	–		–		20	mA
Power-down peak current (V_{CCQ})	–	$I_{CCQ\_Peak\_Down}$	–		–		15	mA
V_{PP} current (active)	V_{PP} is supplied and enabled during I_{CC1_S}	I_{PPA1}	–		1		5	mA
	V_{PP} is supplied and enabled during I_{CC2_S}	I_{PPA2}	–		1		5	mA
	V_{PP} is supplied and enabled during I_{CC3_S}	I_{PPA3}	–		1		5	mA
V_{PP} current (idle)	V_{PP} is supplied and not enabled	I_{PPI}	–		–		10	µA
Standby current - V_{CC}	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CCQ}	I_{SB}	–		15		75	µA
Standby Current - V_{CCQ}	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CCQ}	I_{SBQ}	–		20		50	µA

Notes:
1. All values are per die (LUN) unless otherwise specified.
2. During I_{SBQ} testing, DQS_t/DQS_c, RE_t/RE_c, and DQ[7:0] are floating.
3. For speeds up to 200MT/s.
4. For speeds greater than 200MT/s up to 400MT/s.

5. For speeds greater than 400MT/s.

Table 91: DC Characteristics and Operating Conditions (NV-DDR3 Interface) 1.2V V_{CCQ}

Parameter	Conditions		Symbol	Min[1]	Single-plane Typ[1]	Two-plane Typ[1]	Four-plane Typ[1]	Max[1]	Unit
Array read current (active)	CE# = V_{IL}	V_{PP} is supplied and not enabled	I_{CC1_S}	–	45	51	57	75	mA
		V_{PP} is supplied and enabled	I_{CC1_S}	–	41	46	51	75	
		–	I_{CCQ1_S}	–	1.5			5	
Array program current (active)	CE# = V_{IL}	V_{PP} is supplied and not enabled	I_{CC2_S}	–	47	56	60	75	mA
		V_{PP} is supplied and enabled	I_{CC2_S}	–	40	48	51	75	
		–	I_{CCQ2_S}	–	2			8	
Erase current (active)	–	V_{PP} is supplied and not enabled	I_{CC3_S}	–	44	52	58	75	mA
		V_{PP} is supplied and enabled	I_{CC3_S}	–	39	47	52	75	
		–	I_{CCQ3_S}	–	1.5			5	
I/O burst read current	$^{t}RC = {}^{t}RC$ (MIN); I_{OUT}= 0mA		I_{CC4R_S}	–	9[3]			12[3]	mA
					20[4]			26[4]	
					28[5]			37[5]	
			I_{CCQ4R_S}	–	19[3]			25[3]	mA
					38[4]			50[4]	
					68[5]			88[5]	
I/O burst write current	$^{t}DSC = {}^{t}DSC$ (MIN)		I_{CC4W_S}	–	11[3]			14[3]	mA
					19[4]			25[4]	
					25[5]			33[5]	
			I_{CCQ4W_S}	–	12[3]			16[3]	mA
					18[4]			24[4]	
					34[5]			42[5]	
Bus idle current	–		I_{CC5_S}	–	5			10	mA
			I_{CCQ5_S}	–	5			10	mA
Power-up peak current (V_{CC})	–		$I_{CC\_Peak\_Up}$	–	–			20	mA
Power-down peak current (V_{CC})	–		$I_{CC\_Peak\_Down}$	–	–			20	mA
Power-up peak current (V_{CCQ})	–		$I_{CCQ\_Peak\_Up}$	–	–			10	mA

Table 91: DC Characteristics and Operating Conditions (NV-DDR3 Interface) 1.2V V_{CCQ} (Continued)

Parameter	Conditions	Symbol	Min[1]	Single-plane Typ[1]	Two-plane Typ[1]	Four-plane Typ[1]	Max[1]	Unit
Power-down peak current (V_{CCQ})	–	$I_{CCQ\_Peak\_Down}$	–		–		15	mA
V_{PP} current (active)	V_{PP} is supplied and enabled during I_{CC1_S}	I_{PPA1}	–		1		5	mA
	V_{PP} is supplied and enabled during I_{CC2_S}	I_{PPA2}	–		1		5	mA
	V_{PP} is supplied and enabled during I_{CC3_S}	I_{PPA3}	–		1		5	mA
V_{PP} current (idle)	V_{PP} is supplied and not enabled	I_{PPI}	–		–		10	µA
Standby current - V_{CC}	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CCQ}	I_{SB}	–		10		70	µA
Standby Current - V_{CCQ}	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CCQ}	I_{SBQ}	–		10		50	µA

Notes:
1. All values are per die (LUN) unless otherwise specified.
2. During I_{SBQ} testing, DQS_t/DQS_c, RE_t/RE_c, and DQ[7:0] are floating.
3. For speeds up to 200MT/s.
4. For speeds greater than 200MT/s up to 400MT/s.
5. For speeds greater than 400MT/s up to 667MT/s.

Electrical Specifications – DC Characteristics and Operating Conditions (V_{CCQ})

Table 92: NV-DDR3 DC Characteristics and Operating Conditions for Single-Ended signals (1.2V V_{CCQ})

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
AC input high voltage	DQ[7:0], DQS, ALE, CLE, WE#, RE#	$V_{IH(AC)}$	V_{REFQ} + 0.150	–	–	V	4
AC input low voltage		$V_{IL(AC)}$	–	–	V_{REFQ} - 0.150	V	4
AC input high voltage	CE#, WP#	$V_{IH(AC)}$	0.8 × V_{CCQ}	–	V_{CCQ} + 0.3	V	4
AC input low voltage		$V_{IL(AC)}$	–0.3	–	0.2 × V_{CCQ}	V	4
DC input high voltage	DQ[7:0], DQS, ALE, CLE, WE#, RE#	$V_{IH(DC)}$	V_{REFQ} + 0.100	–	V_{CCQ}	V	on page
DC input low voltage		$V_{IL(DC)}$	V_{SSQ}	–	V_{REFQ} - 0.100	V	on page
DC input high voltage	CE#, WP#	$V_{IH(DC)}$	0.7 × V_{CCQ}	–	V_{CCQ} + 0.3	V	
DC input low voltage		$V_{IL(DC)}$	-0.3	–	0.3 × V_{CCQ}	V	

Table 92: NV-DDR3 DC Characteristics and Operating Conditions for Single-Ended signals (1.2V V_{CCQ}) (Continued)

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
Input leakage current	Any input V_{IN} = 0V to V_{CCQ}	I_{LI}	–	–	±10	µA	on page
Output leakage current	DQ are disabled; V_{OUT} = V_{CCQ}	I_{LO_pd}	–	0.3	1	µA	5
	DQ are disabled; V_{OUT} = 0V; ODT disabled	I_{LO_pu}	–	0.9	5	µA	
Output low current (R/B#)	V_{OL} = 0.2V	I_{OL} (R/B#)	3	4	–	mA	on page
V_{REFQ} leakage current	V_{REFQ}= V_{CCQ}/2 (all other pins not under test = 0V)	I_{VREFQ}	–	–	±5	µA	

Notes:
1. All leakage currents are per die (LUN). For example, two die (LUNs) have a maximum leakage current of ±20µA and four die (LUNs) have a maximum leakage current of ±40µA.
2. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [$V_{IH(DC)}$ Max, $V_{IL(DC)}$ Min] for single-ended signals as well as the limitations for overshoot and undershoot.
3. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full strength. See Table 29 (page 117) for additional details.
4. See AC Overshoot/Undershoot Specifications (page 198) AC Overshoot and Undershoot requirements.
5. Absolute leakage value per I/O per NAND die (DQ[7:0], DQS_t, DQS_c, RE_t, RE_c).

Table 93: NV-DDR3 DC Characteristics and Operating Conditions for Differential signals (1.2V V_{CCQ})

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
Differential AC input high voltage	DQS_t, DSQ_c, RE_t, RE_c	$V_{IHdiff(AC)}$	2 x [$V_{IH(DC)}$ - V_{REF}]	–	See Note	V	on page
Differential AC input low voltage		$V_{ILdiff(AC)}$	See Note	–	2 × [V_{REF} - $V_{IL(AC)}$]	V	on page
Differential DC input high voltage	DQS_t, DSQ_c, RE_t, RE_c	$V_{IHdiff(DC)}$	2 × [$V_{IH(DC)}$ - V_{REF}]	–	See Note	V	on page
Differential DC input low voltage		$V_{ILdiff(DC)}$	See Note	–	2 × [V_{REF} - $V_{IL(DC)}$]	V	on page
Input leakage current	Any input V_{IN} = 0V to V_{CCQ}	I_{LI}	–	–	±10	µA	on page
Output leakage current	DQ are disabled; V_{OUT} = V_{CCQ}	I_{LO_pd}	–	0.3	1	µA	4
	DQ are disabled; V_{OUT} = 0V; ODT disabled	I_{LO_pu}	–	0.9	5	µA	
Output low current (R/B#)	V_{OL} = 0.2V	I_{OL} (R/B#)	3	4	–	mA	on page

Table 93: NV-DDR3 DC Characteristics and Operating Conditions for Differential signals (1.2V V_{CCQ}) (Continued)

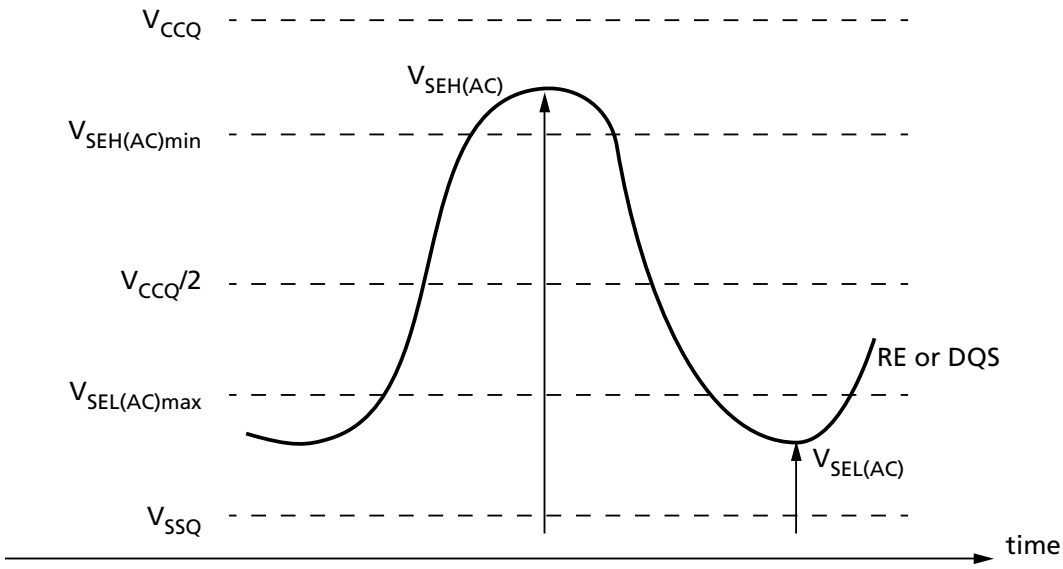
Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
V_{REFQ} leakage current	V_{REFQ}= V_{CCQ}/2 (all other pins not under test = 0V)	I_{VREFQ}	–	–	±5	µA	

Notes:
1. All leakage currents are per die (LUN). For example, two die (LUNs) have a maximum leakage current of ±20µA and four die (LUNs) have a maximum leakage current of ±40µA.
2. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [$V_{IH(DC)}$ Max, $V_{IL(DC)}$ Min] for single-ended signals as well as the limitations for overshoot and undershoot.
3. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full strength. See Table 29 (page 117) for additional details.
4. Absolute leakage value per I/O per NAND die (DQ[7:0], DQS_t, DQS_c, RE_t, RE_c).

Single-Ended Requirements for Differential signals

Each individual component of a differential signal (RE_t, RE_c, DQS_t, or DQS_c) shall comply with requirements for single-ended signals. RE_t and RE_c shall meet $V_{SEH(AC)}$ Min / $V_{SEL(AC)}$ Max in every half-cycle. DQS_t and DQS_c shall meet $V_{SEH(AC)}$ Min / $V_{SEL(AC)}$ Max in every half-cycle preceeding and following a valid transition.

Figure 107: Single-Ended requirements for Differential Signals



While control (e.g., ALE, CLE) and DQ signal requirements are with respect to VREF, the single-ended components of differential signals have a requirement with respect to V_{CCQ}/2; this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach $V_{SEL(AC)}$ Max, $V_{SEH(AC)}$ Min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 94: Single-Ended Levels for RE_t, RE_c, DQS_t, DQS_c for NV-DDR3 (1.2V V_{CCQ})

Parameter	Symbol	Min	Max	Unit	Notes
Single-Ended high level	$V_{SEH(AC)}$	V_{CCQ}/2 + 0.150	See note	V	1
Single-Ended low level	$V_{SEL(AC)}$	See note	V_{CCQ}/2 - 0.150	V	1

Note: 1. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [$V_{IH(DC)}$ Max, $V_{IL(DC)}$ Min] for single-ended signals as well as the limitations for overshoot and undershoot.

Table 95: Differential AC Input/Ouput Parameters

Parameter	Symbol	Min	Max	Unit	Notes
AC differential input cross-point voltage relative to V_{CCQ} / 2: NV-DDR2 interface	$V_{IX(AC)}$	0.5 x V_{CCQ} - 0.175	0.5 x V_{CCQ} + 0.175	V	1
AC differential input cross-point voltage relative to V_{CCQ} / 2: NV-DDR3 interface	$V_{IX(AC)}$	0.5 x V_{CCQ} - 0.120	0.5 x V_{CCQ} + 0.120	V	1
AC differential output cross-point voltage without ZQ calibration	$V_{OX(AC)}$	0.5 x V_{CCQ} - 0.2	0.5 x V_{CCQ} + 0.2	V	2, 3, 4
AC differential output cross-point voltage with ZQ calibration	$V_{OX(AC)}$	0.5 x V_{CCQ} - 0.150	0.5 x V_{CCQ} + 0.150	V	2, 3, 4

Notes:
1. The typical value of $V_{IX(AC)}$ is expected to be 0.5 x V_{CCQ} of the transmitting device. $V_{IX(AC)}$ is expected to track variations in V_{CCQ}. $V_{IX(AC)}$ indicates the voltage at which differential input signals shall cross.
2. The typical value of $V_{OX(AC)}$ is expected to be 0.5 x V_{CCQ} of the transmitting device. $V_{OX(AC)}$ is expected to track variations in V_{CCQ}. $V_{OX(AC)}$ indicates the voltage at which differential input signals shall cross.
3. $V_{OX(AC)}$ is measured with ½ DQ signals per data byte driving logic HIGH and ½ DQ signals per data byte driving logic LOW.
4. $V_{OX(AC)}$ is verified by design and characterization; it may not be subject to production testing.

Electrical Specifications – AC Characteristics and Operating Conditions (Asynchronous)

Table 96: AC Characteristics: Asynchronous Command, Address, and Data

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock period		100		50		35		30		25		20		ns	
Frequency		≈10		≈20		≈28		≈33		≈40		≈50		MHz	
ALE to data start	^{t}ADL	150	–	150	–	150	–	150	–	150	–	150	–	ns	1
ALE hold time	^{t}ALH	20	–	10	–	10	–	5	–	5	–	5	–	ns	
ALE setup time	^{t}ALS	50	–	25	–	15	–	10	–	10	–	10	–	ns	
ALE to RE# delay	^{t}AR	25	–	10	–	10	–	10	–	10	–	10	–	ns	
CE# access time	^{t}CEA	–	100	–	45	–	30	–	25	–	25	–	25	ns	

Table 96: AC Characteristics: Asynchronous Command, Address, and Data (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CE# HIGH hold time prior to VOLUME SELECT (E1h)	tCEH	20	–	20	–	20	–	20	–	20	–	20	–	ns	
CE# hold time	tCH	20	–	10	–	10	–	5	–	5	–	5	–	ns	
Delay before CE# HIGH for any Volume after a Volume is selected	tCEVDLY	50	–	50	–	50	–	50	–	50	–	50	–	ns	
CE# HIGH to output High-Z	tCHZ	–	100	–	50	–	50	–	50	–	30	–	30	ns	2
CLE hold time	tCLH	20	–	10	–	10	–	5	–	5	–	5	–	ns	
CLE to RE# delay	tCLR	20	–	10	–	10	–	10	–	10	–	10	–	ns	
CLE setup time	tCLS	50	–	25	–	15	–	10	–	10	–	10	–	ns	
CE# HIGH to output hold	tCOH	0	–	15	–	15	–	15	–	15	–	15	–	ns	
CE# setup time	tCS	70	–	35	–	25	–	25	–	20	–	15	–	ns	
CE# to RE# LOW or RE_t / RE_c	tCR	10	–	10	–	10	–	10	–	10	–	10	–	ns	
CE# to RE# LOW after CE# has been HIGH for > 1µs	tCR2	100	–	100	–	100	–	100	–	100	–	100	–	ns	
	tCR2 (Read ID)	150	–	150	–	150	–	150	–	150	–	150	–	ns	5
CE# setup time for data input after CE# has been HIGH for > 1µs	tCS3	100	–	100	–	100	–	100	–	100	–	100	–	ns	
Data hold time	tDH	20	–	10	–	5	–	5	–	5	–	5	–	ns	
Data setup time	tDS	40	–	20	–	15	–	10	–	10	–	7	–	ns	
ENi LOW until any issued command is ignored	tENi	–	15	–	15	–	15	–	15	–	15	–	15	ns	
CE# LOW until ENo LOW	tENo	–	50	–	50	–	50	–	50	–	50	–	50	ns	
Output High-Z to RE# LOW	tIR	10	–	0	–	0	–	0	–	0	–	0	–	ns	
RE# cycle time	tRC	100	–	50	–	35	–	30	–	25	–	20	–	ns	
RE# access time	tREA	–	40	–	30	–	25	–	20	–	20	–	16	ns	3
RE# HIGH hold time	tREH	30	–	15	–	15	–	10	–	10	–	7	–	ns	3
RE# HIGH to output hold	tRHOH	0	–	15	–	15	–	15	–	15	–	15	–	ns	3

Table 96: AC Characteristics: Asynchronous Command, Address, and Data (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
RE# HIGH to WE# LOW	tRHW	200	–	100	–	100	–	100	–	100	–	100	–	ns	
RE# HIGH to output High-Z	tRHZ	–	200	–	100	–	100	–	100	–	100	–	100	ns	2, 3
RE# LOW to output hold	tRLOH	0	–	0	–	0	–	0	–	5	–	5	–	ns	3
RE# pulse width	tRP	50	–	25	–	17	–	15	–	12	–	10	–	ns	
Ready to RE# LOW	tRR	40	–	20	–	20	–	20	–	20	–	20	–	ns	
WE# HIGH to R/B# LOW	tWB	–	200	–	100	–	100	–	100	–	100	–	100	ns	4
WE# cycle time	tWC	100	–	45	–	35	–	30	–	25	–	20	–	ns	
WE# HIGH hold time	tWH	30	–	15	–	15	–	10	–	10	–	7	–	ns	
WE# HIGH to RE# LOW	tWHR	120	–	80	–	80	–	60	–	60	–	60	–	ns	
WE# pulse width	tWP	50	–	25	–	17	–	15	–	12	–	10	–	ns	
WP# transition to WE# LOW	tWW	100	–	100	–	100	–	100	–	100	–	100	–	ns	
Delay before next command after a Volume is selected	tVDLY	50	–	50	–	50	–	50	–	50	–	50	–	ns	

Notes:
1. Timing for tADL begins in the address cycle, on the final rising edge of WE# and ends with the first rising edge of WE# for data input. tADL SPEC for SET FEATURES operations is 70ns.
2. Data transition is measured ±200mV from steady-steady voltage with load. This parameter is sampled and not 100 percent tested.
3. AC characteristics may need to be relaxed if output drive strength is not set to at least nominal.
4. Do not issue a new command during tWB, even if R/B# or RDY is ready.
5. tCR2(min) is 150ns for Read ID sequence only. For all other command sequences tCR2(min) requirement is 100ns.

Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR, NV-DDR2, NV-DDR3)

Table 97: AC Characteristics: NV-DDR Command, Address, and Data

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock period		50		30		20		15		12		10		ns	
Frequency		≈20		≈33		≈50		≈67		≈83		≈100		MHz	
Access window of DQ[7:0] from CLK	^{t}AC	3	20	3	20	3	20	3	20	3	20	3	20	ns	
ALE to data loading time	^{t}ADL	150	–	150	–	150	–	150	–	150	–	150	–	ns	6
Command, address data delay	^{t}CAD	25	–	25	–	25	–	25	–	25	–	25	–	ns	1
DQ hold – command, address	^{t}CAH	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
ALE, CLE, W/R# hold	^{t}CALH	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
ALE, CLE, W/R# setup	^{t}CALS	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
DQ setup – command, address	^{t}CAS	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
CE# HIGH hold time prior to VOLUME SELECT (E1h)	^{t}CEH	20	–	20	–	20	–	20	–	20	–	20	–	ns	
Delay before CE# HIGH for any Volume after a Volume is selected	^{t}CEVDLY	50	–	50	–	50	–	50	–	50	–	50	–	ns	
CE# hold	^{t}CH	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
Average CLK cycle time	^{t}CK (avg)	50	100	30	50	20	30	15	20	12	15	10	12	ns	2
Absolute CLK cycle time, from rising edge to rising edge	^{t}CK (abs)	^{t}CK (abs) MIN = ^{t}CK (avg) + ^{t}JIT (per) MIN ^{t}CK (abs) MAX = ^{t}CK (avg) + ^{t}JIT (per) MAX												ns	
CLK cycle HIGH	^{t}CKH (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	^{t}CK	3
CLK cycle LOW	^{t}CKL (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	^{t}CK	3

Table 97: AC Characteristics: NV-DDR Command, Address, and Data (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Data output end to W/R# HIGH	tCKWR	tCKWR(MIN) = RoundUp[(tDQSCK(MAX) + tCK)/tCK]												tCK	
CE# setup time for data input and data output after CE# has been HIGH for > 1µs	tCS3	75	–	75	–	75	–	75	–	75	–	75	–	ns	
CE# setup	tCS	35	–	25	–	15	–	15	–	15	–	15	–	ns	
Data In hold	tDH	5	–	2.5	–	1.7	–	1.3	–	1.1	–	0.9	–	ns	
Access window of DQS from CLK	tDQSCK	–	20	–	20	–	20	–	20	–	20	–	20	ns	
DQS, DQ[7:0] Driven by NAND	tDQSD	–	18	–	18	–	18	–	18	–	18	–	18	ns	
DQS, DQ[7:0] to tri-state	tDQSHZ	–	20	–	20	–	20	–	20	–	20	–	20	ns	4
DQS input high pulse width	tDQSH	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS input low pulse width	tDQSL	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS-DQ skew	tDQSQ	–	5	–	2.5	–	1.7	–	1.3	–	1.0	–	0.85	ns	
Data input	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
Data In setup	tDS	5	–	3	–	2	–	1.5	–	1.1	–	0.9	–	ns	
DQS falling edge from CLK rising – hold	tDSH	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	tCK	
DQS falling to CLK rising – setup	tDSS	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	tCK	
Data valid window	tDVW	tDVW = tQH - tDQSQ												ns	
ENi LOW until any issued command is ignored	tENi	–	15	–	15	–	15	–	15	–	15	–	15	ns	
CE# LOW until ENo LOW	tENo	–	50	–	50	–	50	–	50	–	50	–	50	ns	
Half clock period	tHP	tHP = Min(tCKH, tCKL)												ns	

Table 97: AC Characteristics: NV-DDR Command, Address, and Data (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
The deviation of a given tCK (abs) from a tCK (avg)	tJIT (per)	–0.7	0.7	–0.7	0.7	–0.7	0.7	–0.6	0.6	–0.6	0.6	–0.5	0.5	ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	tQH	tQH = tHP - tQHS												ns	
Data hold skew factor	tQHS	–	6	–	3	–	2	–	1.5	–	1.2	–	1	ns	
Data output to command, address, or data input	tRHW	100	–	100	–	100	–	100	–	100	–	100	–	ns	
Ready to data output	tRR	20	–	20	–	20	–	20	–	20	–	20	–	ns	
CLK HIGH to R/B# LOW	tWB	–	100	–	100	–	100	–	100	–	100	–	100	ns	
Command cycle to data output	tWHR	80	–	80	–	80	–	80	–	80	–	80	–	ns	
DQS write preamble	tWPRE	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	tCK	
DQS write postamble	tWPST	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	tCK	
W/R# LOW to data output cycle	tWRCK	20	–	20	–	20	–	20	–	20	–	20	–	ns	
WP# transition to command cycle	tWW	100	–	100	–	100	–	100	–	100	–	100	–	ns	
Delay before next command after a Volume is selected	tVDLY	50	–	50	–	50	–	50	–	50	–	50	–	ns	

Notes:
1. Delay is from start of command to next command, address, or data cycle; start of address to next command, address, or data cycle; and end of data to start of next command, address, or data cycle.
2. tCK(avg) is the average clock period over any consecutive 200-cycle window.
3. tCKH(abs) and tCKL(abs) include static offset and duty cycle jitter.
4. tDQSHZ begins when W/R# is latched HIGH by CLK. This parameter is not referenced to a specific voltage level; it specifies when the device outputs are no longer driving.
5. If RESET (FFh) is issued when the target is idle, the target goes busy for a maximum of 5µs.

6. ^{t}ADL SPEC for SET FEATURES operations is 100ns.

Table 98: AC Characteristics: NV-DDR2/NV-DDR3 Command, Address, and Data for modes 0 - 4

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock period		30		25		15		12		10		ns	
Frequency		≈33		≈40		≈66		≈83		≈100		MHz	
Command and Address													
Access window of DQ[7:0] from RE# LOW or RE_t / RE_c	^{t}AC	3	25	3	25	3	25	3	25	3	25	ns	
ALE to data loading time	^{t}ADL	150	–	150	–	150	–	150	–	150	–	ns	13
ALE to RE# LOW or RE_t / RE_c	^{t}AR	10	–	10	–	10	–	10	–	10	–	ns	
DQ hold – command, address	^{t}CAH	5	–	5	–	5	–	5	–	5	–	ns	
ALE, CLE hold	^{t}CALH	5	–	5	–	5	–	5	–	5	–	ns	
ALE, CLE setup with ODT disabled	^{t}CALS	15	–	15	–	15	–	15	–	15	–	ns	
ALE, CLE setup with ODT enabled	^{t}CALS2	25	–	25	–	25	–	25	–	25	–	ns	
DQ setup – command, address	^{t}CAS	5	–	5	–	5	–	5	–	5	–	ns	
CE# HIGH hold time prior to VOLUME SELECT (E1h)	^{t}CEH	20	–	20	–	20	–	20	–	20	–	ns	
Delay before CE# HIGH for any Volume after a Volume is selected	^{t}CEVDLY	50	–	50	–	50	–	50	–	50	–	ns	
CE# hold	^{t}CH	5	–	5	–	5	–	5	–	5	–	ns	
CE# HIGH to output Hi-Z	^{t}CHZ	–	30	–	30	–	30	–	30	–	30	ns	1
CLE HIGH to output Hi-Z	^{t}CLHZ	–	30	–	30	–	30	–	30	–	30		1
CLE to RE# LOW or RE_t / RE_c	^{t}CLR	10	–	10	–	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t / RE_c	^{t}CR	10	–	10	–	10	–	10	–	10	–	ns	

Table 98: AC Characteristics: NV-DDR2/NV-DDR3 Command, Address, and Data for modes 0 - 4 (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CE# to RE# LOW or RE_t / RE_c if CE# has been HIGH for > 1µs	^{t}CR2	100	–	100	–	100	–	100	–	100	–	ns	
	^{t}CR2 (Read ID)	150	–	150	–	150	–	150	–	150	–	ns	14
CE# setup	^{t}CS	20	–	20	–	20	–	20	–	20	–	ns	
CE# setup for data output with ODT disabled	^{t}CS1	30	–	30	–	30	–	30	–	30	–	ns	
CE# setup for DQS/DQ[7:0] with ODT enabled	^{t}CS2	40	–	40	–	40	–	40	–	40	–	ns	
CE# setup time to DQS_t low after CE# has been HIGH for > 1µs	^{t}CD	100	–	100	–	100	–	100	–	100	–	ns	
ALE, CLE, WE#, hold time from CE# HIGH	^{t}CSD	10	–	10	–	10	–	10	–	10	–	ns	
ENi LOW until any issued command is ignored	^{t}ENi	–	15	–	15	–	15	–	15	–	15	ns	
CE_# LOW until ENo LOW	^{t}ENo	–	50	–	50	–	50	–	50	–	50	ns	
Ready to data output	^{t}RR	20	–	20	–	20	–	20	–	20	–	ns	
CLK HIGH to R/B# LOW	^{t}WB	–	100	–	100	–	100	–	100	–	100	ns	
WE# cycle time	^{t}WC	25	–	25	–	25	–	25	–	25	–	ns	
WE# pulse width	^{t}WH	11	–	11	–	11	–	11	–	11	–	ns	
Command cycle to data output	^{t}WHR	80	–	80	–	80	–	80	–	80	–	ns	
WE# pulse width	^{t}WP	11	–	11	–	11	–	11	–	11	–	ns	
WP# transition to command cycle	^{t}WW	100	–	100	–	100	–	100	–	100	–	ns	
Delay before next command after a Volume is selected	^{t}VDLY	50	–	50	–	50	–	50	–	50	–	ns	
Jitter													

Table 98: AC Characteristics: NV-DDR2/NV-DDR3 Command, Address, and Data for modes 0 - 4 (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
The deviation of a given ^{t}DQS (abs) / ^{t}DSC (abs) from a ^{t}DQS (avg) / ^{t}DSC (avg)	^{t}JITper (DQS)	-2.4	2.4	-2.0	2.0	-1.2	1.2	–1.0	1.0	-0.8	0.8	ns	3, 5, 7
The deviation of a given ^{t}RC (abs) / ^{t}DSC (abs) from a ^{t}RC (avg) / ^{t}DSC (avg)	^{t}JITper (RE#)	-1.8	1.8	-1.5	1.5	-0.9	0.9	-0.75	0.75	–0.6	0.6	ns	3, 5, 7
Cycle to cycle jitter for DQS	^{t}JITcc (DQS)	4.8	–	4.0	–	2.4	–	2.0	–	1.6	–	ns	3, 6
Cycle to cycle jitter for RE#	^{t}JITcc (RE#)	3.6	–	3.0	–	1.8	–	1.5	–	1.2	–	ns	3, 6
Data Input													
DQS setup time for data input start	^{t}CDQSS	30	–	30	–	30	–	30	–	30	–	ns	
DQS hold time for data input burst end	^{t}CDQSH	100	–	100	–	100	–	100	–	100	–	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	^{t}DBS	5	–	5	–	5	–	5	–	5	–	ns	
Data In hold	^{t}DH	4.0	–	3.3	–	2.0	–	1.1	–	0.7	–	ns	10
Data In setup	^{t}DS	4.0	–	3.3	–	2.0	–	1.1	–	0.7	–	ns	10
DQ input pulse width	^{t}DIPW	0.31	–	0.31	–	0.31	–	0.31	–	0.31	–	^{t}DSC(avg)	12
DQS input high pulse width	^{t}DQSH	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	^{t}DSC (avg)	
DQS input low pulse width	^{t}DQSL	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	^{t}DSC (avg)	
Average DQS cycle time	^{t}DSC (avg) or ^{t}DSC	30	–	25	–	15	–	12	–	10	–	ns	2

Table 98: AC Characteristics: NV-DDR2/NV-DDR3 Command, Address, and Data for modes 0 - 4 (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Absolute DQS cycle time, from rising edge to rising edge	^{t}DSC (abs)	^{t}DSC (abs) MIN = ^{t}DSC (avg) + ^{t}JITper(DQS) MIN ^{t}DSC (abs) MAX = ^{t}DSC (avg) + ^{t}JITper(DQS) MAX				^{t}DSC (abs) MIN = ^{t}DSC (avg) + ^{t}JITper(DQS) MIN ^{t}DSC (abs) MAX = ^{t}DSC (avg) + ^{t}JITper(DQS) MAX						ns	
ENi LOW until any issued command is ignored	^{t}ENi	–	15	–	15	–	15	–	15	–	15	ns	
CE# LOW until ENo LOW	^{t}ENo	–	50	–	50	–	50	–	50	–	50	ns	
DQS write preamble with ODT disabled	^{t}WPRE	15	–	15	–	15	–	15	–	15	–	ns	
DQS write preamble with ODT enabled	^{t}WPRE2	25	–	25	–	25	–	25	–	25	–	ns	
DQS write postamble	^{t}WPST	6.5	–	6.5	–	6.5	–	6.5	–	6.5	–	ns	
DQS write postamble hold time	^{t}WPSTH	15	–	15	–	15	–	15	–	15	–	ns	
Data Output													
Access window of DQ[7:0] from CLK	^{t}AC	3	25	3	25	3	25	3	25	3	25	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	^{t}DBS	5	–	5	–	5	–	5	–	5	–	ns	
DQS-DQ skew	^{t}DQSQ	–	2.5	–	2.0	–	1.4	–	1.0	–	0.8	ns	
Access window of DQS from RE# or RE_t / RE_c	^{t}DQSRE	3	25	3	25	3	25	3	25	3	25	ns	
RE# LOW to DQS or DQ[7:0] driven	^{t}DQSD	6	18	6	18	6	18	6	18	6	18	ns	

Table 98: AC Characteristics: NV-DDR2/NV-DDR3 Command, Address, and Data for modes 0 - 4 (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS hold time after RE# LOW or RE_t/RE_c cross-point	tDQSRH	5	–	5	–	5	–	5	–	5	–	ns	15
Data valid window	tDVW	tDVW = tQH - tDQSQ								tDVW = tQH - tDQSQ		ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	tQH	0.37	–	0.37	–	0.37	–	0.37	–	0.37	–	tRC (avg)	9, 11
DQS (DQS_t / DQS_c) output HIGH time	tQSH	0.37	–	0.37	–	0.37	–	0.37	–	0.37	–	tRC (avg)	9, 11
DQS (DQS_t / DQS_c) output LOW time	tQSL	0.37	–	0.37	–	0.37	–	0.37	–	0.37	–	tRC (avg)	9, 11
Average RE# cycle time	tRC (avg) or tRC	30	–	25	–	15	–	12	–	10	–	ns	2
Absolute RE# cycle time	tRC (abs)	tRC (abs) MIN = tRC (avg) + tJITper(RE#) MIN tRC (abs) MAX = tRC (avg) + tJITper(RE#) MAX								tRC (abs) MIN = tRC (avg) + tJITper(RE#) MIN tRC (abs) MAX = tRC (avg) + tJITper(RE#) MAX		ns	
Average RE# HIGH hold time	tREH (avg)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC (avg)	4
Absolute RE# HIGH hold time	tREH (abs)	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	tRC (avg)	
Data output to command, address, or data input	tRHW	100	–	100	–	100	–	100	–	100	–	ns	
Average RE# pulse width	tRP (avg)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tRC (avg)	4
Absolute RE# pulse width	tRP (abs)	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	tRC (avg)	
Read preamble with ODT disabled	tRPRE	15	–	15	–	15	–	15	–	15	–	ns	

Table 98: AC Characteristics: NV-DDR2/NV-DDR3 Command, Address, and Data for modes 0 - 4 (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read preamble with ODT enabled	tRPRE2	25	–	25	–	25	–	25	–	25	–	ns	
Read postamble	tRPST	tDQSRE + 0.5 * tRC	–	tDQSRE + 0.5 * tRC	–	tDQSRE + 0.5 * tRC	–	tDQSRE + 0.5 * tRC	–	tDQSRE + 0.5 * tRC	–	ns	
Read postable hold time	tRPSTH	15	–	15	–	15	–	15	–	15	–	ns	

Notes:
1. tCHZ and tCLHZ are not referenced to a specific voltage level, but specify when the device output is no longer driving.
2. The parameters tRC(avg) and tDSC(avg) are the average over any 200 consecutive periods and tRC(avg) / tDSC(avg) min are the smallest rates allowed, with the exception of a deviation due to tJIT (per).
3. Input jitter is allowed provided it does not exceed values specified.
4. tREH(avg) and tRP(avg) are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter. Input clock jitter is allowed provided it does not exceed values specified.
5. The period jitter tJIT (per) is the maximum deviation in the tRC or tDSC period from the average or nominal tRC or tDSC period. It is allowed in either the positive or negative direction.
6. The cycle-to-cycle jitter tJITcc is the amount the clock period can deviate from one cycle to the next.
7. The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed tJITper. As long as the absolute minimum half period tRP(abs), tREH(abs), tDQSH or tDQSL is not less than 43 percent of the average cycle.
8. All timing parameter values assume differential signaling for RE# and DQS is used.
9. When the device is operated with input clock jitter, tQSL, tQSH, and tQH need to be derated by the actual tJITper in the input clock. (output deratings are relative to the NAND input RE pulse that generated the DQS pulse).
10. The tDS and tDH times listed are based on an input slew rate of 1 V/ns. If the input slew rate is not 1 V/ns, then the derating methodology shall be used.
11. When the device is operated with input RE (RE_t/RE_c) jitter, tQSL, tQSH, and tQH need to be derated by the actual input duty cycle jitter beyond 0.45 * tRC(avg) but not exceeding 0.43 * tRC(avg). Output deratings are relative to the device input RE pulse that generated the DQS pulse.
12. The parameter tDIPW is defined as the pulse width of the input signal between the first crossing of $V_{REFQ(DC)}$ and the consecutive crossing of $V_{REFQ(DC)}$.
13. tADL SPEC for SET FEATURES operations is 100ns.
14. tCR2(min) is 150ns for Read ID sequence only. For all other command sequences tCR2(min) requirement is 100ns.
15. tDQSRH is only required if Matrix ODT is enabled.

Table 99: AC Characteristics: NV-DDR2/NV-DDR3 Command, Address, and Data for timing modes 5 - 7

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock period		7.5		6		5		ns	
Frequency		≈133		≈166		≈200		MHz	
Command and Address									
Access window of DQ[7:0] from RE# LOW or RE_t / RE_c	^{t}AC	3	25	3	25	3	25	ns	
ALE to data loading time	^{t}ADL	150	–	150	–	150	–	ns	13
ALE to RE# LOW or RE_t / RE_c	^{t}AR	10	–	10	–	10	–	ns	
DQ hold – command, address	^{t}CAH	5	–	5	–	5	–	ns	
ALE, CLE hold	^{t}CALH	5	–	5	–	5	–	ns	
ALE, CLE setup with ODT disabled	^{t}CALS	15	–	15	–	15	–	ns	
ALE, CLE setup with ODT enabled	^{t}CALS2	25	–	25	–	25	–	ns	
DQ setup – command, address	^{t}CAS	5	–	5	–	5	–	ns	
CE# HIGH hold time	^{t}CEH	20	–	20	–	20	–	ns	
Delay before CE# HIGH for any Volume after a Volume is selected	^{t}CEVDLY	50	–	50	–	50	–	ns	
CE# hold	^{t}CH	5	–	5	–	5	–	ns	
CE# HIGH to output Hi-Z	^{t}CHZ	–	30	–	30	–	30	ns	1
CLE HIGH to output Hi-Z	^{t}CLHZ	–	30	–	30	–	30		1
CLE to RE# LOW or RE_t / RE_c	^{t}CLR	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t / RE_c	^{t}CR	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t / RE_c if CE# has been HIGH for > 1µs	^{t}CR2	100	–	100	–	100	–	ns	
	^{t}CR2 (Read ID)	150	–	150	–	150	–	ns	14
CE# setup	^{t}CS	20	–	20	–	20	–	ns	
CE# setup for data output with ODT disabled	^{t}CS1	30	–	30	–	30	–	ns	

Table 99: AC Characteristics: NV-DDR2/NV-DDR3 Command, Address, and Data for timing modes 5 - 7 (Continued)

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
CE# setup for DQS/DQ[7:0] with ODT enabled	^{t}CS2	40	–	40	–	40	–	ns	
CE# setup time to DQS_t low after CE# has been HIGH for > 1µs	^{t}CD	100	–	100	–	100	–	ns	
ALE, CLE, WE#, hold time from CE# HIGH	^{t}CSD	10	–	10	–	10	–	ns	
ENi LOW until any issued command is ignored	^{t}ENi	–	15	–	15	–	15	ns	
CE# LOW until ENo LOW	^{t}ENo	–	50	–	50	–	50	ns	
Ready to data output	^{t}RR	20	–	20	–	20	–	ns	
CLK HIGH to R/B# LOW	^{t}WB	–	100	–	100	–	100	ns	
WE# cycle time	^{t}WC	25	–	25	–	25	–	ns	
WE# pulse width	^{t}WH	11	–	11	–	11	–	ns	
Command cycle to data output	^{t}WHR	80	–	80	–	80	–	ns	
WE# pulse width	^{t}WP	11	–	11	–	11	–	ns	
WP# transition to command cycle	^{t}WW	100	–	100	–	100	–	ns	
Delay before next command after a Volume is selected	^{t}VDLY	50	–	50	–	50	–	ns	
Jitter									
The deviation of a given ^{t}DQS (abs) / ^{t}DSC (abs) from a ^{t}DQS (avg) / ^{t}DSC (avg)	^{t}JITper (DQS)	-0.6	0.6	-0.48	0.48	-0.40	0.40	ns	3, 5, 7
The deviation of a given ^{t}RC (abs) / ^{t}DSC (abs) from a ^{t}RC (avg) / ^{t}DSC (avg)	^{t}JITper (RE#)	–0.45	0.45	–0.36	0.36	–0.30	0.30	ns	3, 5, 7
Cycle to cycle jitter for DQS	^{t}JITcc (DQS)	1.2	–	0.96	–	0.80	–	ns	3, 6
Cycle to cycle jitter for RE#	^{t}JITcc (RE#)	0.9	–	0.72	–	0.60	–	ns	3, 6
Data Input									

Table 99: AC Characteristics: NV-DDR2/NV-DDR3 Command, Address, and Data for timing modes 5 - 7 (Continued)

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
DQS setup time for data input start	tCDQSS	30	–	30	–	30	–	ns	
DQS hold time for data input burst end	tCDQSH	100	–	100	–	100	–	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	tDBS	5	–	5	–	5	–	ns	
Data In hold	tDH	0.6	–	0.55	–	0.40	–	ns	10
Data In setup	tDS	0.6	–	0.55	–	0.40	–	ns	10
DQ input pulse width	tDIPW	0.31	–	0.31	–	0.31	–	tDSC(avg)	12
DQS input high pulse width	tDQSH	0.43	–	0.43	–	0.43	–	tDSC (avg)	
DQS input low pulse width	tDQSL	0.43	–	0.43	–	0.43	–	tDSC (avg)	
Average DQS cycle time	tDSC (avg) or tDSC	7.5	–	6	–	5	–	ns	2
Absolute DQS cycle time, from rising edge to rising edge	tDSC (abs)	tDSC (abs) MIN = tDSC (avg) + tJITper(DQS) MIN tDSC (abs) MAX = tDSC (avg) + tJITper(DQS) MAX						ns	
ENi LOW until any issued command is ignored	tENi	–	15	–	15	–	15	ns	
CE# LOW until ENo LOW	tENo	–	50	–	50	–	50	ns	
DQS write preamble with ODT disabled	tWPRE	15	–	15	–	15	–	ns	
DQS write preamble with ODT enabled	tWPRE2	25	–	25	–	25	–	ns	
DQS write postamble	tWPST	6.5	–	6.5	–	6.5	–	ns	
DQS write postamble hold time	tWPSTH	15	–	15	–	15	–	ns	
Data Output									
Access window of DQ[7:0] from CLK	tAC	3	25	3	25	3	25	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	tDBS	5	–	5	–	5	–	ns	
DQS-DQ skew	tDQSQ	–	0.6	–	0.5	–	0.4	ns	

Table 99: AC Characteristics: NV-DDR2/NV-DDR3 Command, Address, and Data for timing modes 5 - 7 (Continued)

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Access window of DQS from RE# or RE_t / RE_c	tDQSRE	3	25	3	25	3	25	ns	
RE# LOW to DQS or DQ[7:0] driven	tDQSD	6	18	6	18	6	18	ns	
DQS hold time after RE# LOW or RE_t/RE_c crosspoint	tDQSRH	5	–	5	–	5	–	ns	15
Data valid window	tDVW	tDVW = tQH - tDQSQ						ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	tQH	0.37	–	0.37	–	0.37	–	tRC (avg)	9, 11
DQS (DQS_t /DQS_c) output HIGH time	tQSH	0.37	–	0.37	–	0.37	–	tRC (avg)	9, 11
DQS (DQS_t /DQS_c) output LOW time	tQSL	0.37	–	0.37	–	0.37	–	tRC (avg)	9, 11
Average RE# cycle time	tRC (avg) or tRC	7.5	–	6	–	5	–	ns	2
Absolute RE# cycle time	tRC (abs)	tRC (abs) MIN = tRC (avg) + tJITper(RE#) MIN tRC (abs) MAX = tRC (avg) + tJITper(RE#) MAX						ns	
Average RE# HIGH hold time	tREH (avg)	0.45	0.55	0.45	0.55	0.45	0.55	tRC (avg)	4
Absolute RE# HIGH hold time	tREH (abs)	0.43	–	0.43	–	0.43	–	tRC (avg)	
Data output to command, address, or data input	tRHW	100	–	100	–	100	–	ns	
Average RE# pulse width	tRP (avg)	0.45	0.55	0.45	0.55	0.45	0.55	tRC (avg)	4
Absolute RE# pulse width	tRP (abs)	0.43	–	0.43	–	0.43	–	tRC (avg)	
Read preamble with ODT disabled	tRPRE	15	–	15	–	15	–	ns	
Read preamble with ODT enabled	tRPRE2	25	–	25	–	25	–	ns	
Read postamble	tRPST	tDQSRE + 0.5 * tRC	–	tDQSRE + 0.5 * tRC	–	tDQSRE + 0.5 * tRC	–	ns	
Read postable hold time	tRPSTH	15	–	15	–	15	–	ns	

Notes: 1. tCHZ and tCLHZ are not referenced to a specific voltage level, but specify when the device output is no longer driving.

2. The parameters tRC(avg) and tDSC(avg) are the average over any 200 consecutive periods and tRC(avg) / tDSC(avg) min are the smallest rates allowed, with the exception of a deviation due to tJIT (per).
3. Input jitter is allowed provided it does not exceed values specified.
4. tREH(avg) and tRP(avg) are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter. Input clock jitter is allowed provided it does not exceed values specified.
5. The period jitter tJIT (per) is the maximum deviation in the tRC or tDSC period from the average or nominal tRC or tDSC period. It is allowed in either the positive or negative direction.
6. The cycle-to-cycle jitter tJITcc is the amount the clock period can deviate from one cycle to the next.
7. The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed tJITper. As long as the absolute minimum half period tRP(abs), tREH(abs), tDQSH or tDQSL is not less than 43 percent of the average cycle.
8. All timing parameter values assume differential signaling for RE# and DQS is used.
9. When the device is operated with input clock jitter, tQSL, tQSH, and tQH need to be derated by the actual tJITper in the input clock. (output deratings are relative to the NAND input RE pulse that generated the DQS pulse).
10. The tDS and tDH times listed are based on an input slew rate of 1 V/ns. If the input slew rate is not 1 V/ns, then the derating methodology shall be used.
11. When the device is operated with input RE (RE_t/RE_c) jitter, tQSL, tQSH, and tQH need to be derated by the actual input duty cycle jitter beyond 0.45 * tRC(avg) but not exceeding 0.43 * tRC(avg). Output deratings are relative to the device input RE pulse that generated the DQS pulse.
12. The parameter tDIPW is defined as the pulse width of the input signal between the first crossing of $V_{REFQ(DC)}$ and the consecutive crossing of $V_{REFQ(DC)}$.
13. tADL SPEC for SET FEATURES operations is 100ns.
14. tCR2(min) is 150ns for Read ID sequence only. For all other command sequences tCR2(min) requirement is 100ns.
15. tDQSRH is only required if Matrix ODT is enabled.

Table 100: AC Characteristics: NV-DDR2/NV-DDR3 Command, Address, and Data for timing modes 8 - 10

Parameter	Symbol	Mode 8		Mode 9		Mode 10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock period		3.75		3		2.5		ns	
Frequency		≈266		≈333		≈400		MHz	
Command and Address									
Access window of DQ[7:0] from RE# LOW or RE_t / RE_c	tAC	3	25	3	25	3	25	ns	
ALE to data loading time	tADL	150	–	150	–	150	–	ns	13
ALE to RE# LOW or RE_t / RE_c	tAR	10	–	10	–	10	–	ns	
DQ hold – command, address	tCAH	5	–	5	–	5	–	ns	
ALE, CLE hold	tCALH	5	–	5	–	5	–	ns	

Release: 11/30/15

Table 100: AC Characteristics: NV-DDR2/NV-DDR3 Command, Address, and Data for timing modes 8 - 10 (Continued)

Parameter	Symbol	Mode 8		Mode 9		Mode 10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
ALE, CLE setup with ODT disabled	^{t}CALS	15	–	15	–	15	–	ns	
ALE, CLE setup with ODT enabled	^{t}CALS2	25	–	25	–	25	–	ns	
DQ setup – command, address	^{t}CAS	5	–	5	–	5	–	ns	
CE# HIGH hold time	^{t}CEH	20	–	20	–	20	–	ns	
Delay before CE# HIGH for any Volume after a Volume is selected	^{t}CEVDLY	50	–	50	–	50	–	ns	
CE# hold	^{t}CH	5	–	5	–	5	–	ns	
CE# HIGH to output Hi-Z	^{t}CHZ	–	30	–	30	–	30	ns	1
CLE HIGH to output Hi-Z	^{t}CLHZ	–	30	–	30	–	30		1
CLE to RE# LOW or RE_t / RE_c	^{t}CLR	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t / RE_c	^{t}CR	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t / RE_c if CE# has been HIGH for > 1µs	^{t}CR2	100	–	100	–	100	–	ns	
	^{t}CR2 (Read ID)	150	–	150	–	150	–	ns	14
CE# setup	^{t}CS	20	–	20	–	20	–	ns	
CE# setup for data output with ODT disabled	^{t}CS1	30	–	30	–	30	–	ns	
CE# setup for DQS/DQ[7:0] with ODT enabled	^{t}CS2	40	–	40	–	40	–	ns	
CE# setup time to DQS_t low after CE# has been HIGH for > 1µs	^{t}CD	100	–	100	–	100	–	ns	
ALE, CLE, WE#, hold time from CE# HIGH	^{t}CSD	10	–	10	–	10	–	ns	
ENi LOW until any issued command is ignored	^{t}ENi	–	15	–	15	–	15	ns	
CE_# LOW until ENo LOW	^{t}ENo	–	50	–	50	–	50	ns	
Ready to data output	^{t}RR	20	–	20	–	20	–	ns	
CLK HIGH to R/B# LOW	^{t}WB	–	100	–	100	–	100	ns	

Release: 11/30/15

Table 100: AC Characteristics: NV-DDR2/NV-DDR3 Command, Address, and Data for timing modes 8 - 10 (Continued)

Parameter	Symbol	Mode 8		Mode 9		Mode 10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
WE# cycle time	tWC	25	–	25	–	25	–	ns	
WE# pulse width	tWH	11	–	11	–	11	–	ns	
Command cycle to data output	tWHR	80	–	80	–	80	–	ns	
WE# pulse width	tWP	11	–	11	–	11	–	ns	
WP# transition to command cycle	tWW	100	–	100	–	100	–	ns	
Delay before next command after a Volume is selected	tVDLY	50	–	50	–	50	–	ns	
Jitter									
The deviation of a given tDQS (abs) / tDSC (abs) from a tDQS (avg) / tDSC (avg)	tJITper (DQS)	-0.30	0.30	-0.24	0.24	-0.20	0.20	ns	3, 5, 7
The deviation of a given tRC (abs) / tDSC (abs) from a tRC (avg) / tDSC (avg)	tJITper (RE#)	–0.225	0.225	–0.18	0.18	–0.15	0.15	ns	3, 5, 7
Cycle to cycle jitter for DQS	tJITcc (DQS)	0.6	–	0.48	–	0.40	–	ns	3, 6
Cycle to cycle jitter for RE#	tJITcc (RE#)	0.45	–	0.36	–	0.30	–	ns	3, 6
Data Input									
DQS setup time for data input start	tCDQSS	30	–	30	–	30	–	ns	
DQS hold time for data input burst end	tCDQSH	100	–	100	–	100	–	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	tDBS	5	–	5	–	5	–	ns	
Data In hold	tDH	0.30	–	0.24	–	0.20	–	ns	10
Data In setup	tDS	0.30	–	0.24	–	0.20	–	ns	10
DQ input pulse width	tDIPW	0.31	–	0.31	–	0.31	–	tDSC(avg)	12
DQS input high pulse width	tDQSH	0.43	–	0.43	–	0.43	–	tDSC (avg)	
DQS input low pulse width	tDQSL	0.43	–	0.43	–	0.43	–	tDSC (avg)	

Table 100: AC Characteristics: NV-DDR2/NV-DDR3 Command, Address, and Data for timing modes 8 - 10 (Continued)

Parameter	Symbol	Mode 8		Mode 9		Mode 10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Average DQS cycle time	tDSC (avg) or tDSC	3.75	–	3	–	2.5	–	ns	2
Absolute DQS cycle time, from rising edge to rising edge	tDSC (abs)	tDSC (abs) MIN = tDSC (avg) + tJITper(DQS) MIN tDSC (abs) MAX = tDSC (avg) + tJITper(DQS) MAX						ns	
ENi LOW until any issued command is ignored	tENi	–	15	–	15	–	15	ns	
CE# LOW until ENo LOW	tENo	–	50	–	50	–	50	ns	
DQS write preamble with ODT disabled	tWPRE	15	–	15	–	15	–	ns	
DQS write preamble with ODT enabled	tWPRE2	25	–	25	–	25	–	ns	
DQS write postamble	tWPST	6.5	–	6.5	–	6.5	–	ns	
DQS write postamble hold time	tWPSTH	15	–	15	–	15	–	ns	
Data Output									
Access window of DQ[7:0] from CLK	tAC	3	25	3	25	3	25	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	tDBS	5	–	5	–	5	–	ns	
DQS-DQ skew	tDQSQ	–	0.350	–	0.30	–	0.25	ns	
Access window of DQS from RE# or RE_t / RE_c	tDQSRE	3	25	3	25	3	25	ns	
RE# LOW to DQS or DQ[7:0] driven	tDQSD	6	18	6	18	6	18	ns	
DQS hold time after RE# LOW or RE_t/RE_c crosspoint	tDQSRH	5	–	5	–	5	–	ns	15
Data valid window	tDVW	tDVW = tQH - tDQSQ						ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	tQH	0.37	–	0.37	–	0.37	–	tRC (avg)	9, 11
DQS (DQS_t /DQS_c) output HIGH time	tQSH	0.37	–	0.37	–	0.37	–	tRC (avg)	9, 11
DQS (DQS_t /DQS_c) output LOW time	tQSL	0.37	–	0.37	–	0.37	–	tRC (avg)	9, 11
Average RE# cycle time	tRC (avg) or tRC	3.75	–	3	–	2.5	–	ns	2

Table 100: AC Characteristics: NV-DDR2/NV-DDR3 Command, Address, and Data for timing modes 8 - 10 (Continued)

Parameter	Symbol	Mode 8		Mode 9		Mode 10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Absolute RE# cycle time	tRC (abs)	tRC (abs) MIN = tRC (avg) + tJITper(RE#) MIN tRC (abs) MAX = tRC (avg) + tJITper(RE#) MAX						ns	
Average RE# HIGH hold time	tREH (avg)	0.45	0.55	0.45	0.55	0.45	0.55	tRC (avg)	4
Absolute RE# HIGH hold time	tREH (abs)	0.43	–	0.43	–	0.43	–	tRC (avg)	
Data output to command, address, or data input	tRHW	100	–	100	–	100	–	ns	
Average RE# pulse width	tRP (avg)	0.45	0.55	0.45	0.55	0.45	0.55	tRC (avg)	4
Absolute RE# pulse width	tRP (abs)	0.43	–	0.43	–	0.43	–	tRC (avg)	
Read preamble with ODT disabled	tRPRE	15	–	15	–	15	–	ns	
Read preamble with ODT enabled	tRPRE2	25	–	25	–	25	–	ns	
Read postamble	tRPST	tDQSRE + 0.5 * tRC	–	tDQSRE + 0.5 * tRC	–	tDQSRE + 0.5 * tRC	–	ns	
Read postable hold time	tRPSTH	15	–	15	–	15	–	ns	

Notes:
1. tCHZ and tCLHZ are not referenced to a specific voltage level, but specify when the device output is no longer driving.
2. The parameters tRC(avg) and tDSC(avg) are the average over any 200 consecutive periods and tRC(avg) / tDSC(avg) min are the smallest rates allowed, with the exception of a deviation due to tJIT (per).
3. Input jitter is allowed provided it does not exceed values specified.
4. tREH(avg) and tRP(avg) are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter. Input clock jitter is allowed provided it does not exceed values specified.
5. The period jitter tJIT (per) is the maximum deviation in the tRC or tDSC period from the average or nominal tRC or tDSC period. It is allowed in either the positive or negative direction.
6. The cycle-to-cycle jitter tJITcc is the amount the clock period can deviate from one cycle to the next.
7. The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed tJITper. As long as the absolute minimum half period tRP(abs), tREH(abs), tDQSH or tDQSL is not less than 43 percent of the average cycle.
8. All timing parameter values assume differential signaling for RE# and DQS is used.
9. When the device is operated with input clock jitter, tQSL, tQSH, and tQH need to be derated by the actual tJITper in the input clock. (output deratings are relative to the NAND input RE pulse that generated the DQS pulse).

10. The ^{t}DS and ^{t}DH times listed are based on an input slew rate of 1 V/ns. If the input slew rate is not 1 V/ns, then the derating methodology shall be used.
11. When the device is operated with input RE (RE_t/RE_c) jitter, ^{t}QSL, ^{t}QSH, and ^{t}QH need to be derated by the actual input duty cycle jitter beyond 0.45 * ^{t}RC(avg) but not exceeding 0.43 * ^{t}RC(avg). Output deratings are relative to the device input RE pulse that generated the DQS pulse.
12. The parameter ^{t}DIPW is defined as the pulse width of the input signal between the first crossing of $V_{REFQ(DC)}$ and the consecutive crossing of $V_{REFQ(DC)}$.
13. ^{t}ADL SPEC for SET FEATURES operations is 100ns.
14. ^{t}CR2(min) is 150ns for Read ID sequence only. For all other command sequences ^{t}CR2(min) requirement is 100ns.
15. ^{t}DQSRH is only required if Matrix ODT is enabled.

Electrical Specifications – Array Characteristics

Table 101: Array Characteristics

Parameter	Symbol	Typ	Max	Unit	Notes
Number of partial page programs	NOP	–	1	Cycles	1
ERASE BLOCK operation time	^{t}BERS	15	45	ms	7
Cache busy	^{t}CBSY	1100	2500	µs	
Change column setup time to data in/out or next command	^{t}CCS	–	400	ns	
Dummy busy time	^{t}DBSY	0.5	1	µs	
ERASE SUSPEND operation time	^{t}ESPD	–	800	µs	
Busy time when ERASE SUSPEND is issued when LUN is already in the suspend state or ERASE RESUME is issued when no erase is suspended or ongoing	^{t}ESPDN	–	18	µs	
Busy time for SET FEATURES and GET FEATURES operations	^{t}FEAT	–	1	µs	
Busy time for interface change	^{t}ITC	–	1	µs	2
LAST PAGE PROGRAM operation time	^{t}LPROG	–	–	µs	3
Busy time for OTP DATA PROGRAM operation if OTP is protected	^{t}OBSY	–	100	µs	
Power-on reset time	^{t}POR	–	3	ms	
PROGRAM PAGE operation time without/with V_{PP}	^{t}PROG	1300/1225	2500	µs	6
PROGRAM SUSPEND operation time	^{t}PSPD	150	500	µs	
Internal Randomization time	^{t}RAND	–	25	µs	9
Multi-Plane READ PAGE operation time without/with V_{PP}	^{t}R	77/63	117/88	µs	5, 9
Single-Plane READ PAGE operation time without/with V_{PP}	^{t}R_SP	66/63	93/88	µs	5, 9
Cache read busy time	^{t}RCBSY	26	117	µs	5, 9
Multi-Plane EXPRESS READ operation time without/with V_{PP}	^{t}RER	75/61	115/86	µs	9
Single-Plane EXPRESS READ operation time without/with V_{PP}	^{t}RER_SP	64/61	91/86	µs	9
Snap Read operation time	^{t}RSNAP	37	46	µs	10
Device reset time (Read/Program/Erase)	^{t}RST	–	10/30/500	µs	4
Busy time for GET FEATURES operation for Temperature sensor readout	^{t}TEMP	–	120	µs	
Full calibration time	^{t}ZQCL	1	–	µs	8
Short calibration time	^{t}ZQCS	0.3	–	µs	8

Notes:
1. The pages in the OTP Block have an NOP of 2.
2. ^{t}ITC (MAX) is the busy time when the interface changes from asynchronous to NV-DDR/NV-DDR2 using the SET FEATURES (EFh) command or synchronous to asynchronous using the RESET (FFh) command. During the ^{t}ITC time, any command, including READ STATUS (70h) and READ STATUS ENHANCED (78h), is prohibited.
3. ^{t}LPROG = ^{t}PROG (last page) + ^{t}PROG (last page - 1) - command load time (last page) - address load time (last page) - data load time (last page).
4. If RESET command is issued when the target is READY, the target goes busy for a maximum of 5µs.
5. For Read Retry options 8 to 15, ^{t}R and ^{t}RCBSY Max may be up to TBDµs.
6. In the case of a program operation that exceeds ^{t}PROG/^{t}CBSY Max, that specific NAND block may be retired by the host system.

7. In the case of a erase operation that exceeds ^{t}BERS Max, that specific NAND block may be retired by the host system.
8. Increased time beyond TYP may result when greater than 8 LUNs share a ZQ resistor.
9. With Randomizer enabled, the total array read time for a given parameter will be the value of that parameter + ^{t}RAND
10. Snap Read can not be used when the internal NAND randomizer is enabled.

Asynchronous Interface Timing Diagrams

Figure 108: RESET Operation

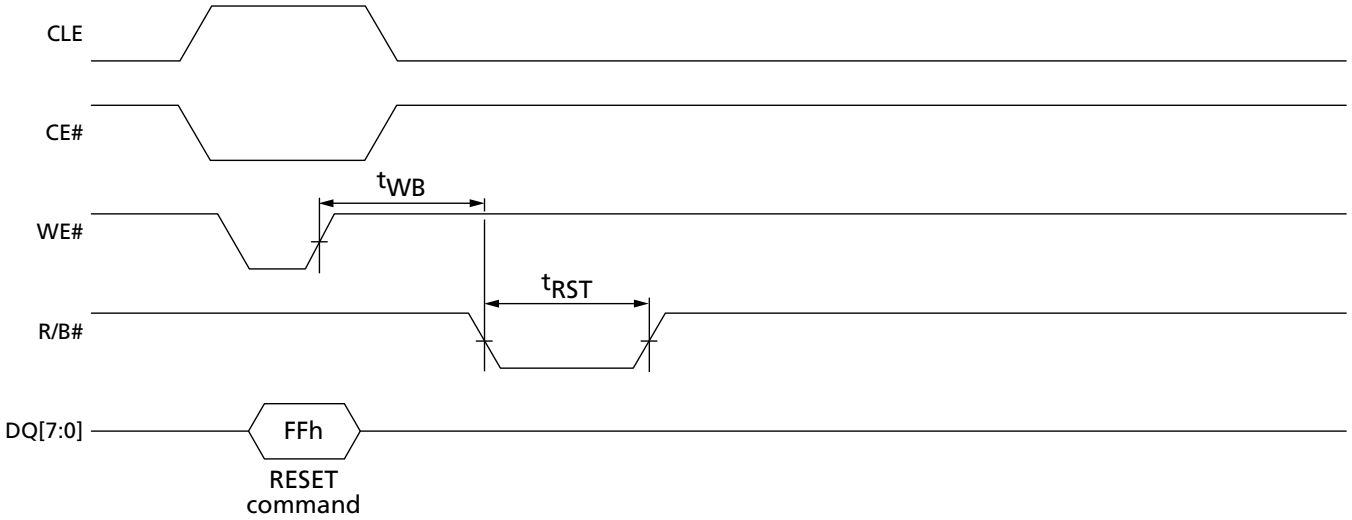


Figure 109: RESET LUN Operation

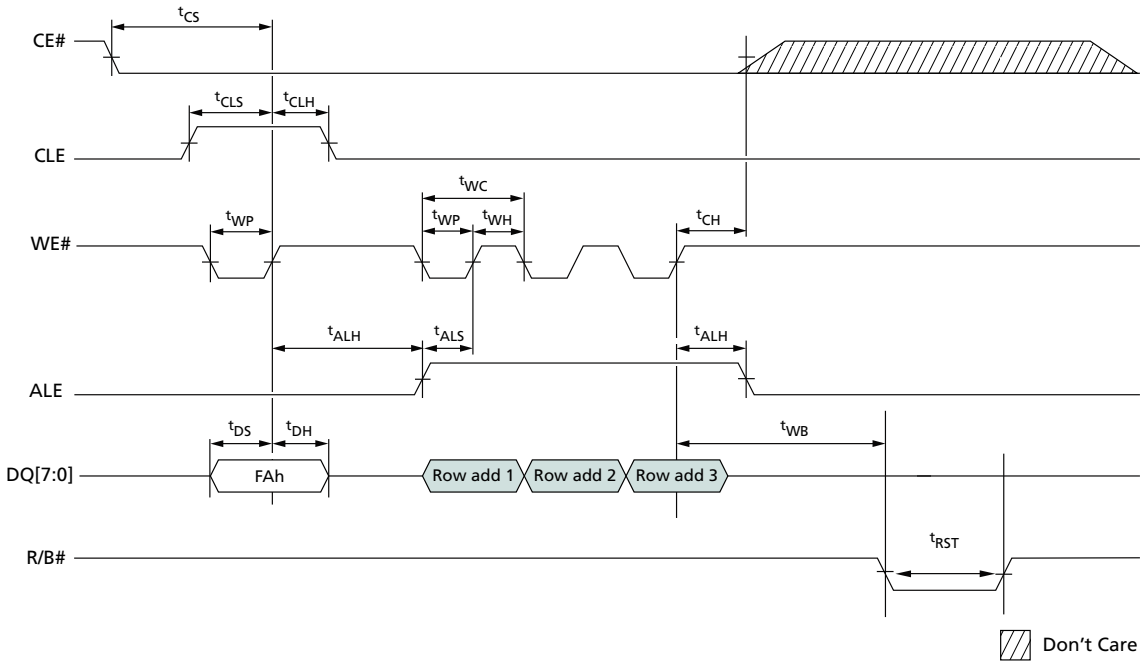


Figure 110: READ STATUS Cycle

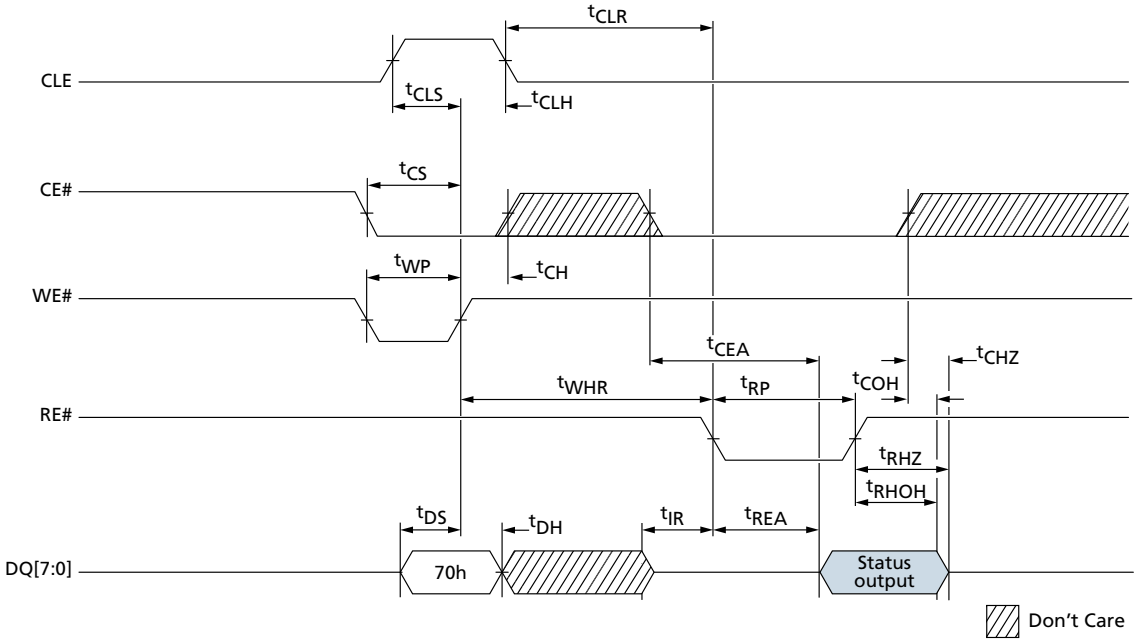


Figure 111: READ STATUS ENHANCED Cycle

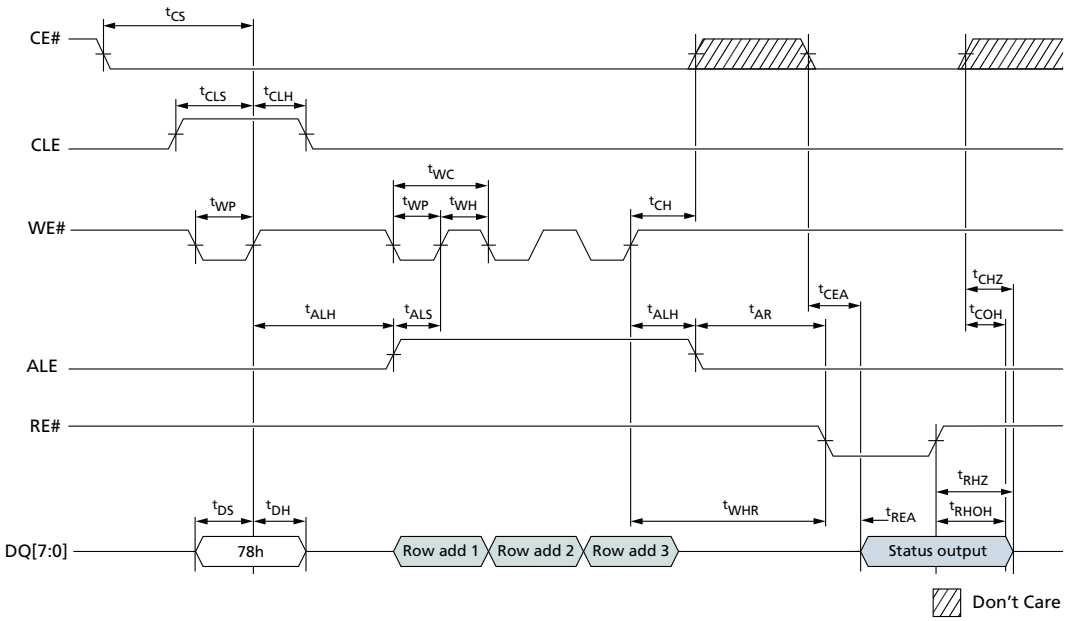


Figure 112: READ PARAMETER PAGE

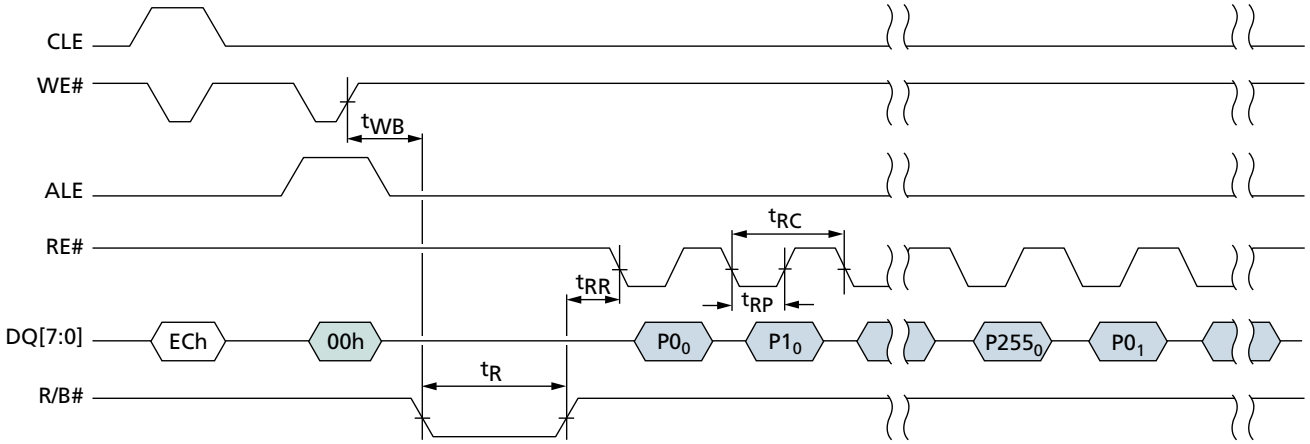


Figure 113: READ PAGE

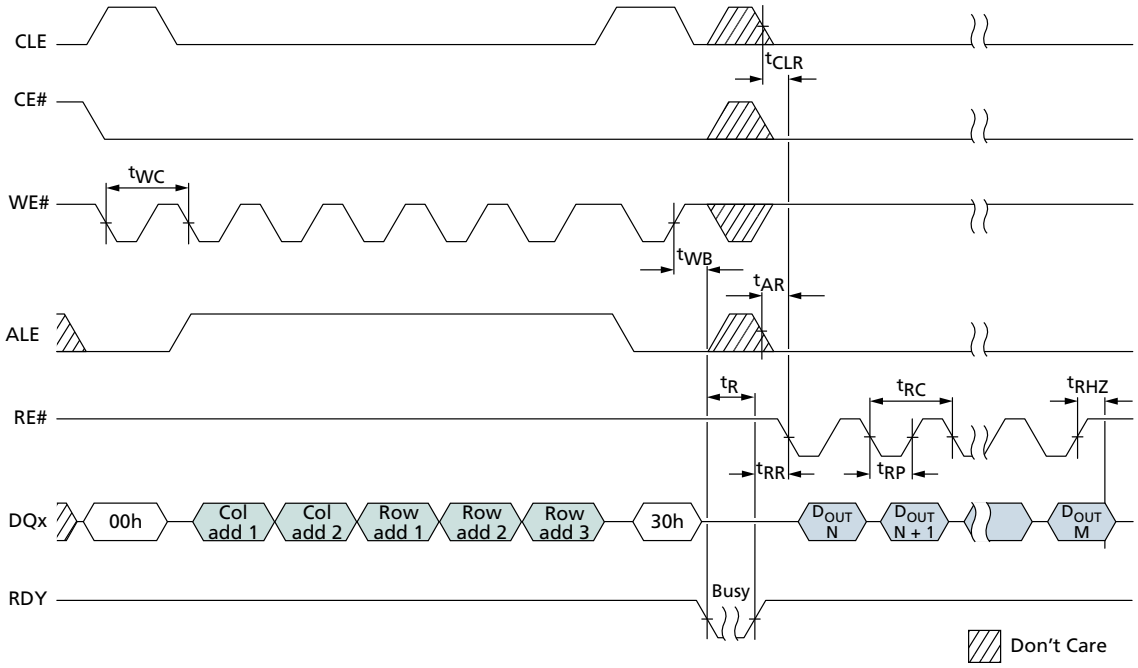


Figure 114: READ PAGE Operation with CE# "Don't Care"

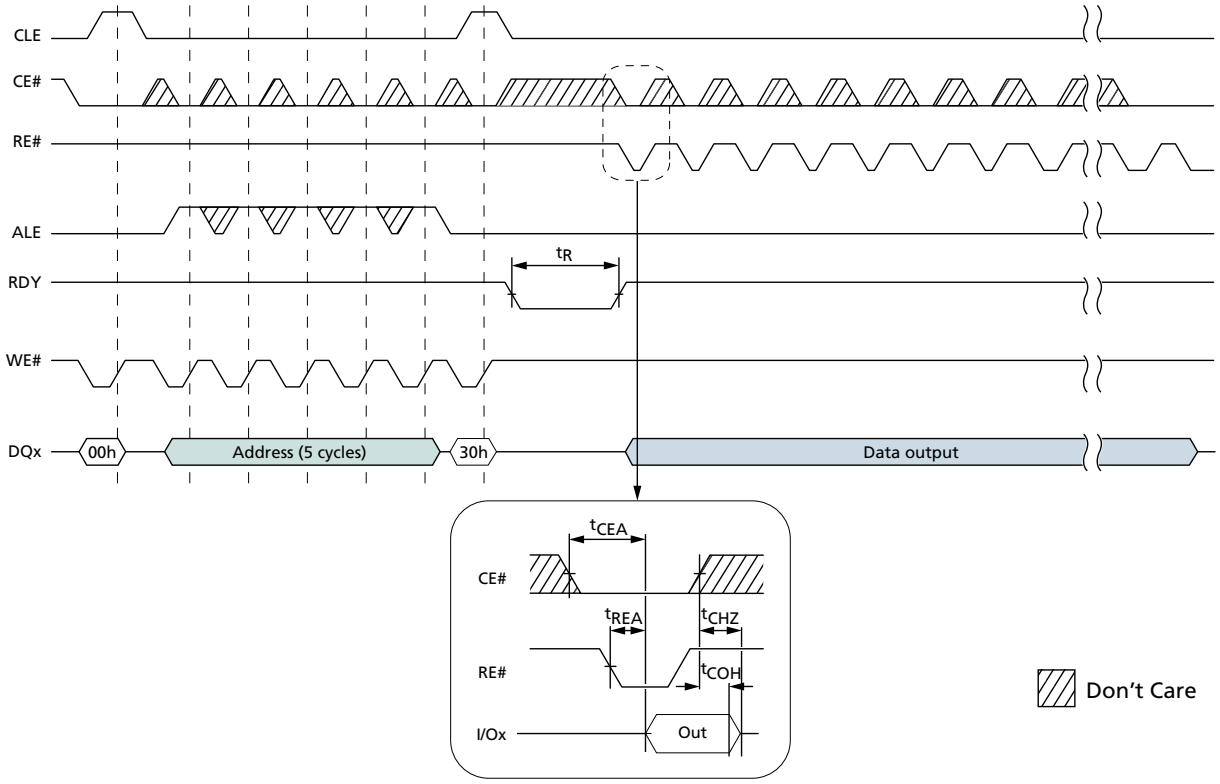


Figure 115: CHANGE READ COLUMN

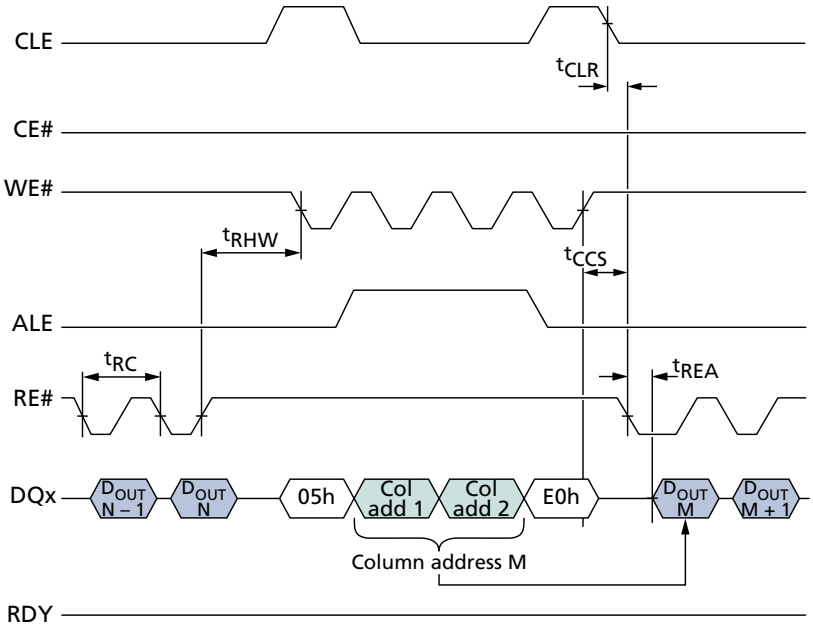


Figure 116: READ PAGE CACHE SEQUENTIAL

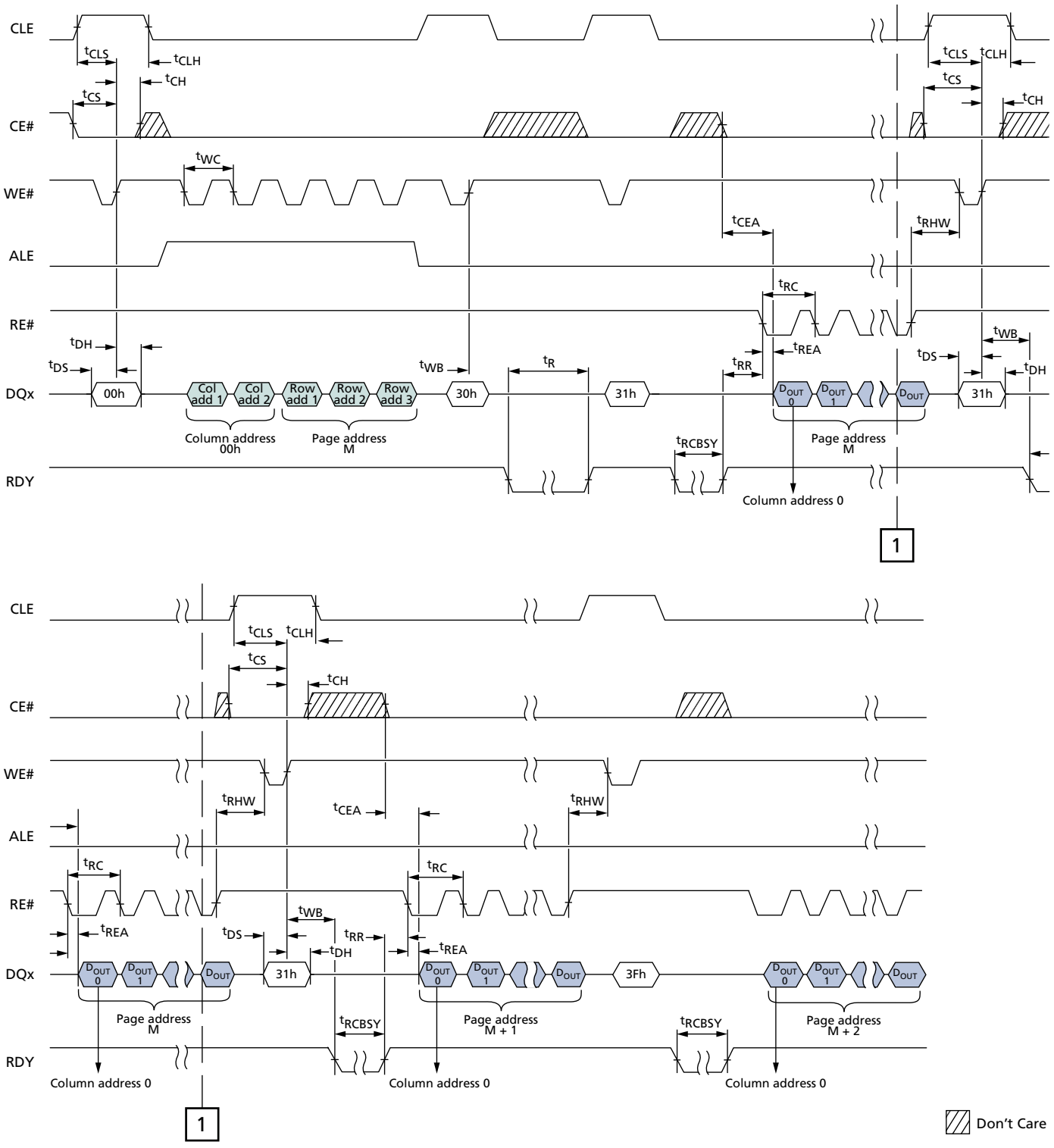


Figure 117: READ PAGE CACHE RANDOM

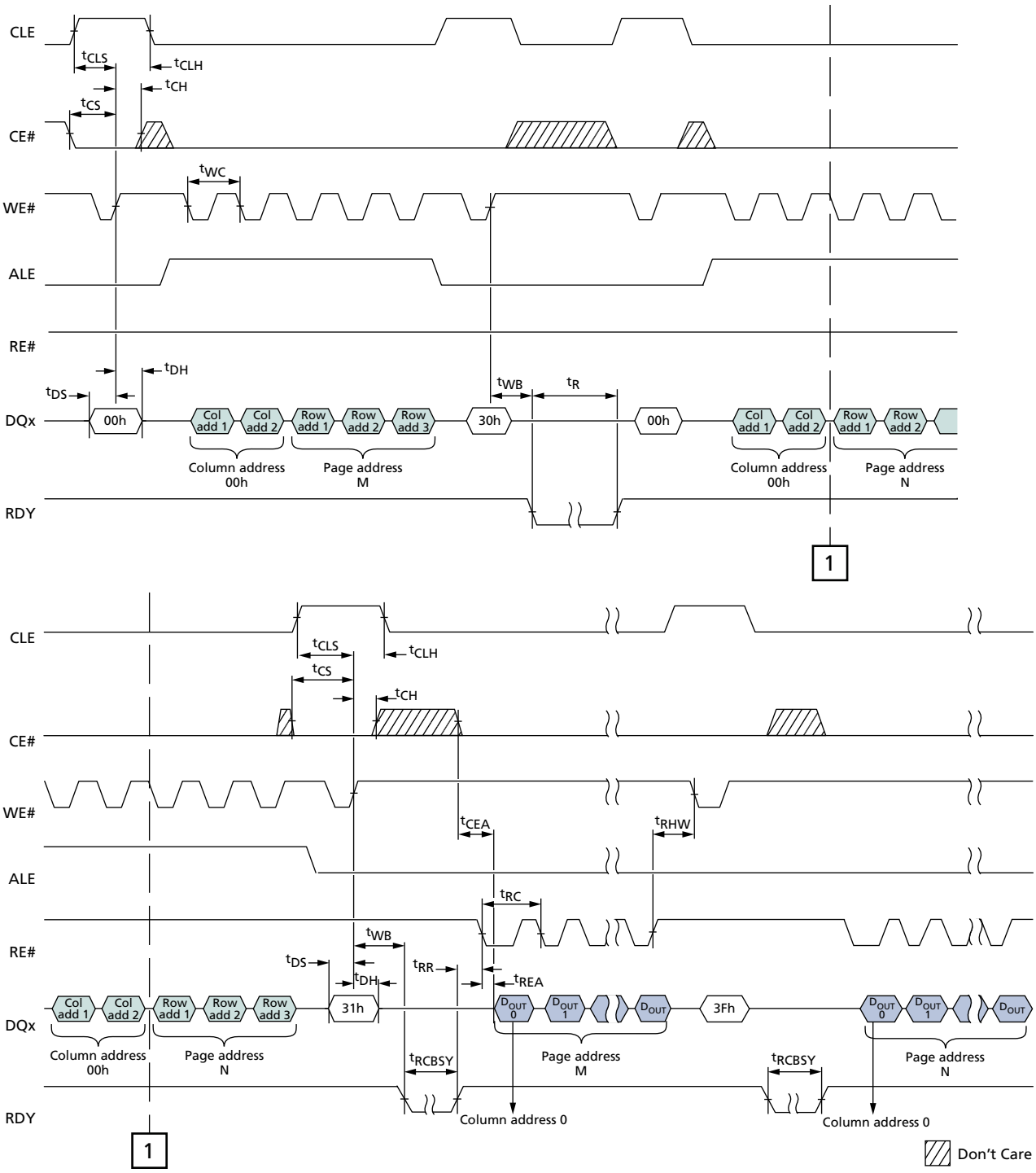


Figure 118: READ ID Operation

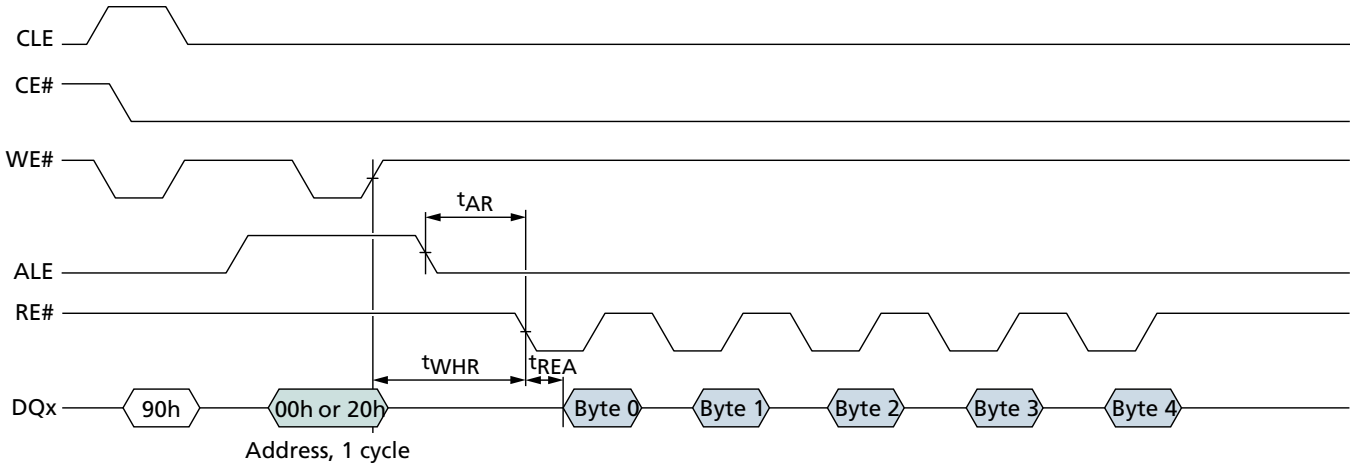


Figure 119: PROGRAM PAGE Operation

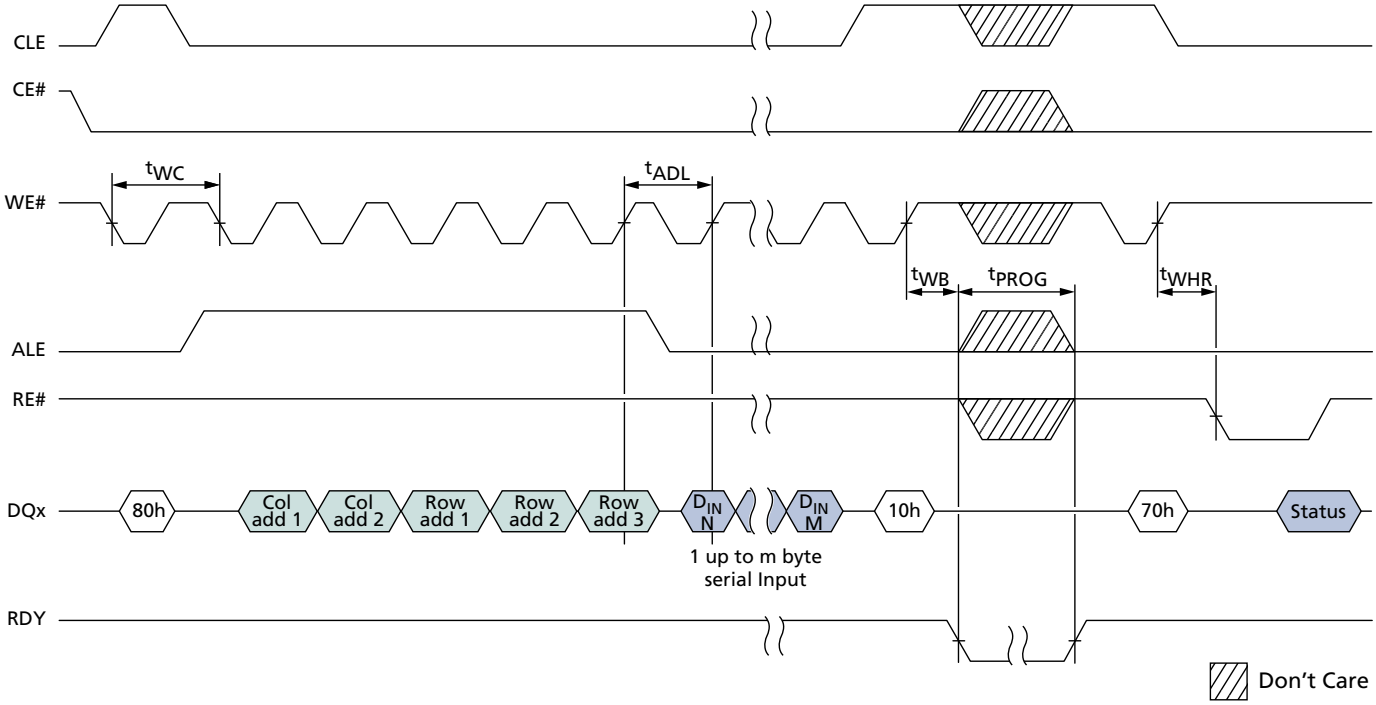


Figure 120: PROGRAM PAGE Operation with CE# "Don't Care"

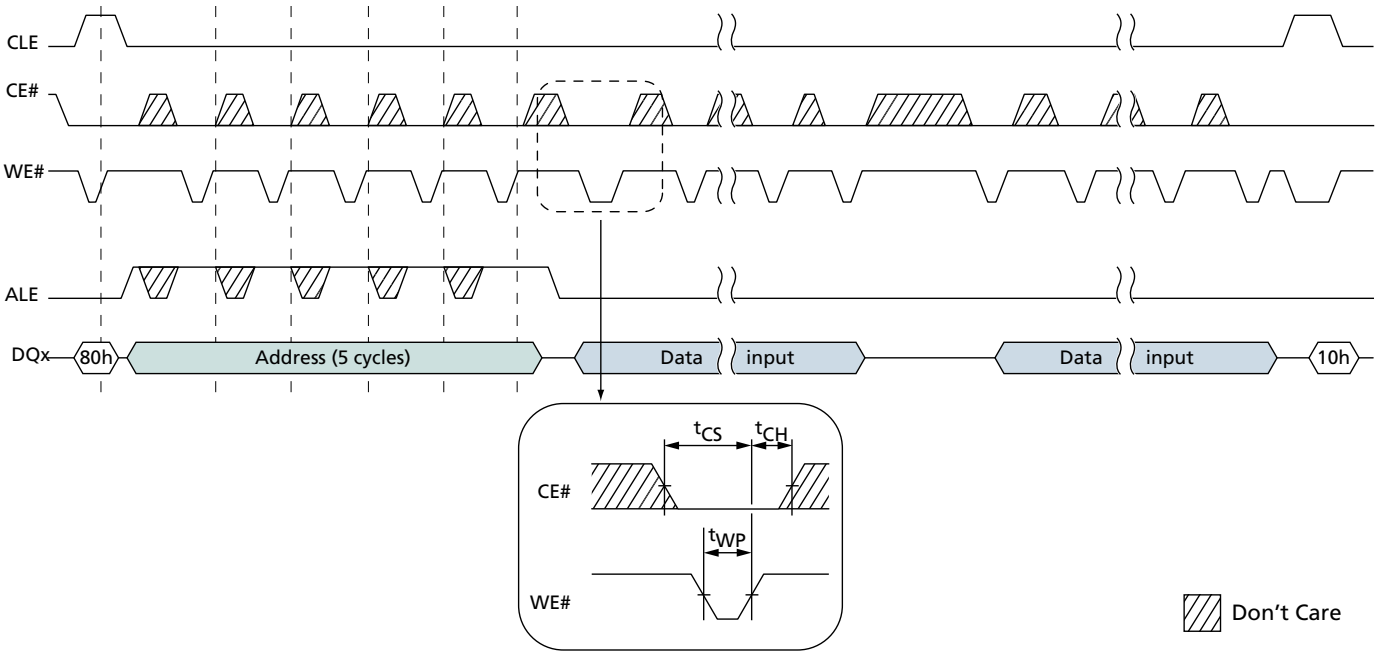


Figure 121: PROGRAM PAGE Operation with CHANGE WRITE COLUMN

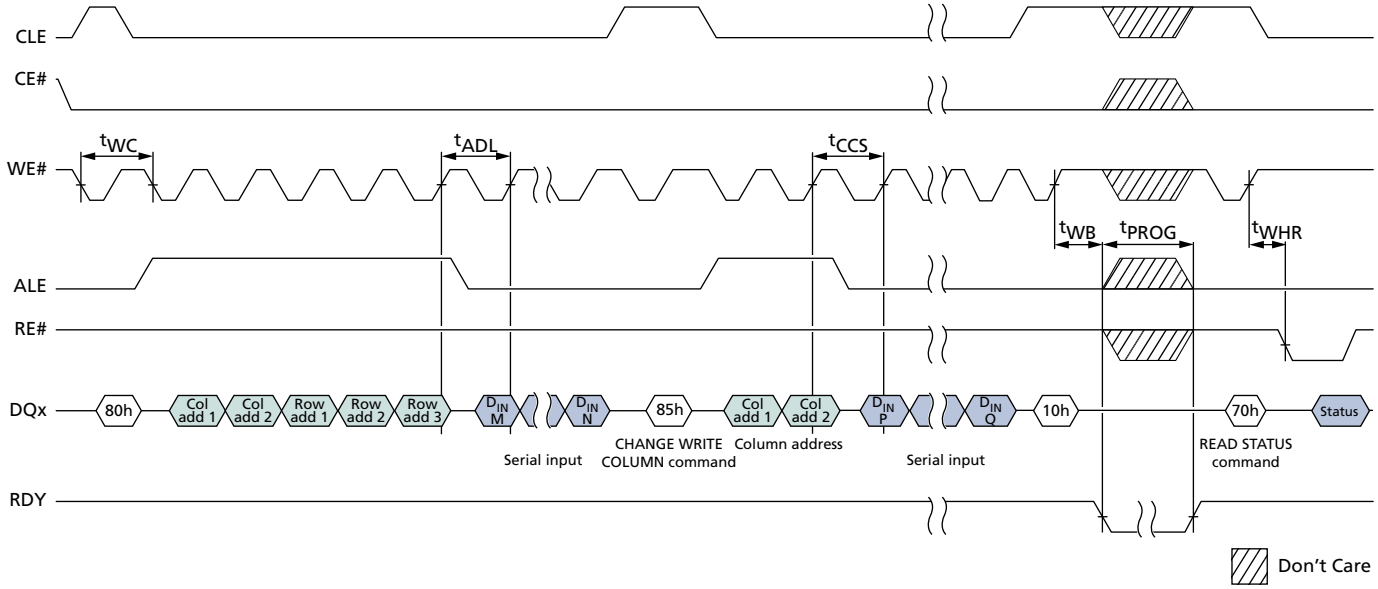


Figure 122: PROGRAM PAGE CACHE

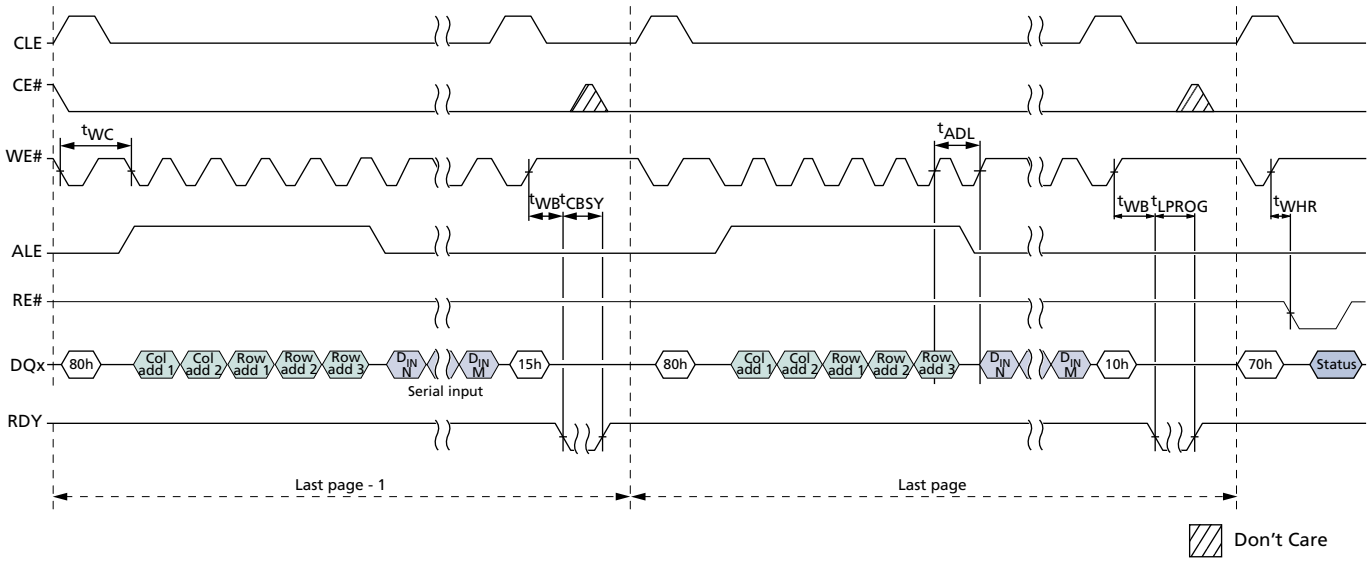


Figure 123: PROGRAM PAGE CACHE Ending on 15h

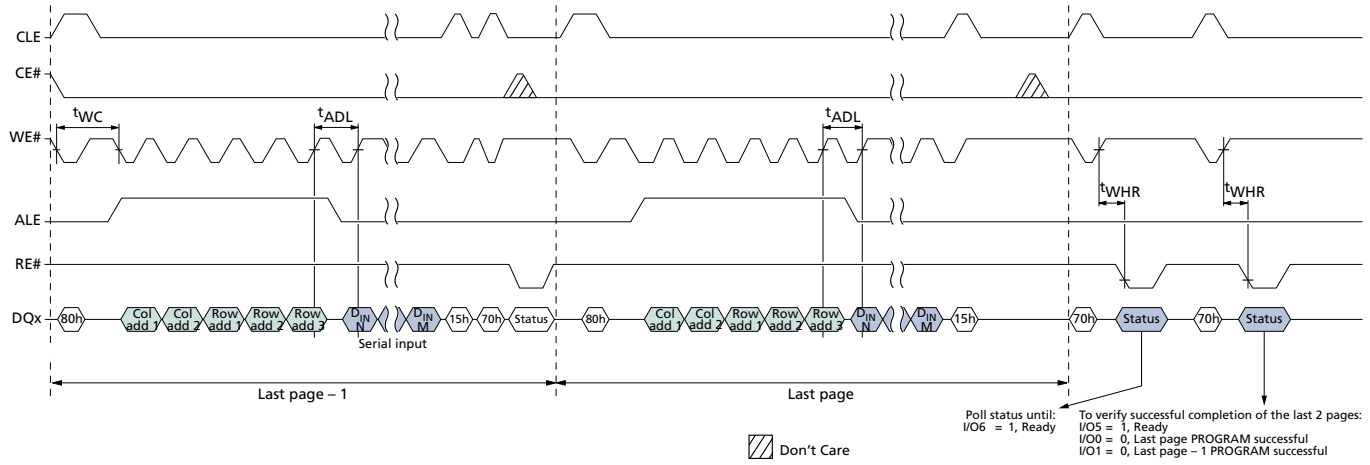


Figure 124: COPYBACK

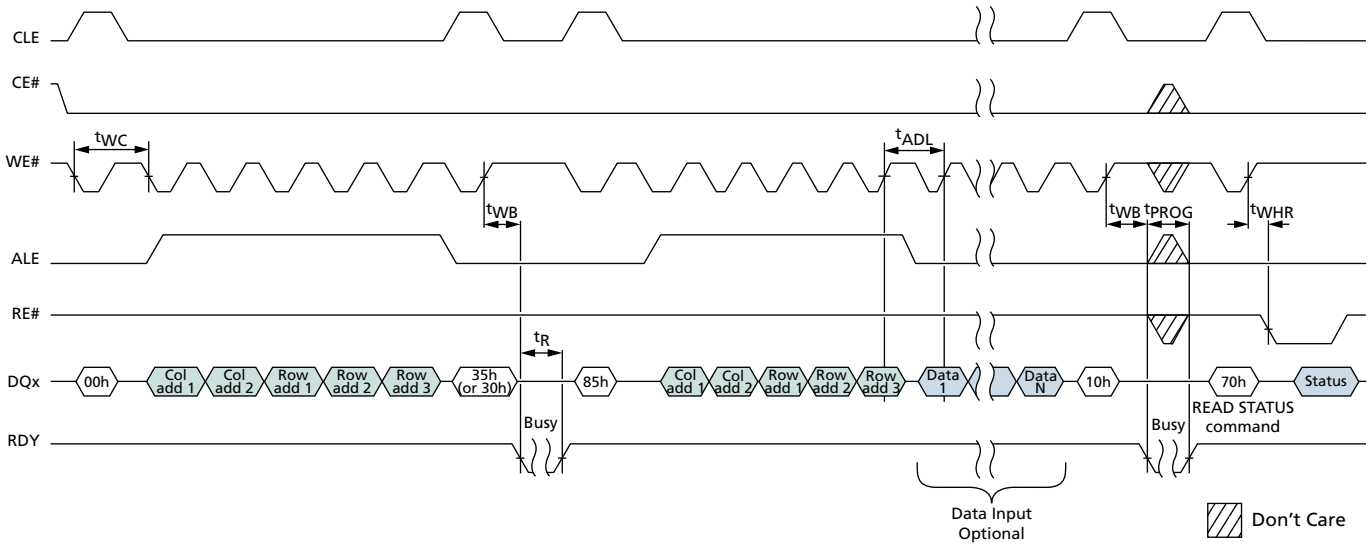
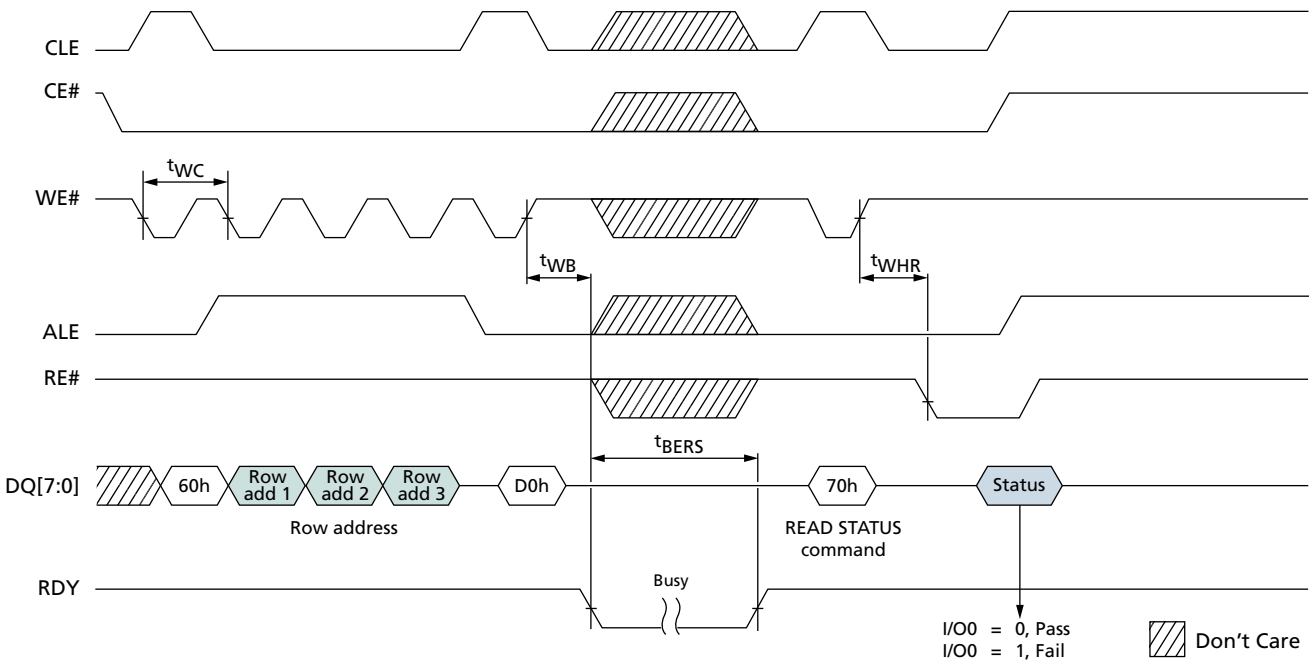
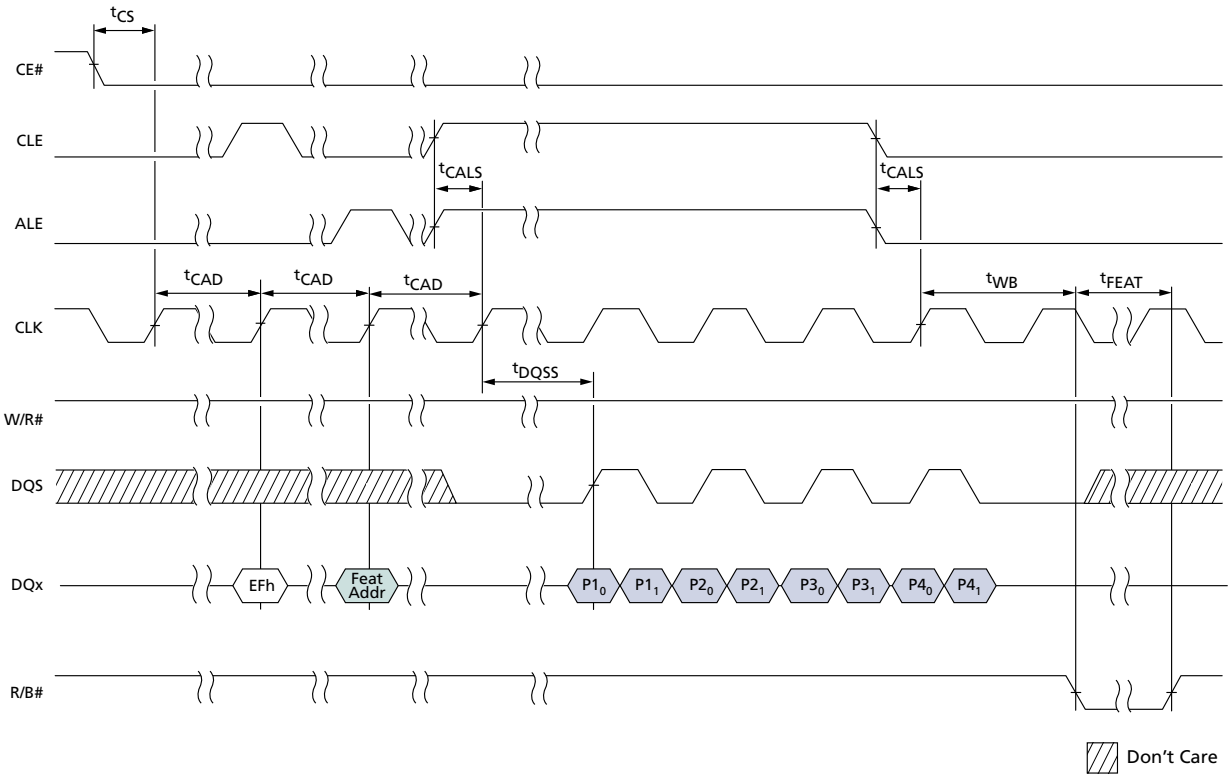


Figure 125: ERASE BLOCK Operation



NV-DDR Interface Timing Diagrams

Figure 126: SET FEATURES Operation



Notes:
1. When CE# remains LOW, tCAD begins at the rising edge of the clock from which the last data byte is input for the subsequent command or data input cycle(s).
2. tDSH (MIN) generally occurs during tDQSS (MIN).
3. tDSS (MIN) generally occurs during tDQSS (MAX).
4. The cycle that tCAD is measured from may be an idle cycle (as shown), another command cycle, an address cycle, or a data cycle. The idle cycle is shown in this diagram for simplicity.

Figure 127: READ ID Operation

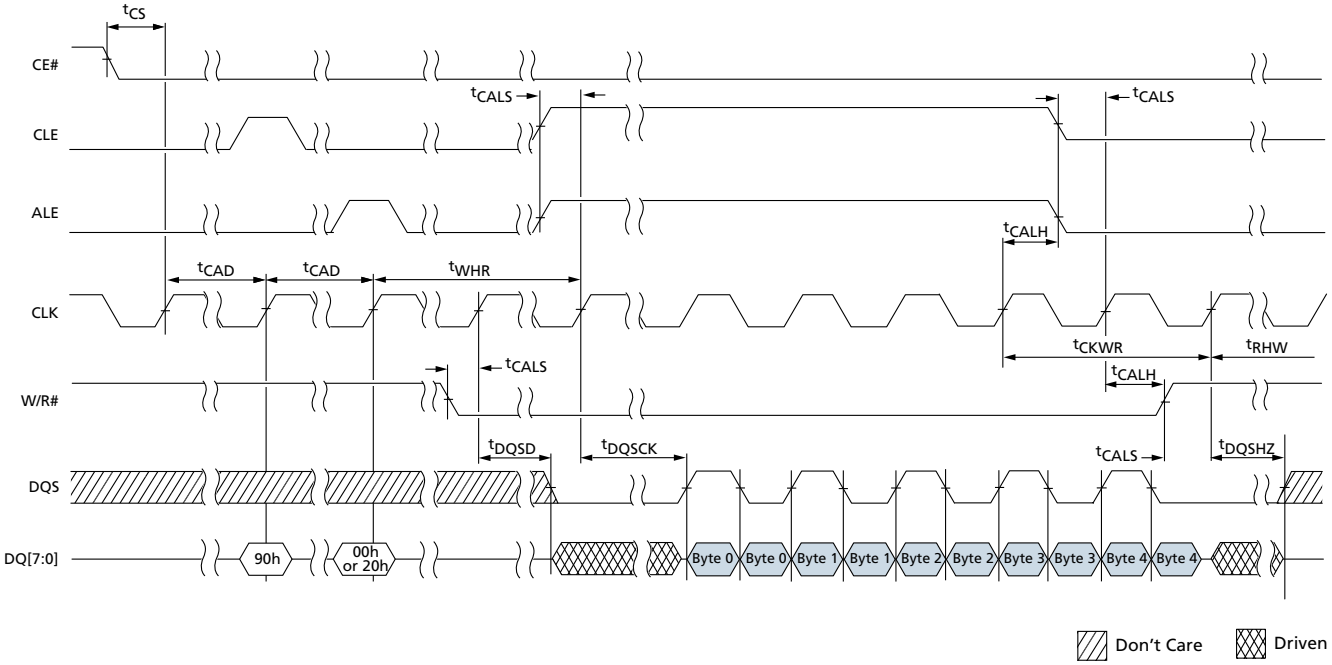


Figure 128: GET FEATURES Operation

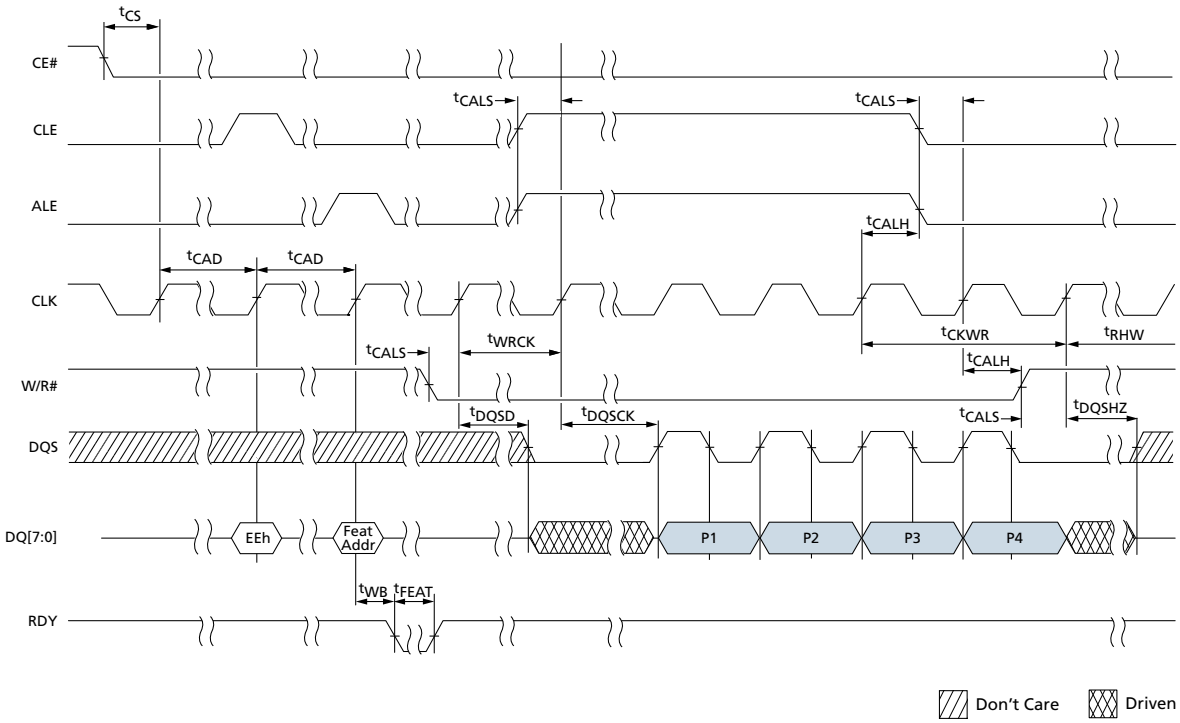


Figure 129: RESET (FCh) Operation

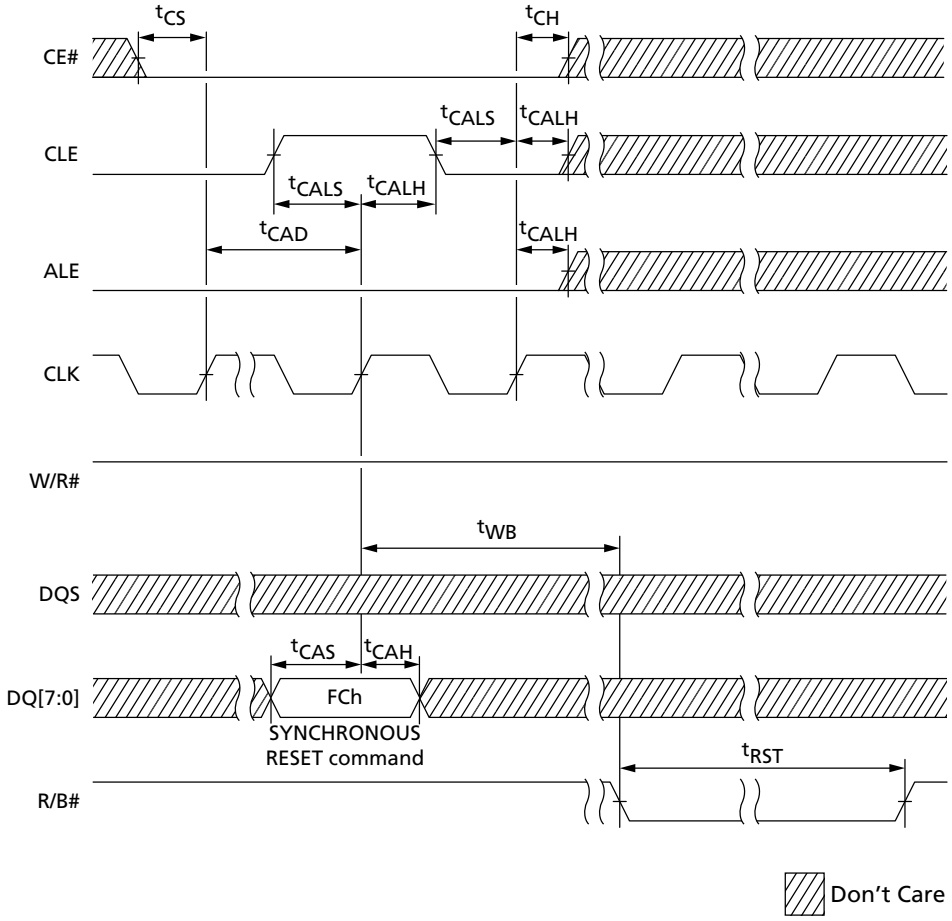


Figure 130: READ STATUS Cycle

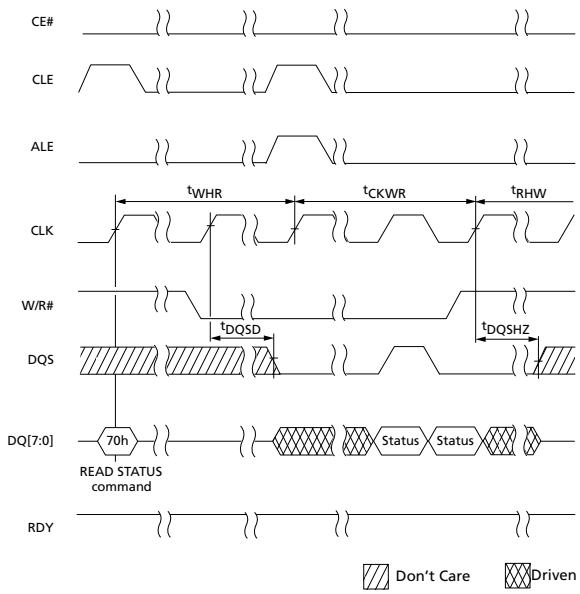


Figure 131: READ STATUS ENHANCED Operation

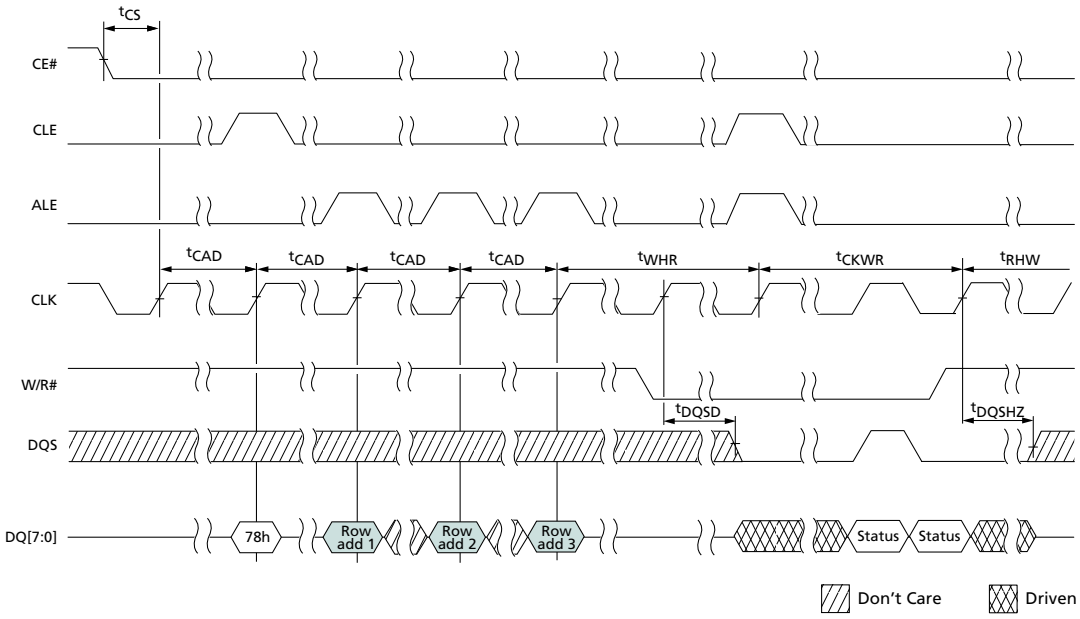


Figure 132: READ PARAMETER PAGE Operation

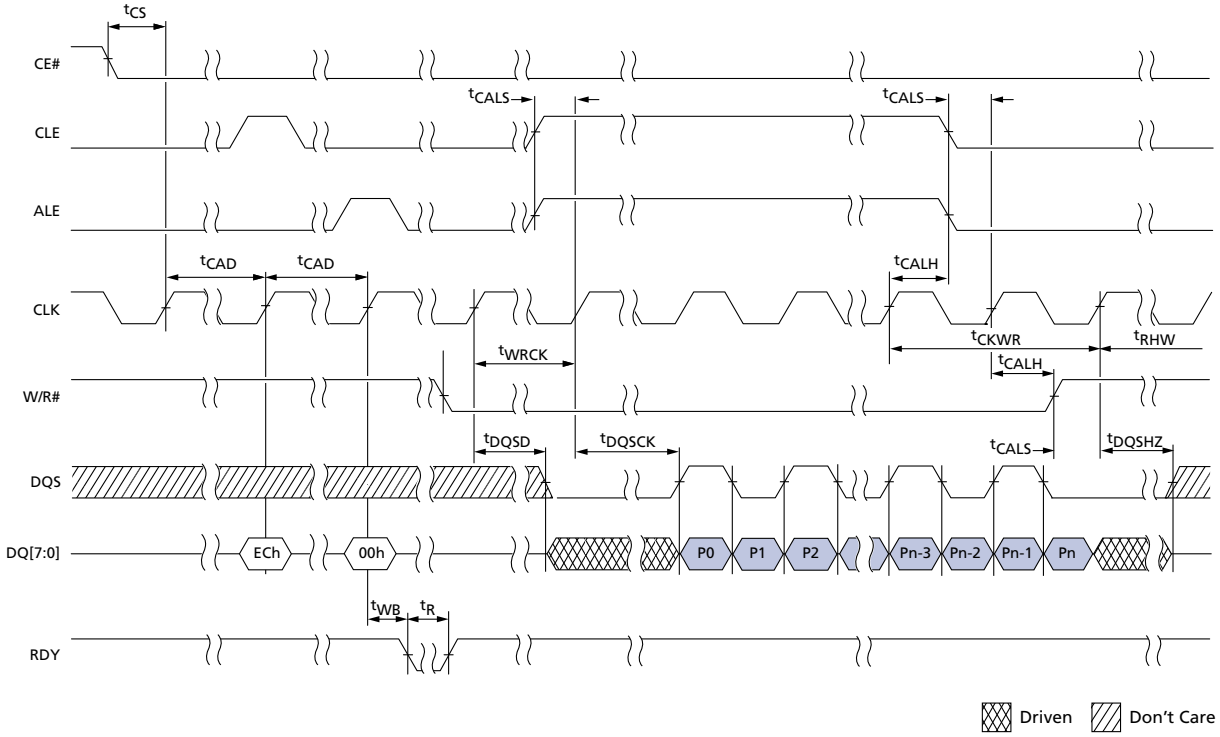


Figure 133: READ PAGE Operation

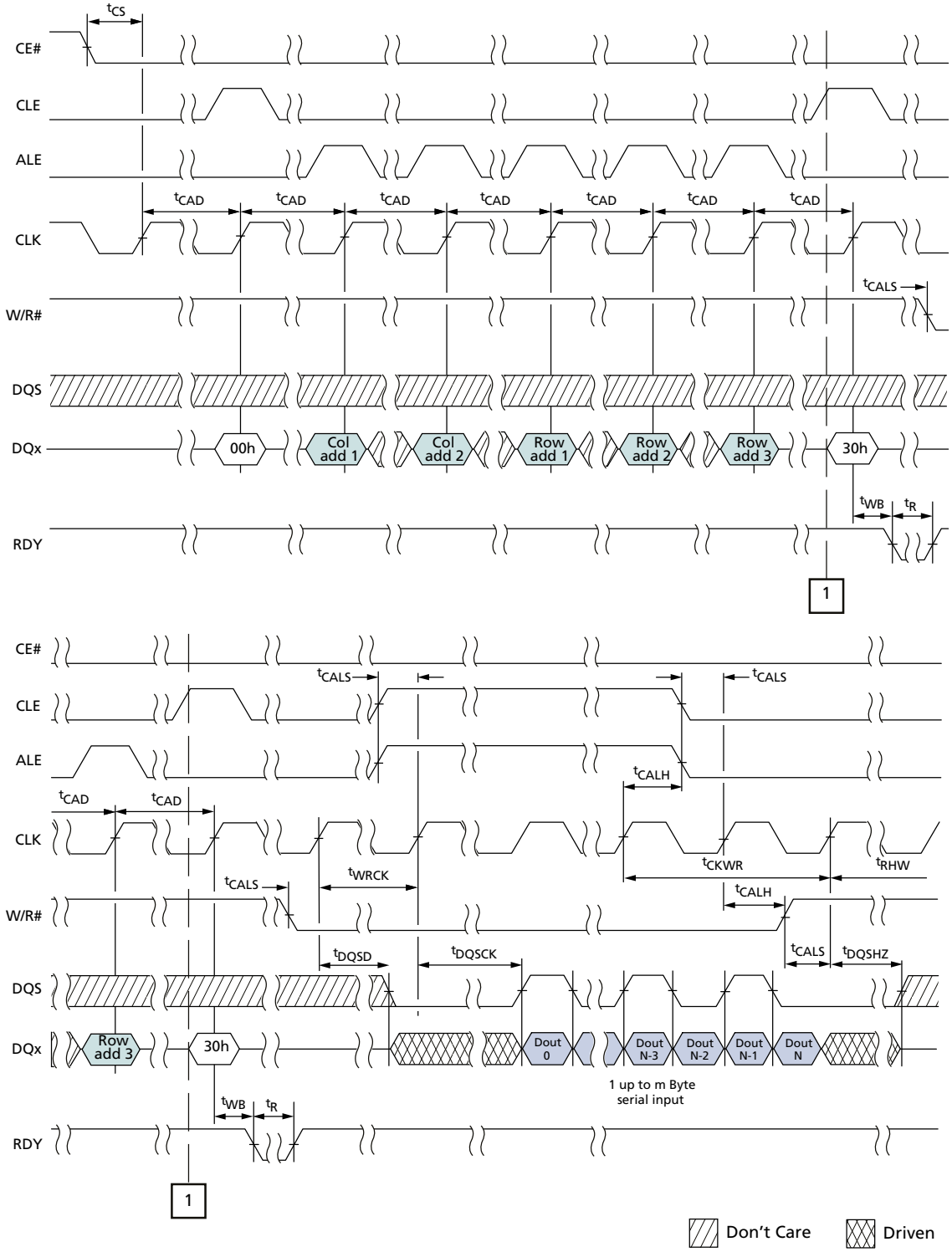


Figure 134: CHANGE READ COLUMN

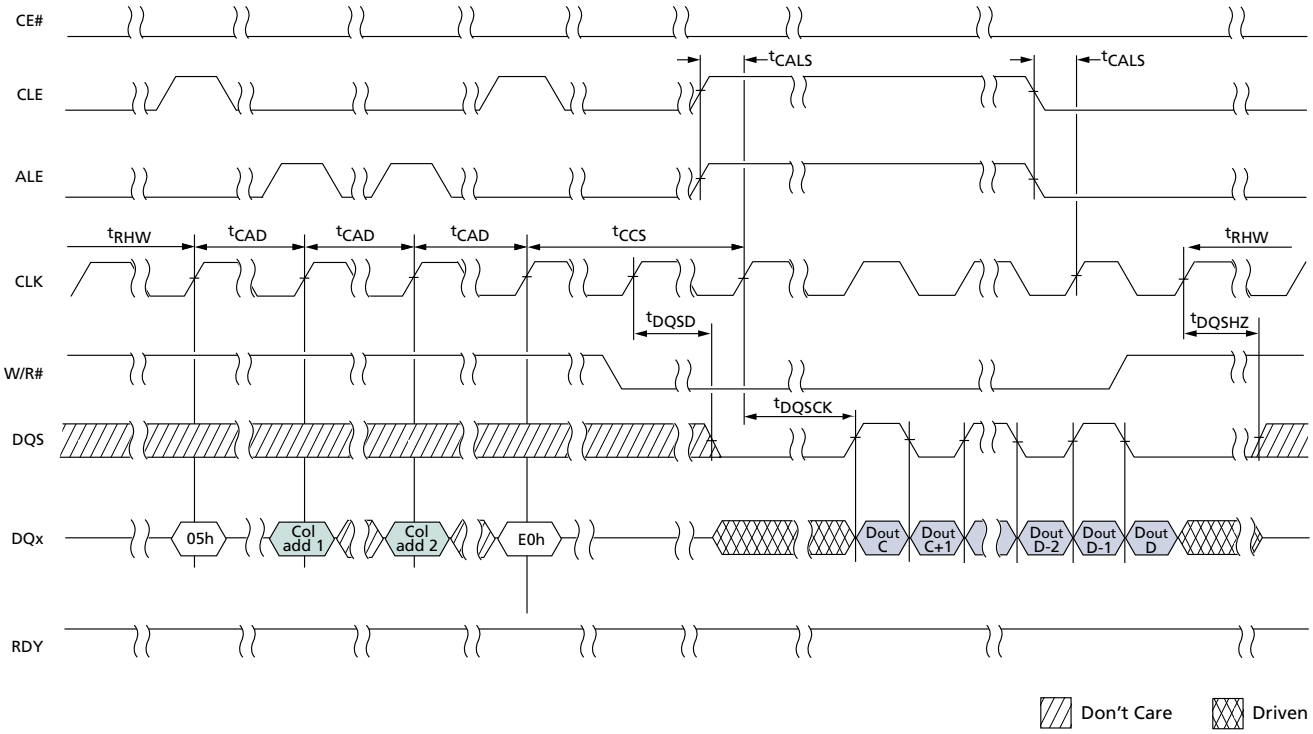


Figure 135: READ PAGE CACHE SEQUENTIAL (1 of 2)

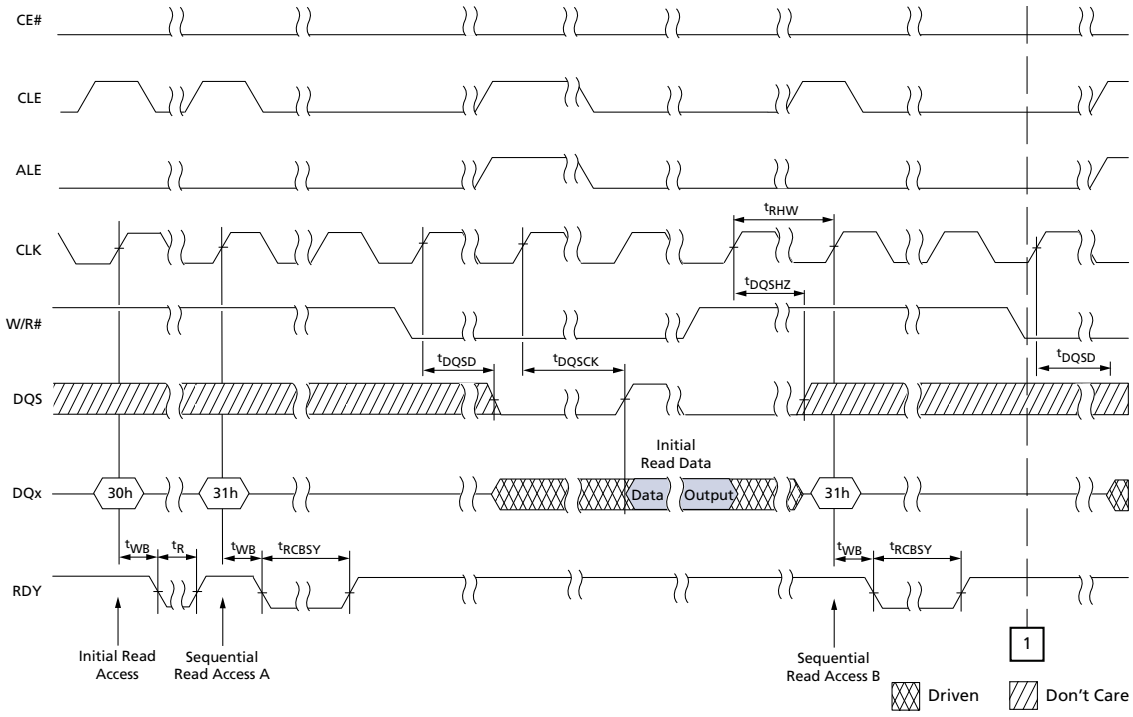


Figure 136: READ PAGE CACHE SEQUENTIAL (2 of 2)

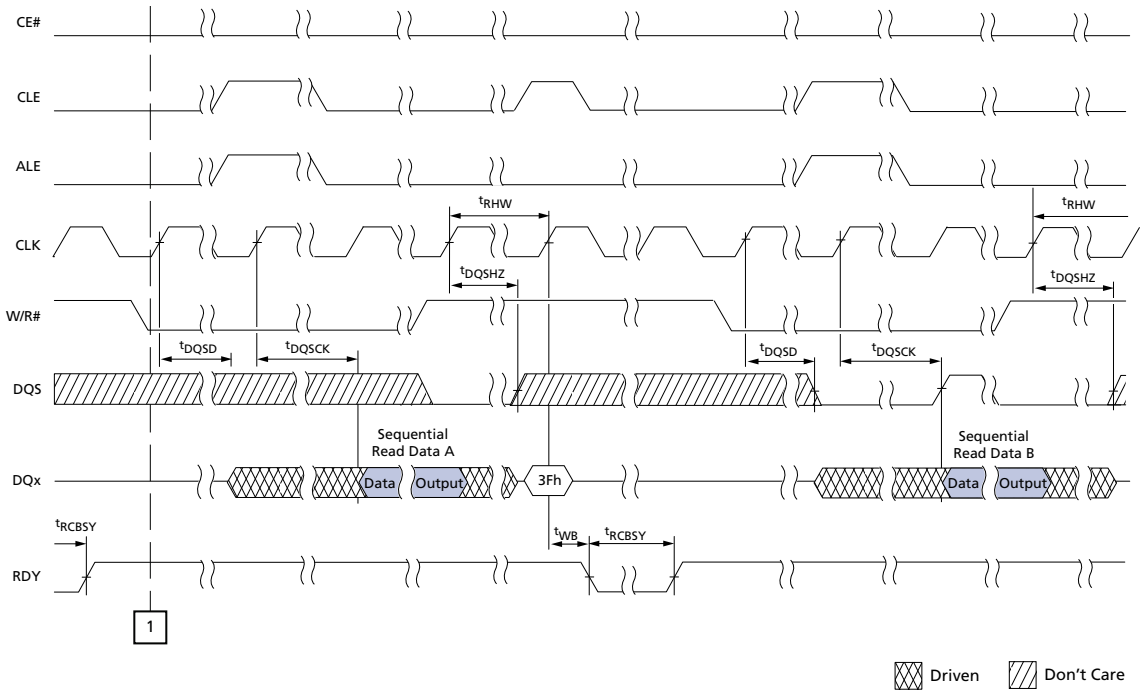


Figure 137: READ PAGE CACHE RANDOM (1 of 2)

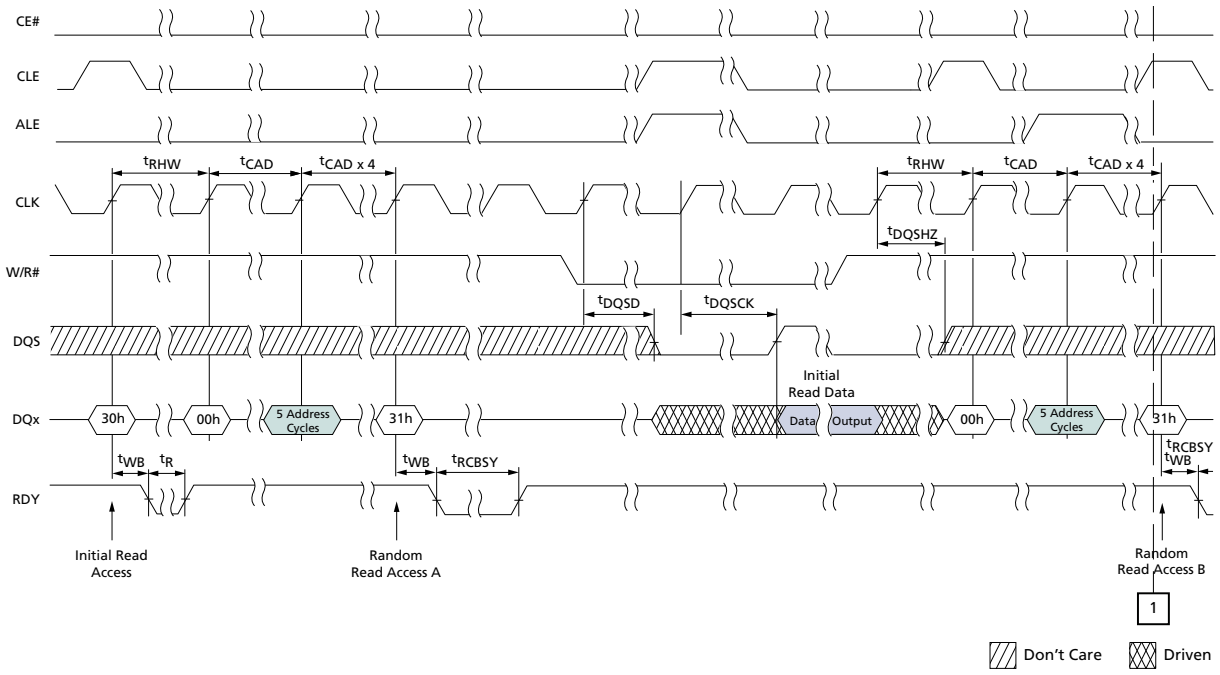


Figure 138: READ PAGE CACHE RANDOM (2 of 2)

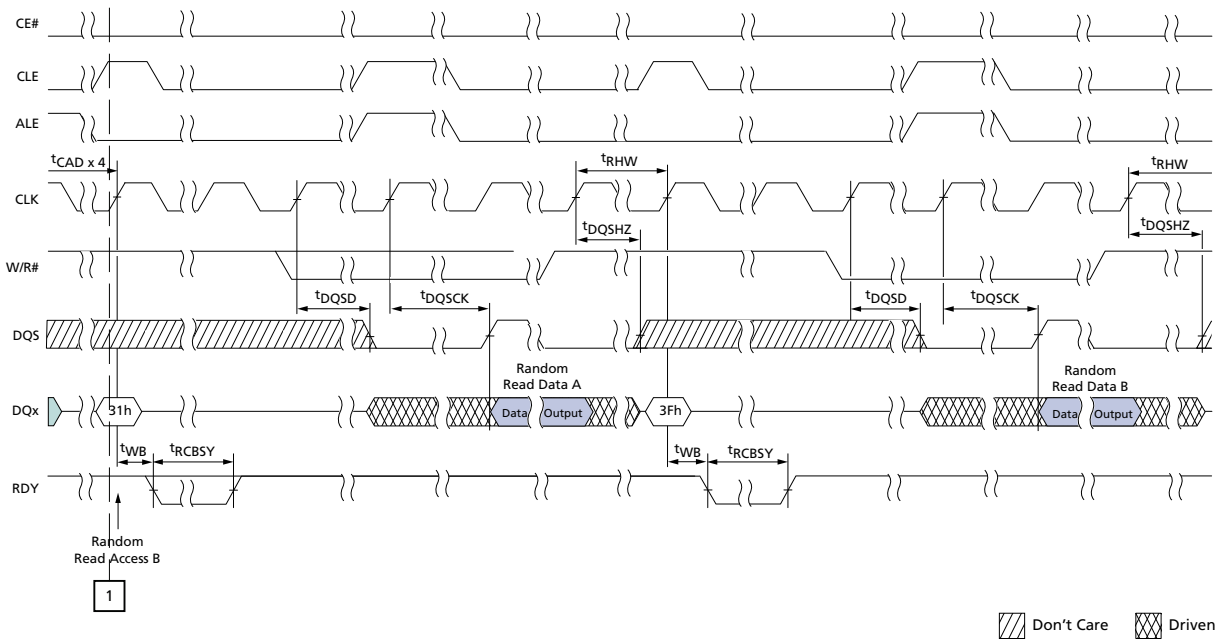


Figure 139: Multi-Plane Read Page (1 of 2)

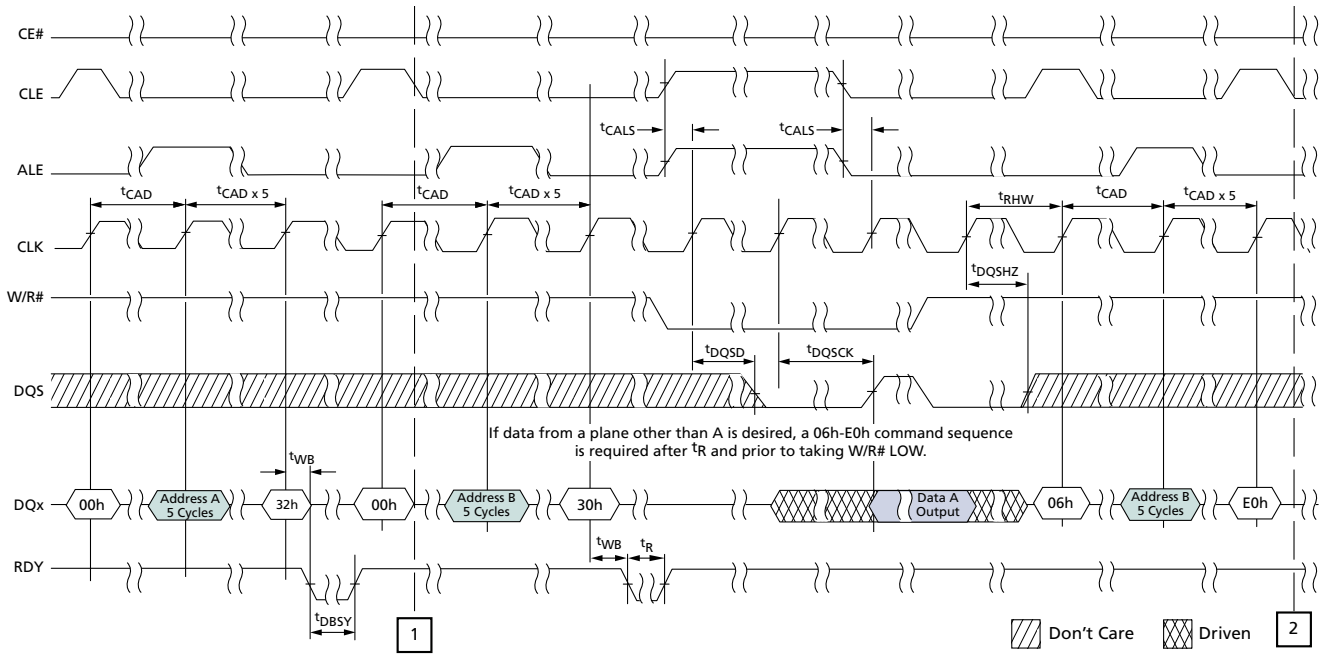


Figure 140: Multi-Plane Read Page (2 of 2)

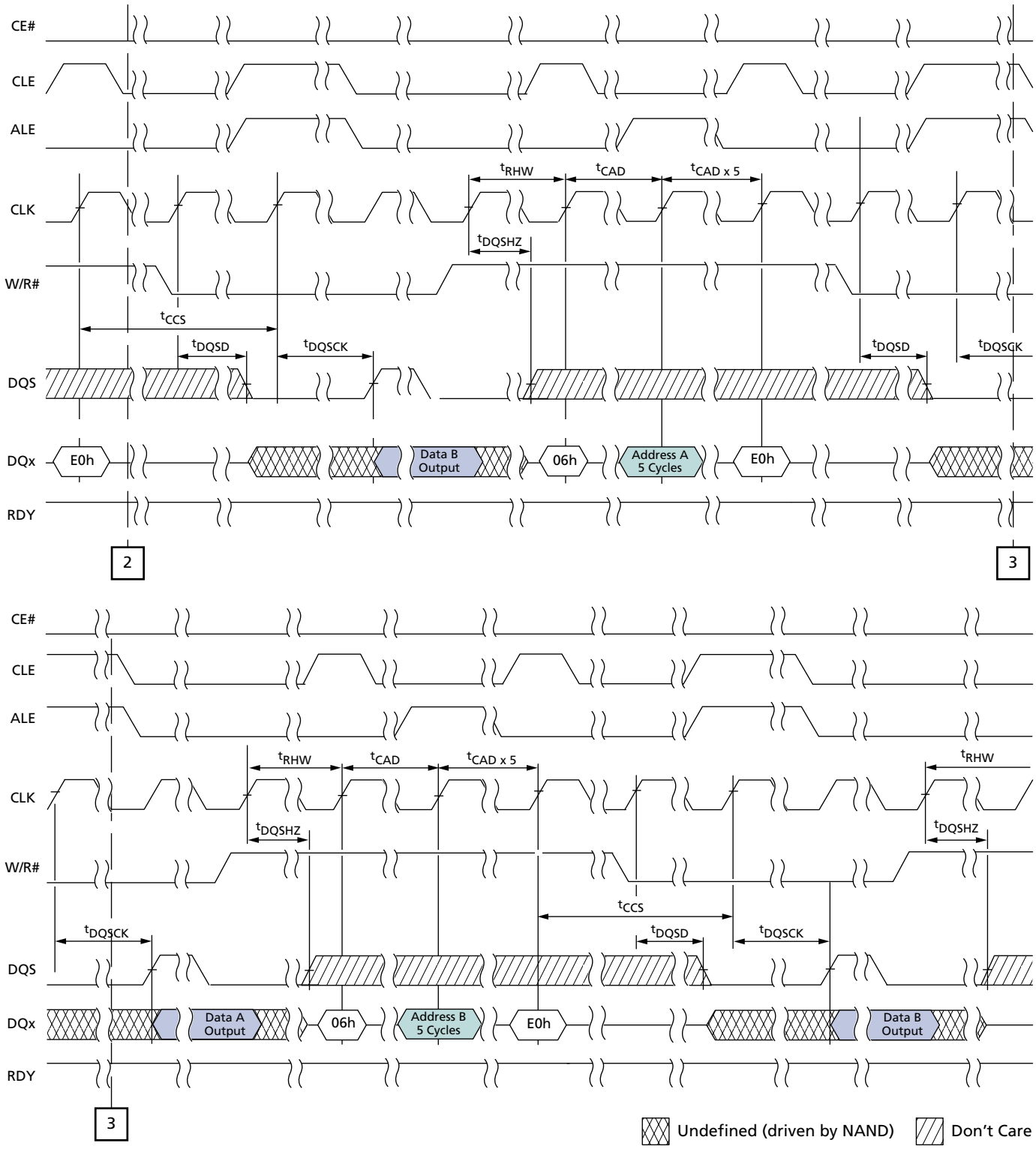


Figure 141: PROGRAM PAGE Operation (1 of 2)

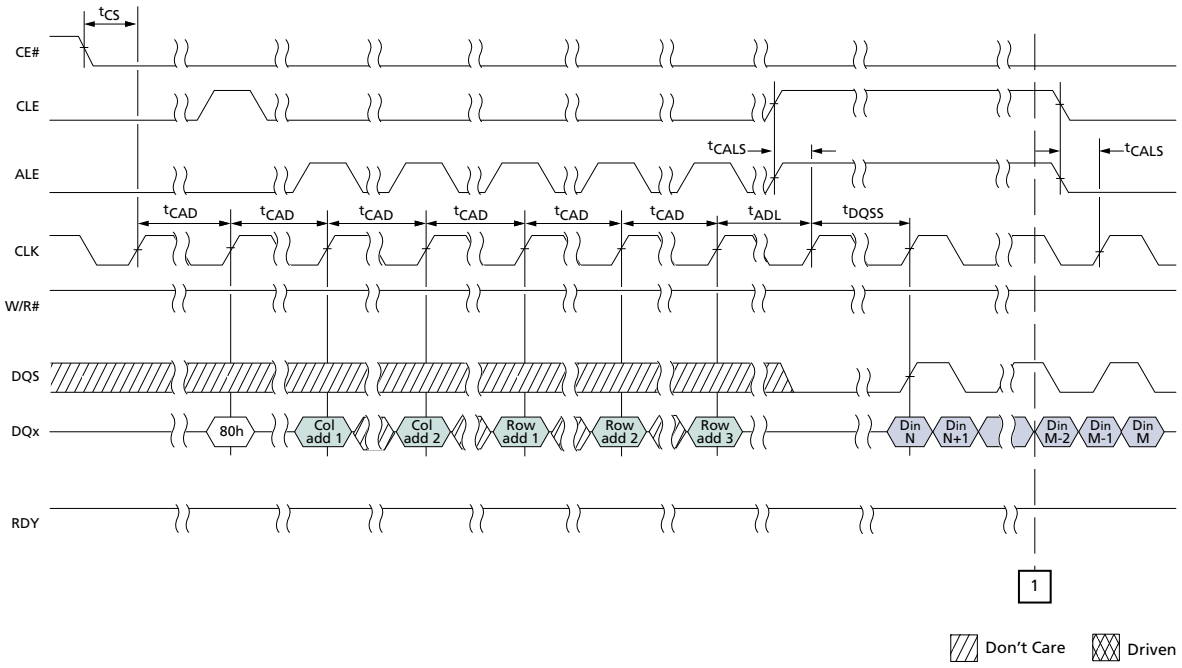


Figure 142: PROGRAM PAGE Operation (2 of 2)

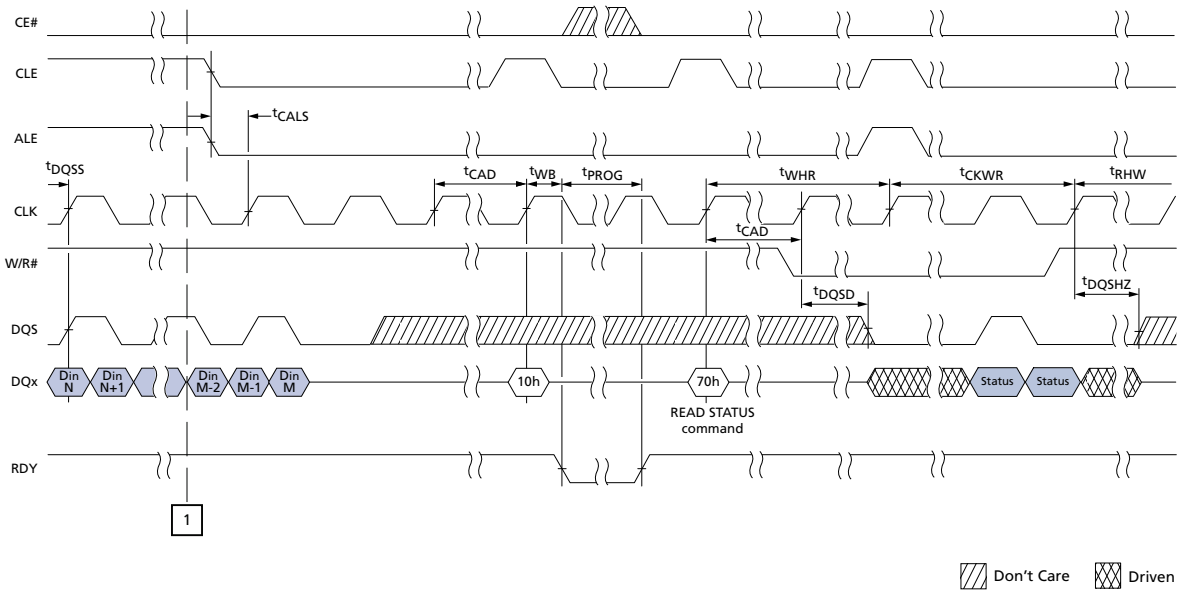


Figure 143: CHANGE WRITE COLUMN

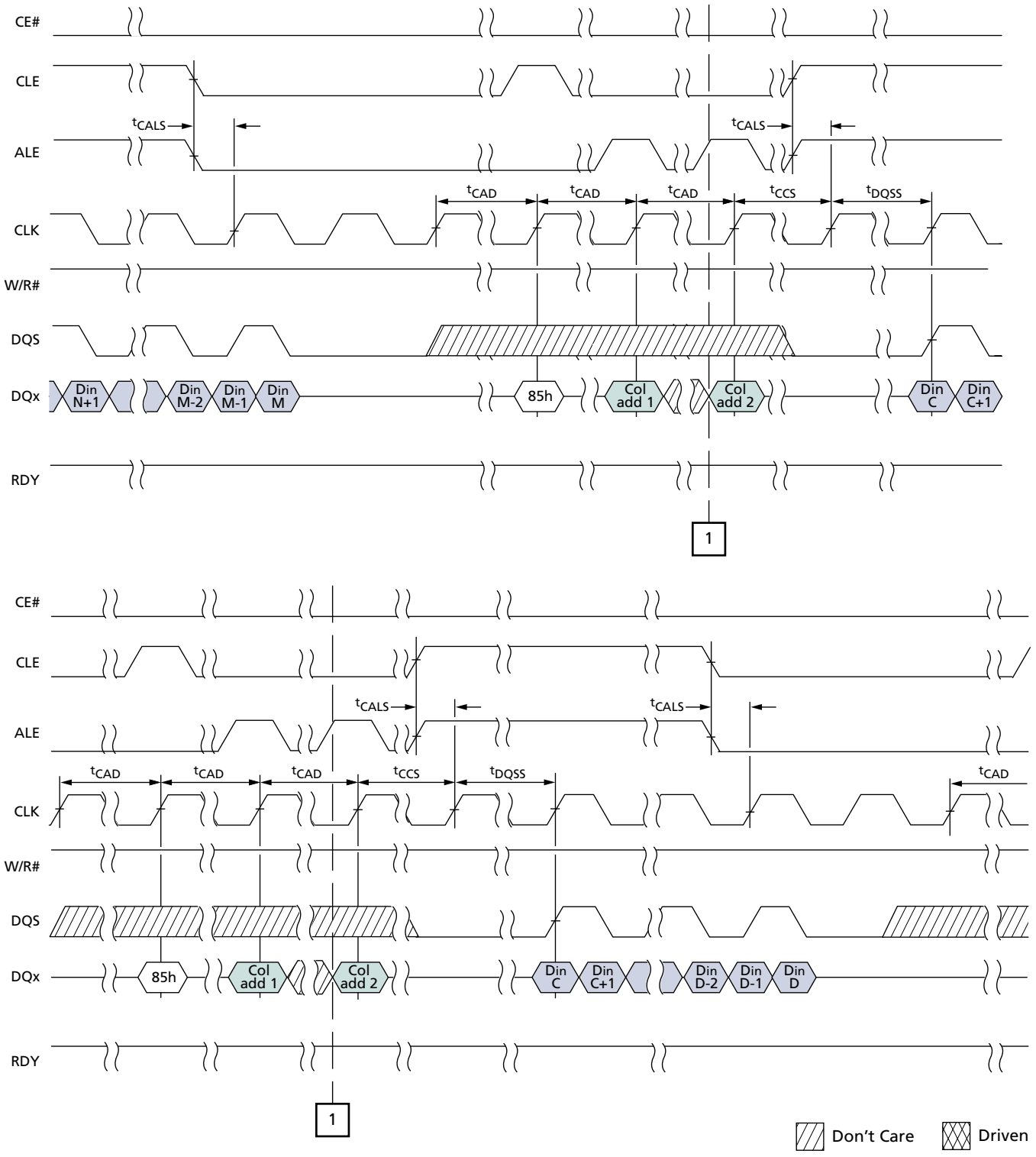


Figure 144: Multi-Plane Program Page

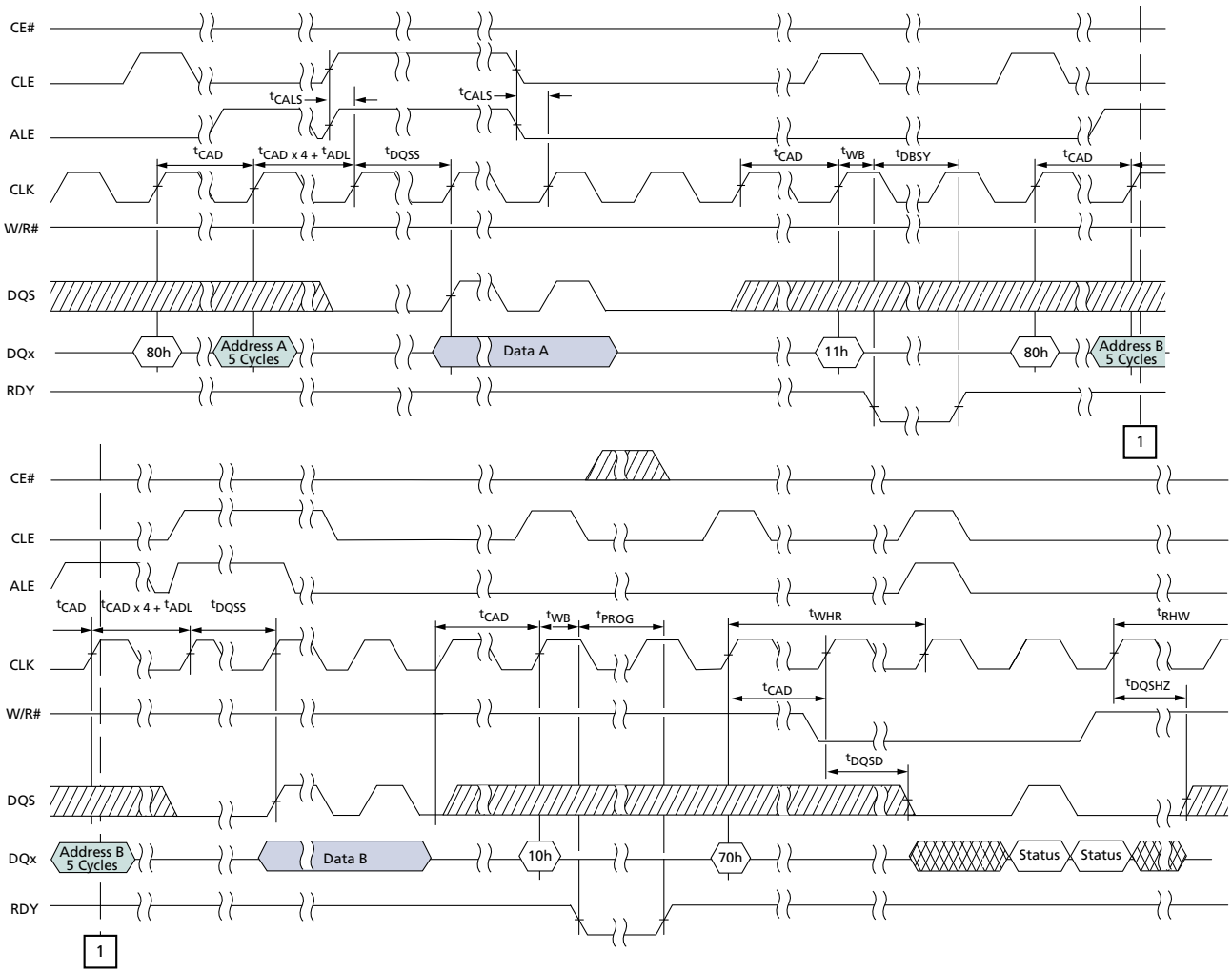


Figure 145: ERASE BLOCK

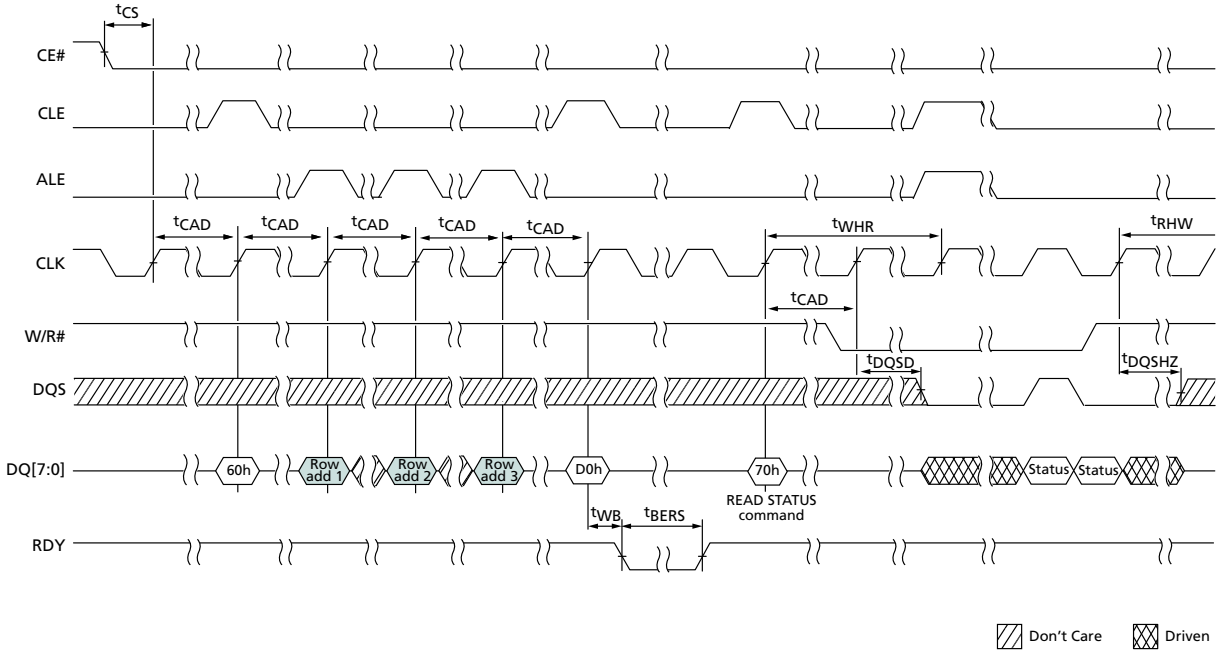


Figure 146: COPYBACK (1 of 3)

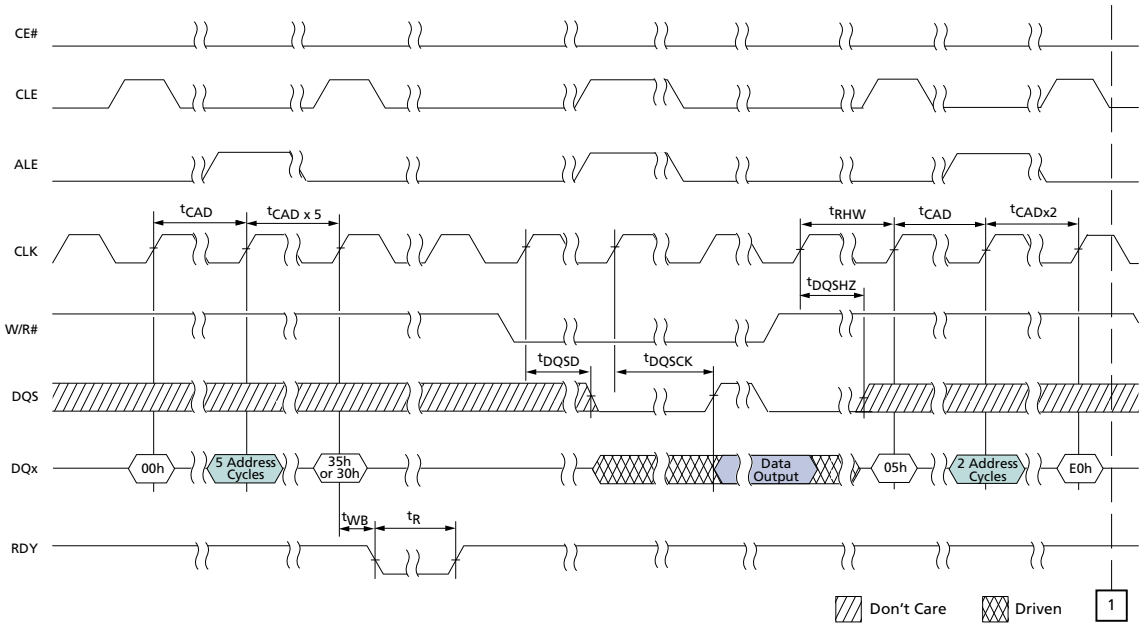


Figure 147: COPYBACK (2 of 3)

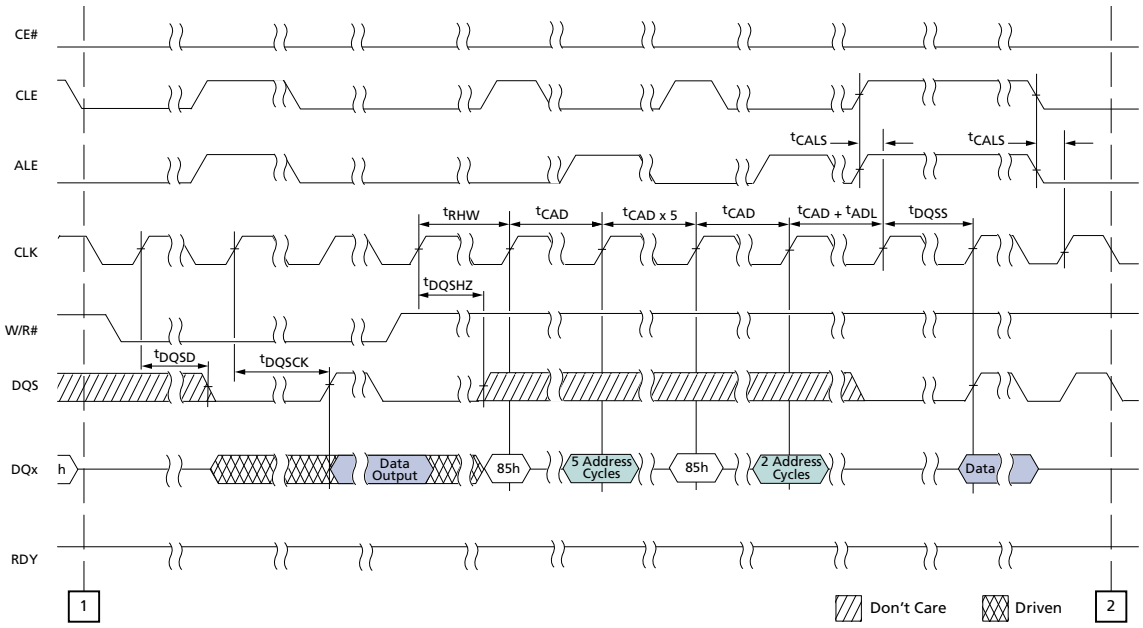


Figure 148: COPYBACK (3 of 3)

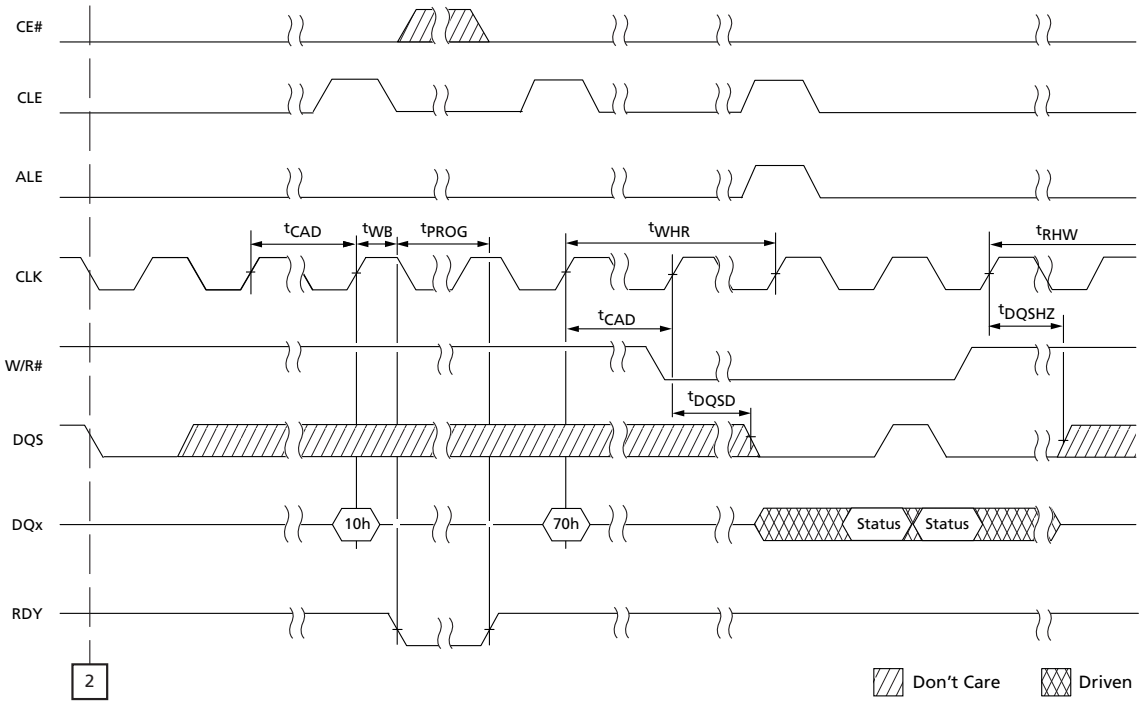


Figure 149: READ OTP PAGE

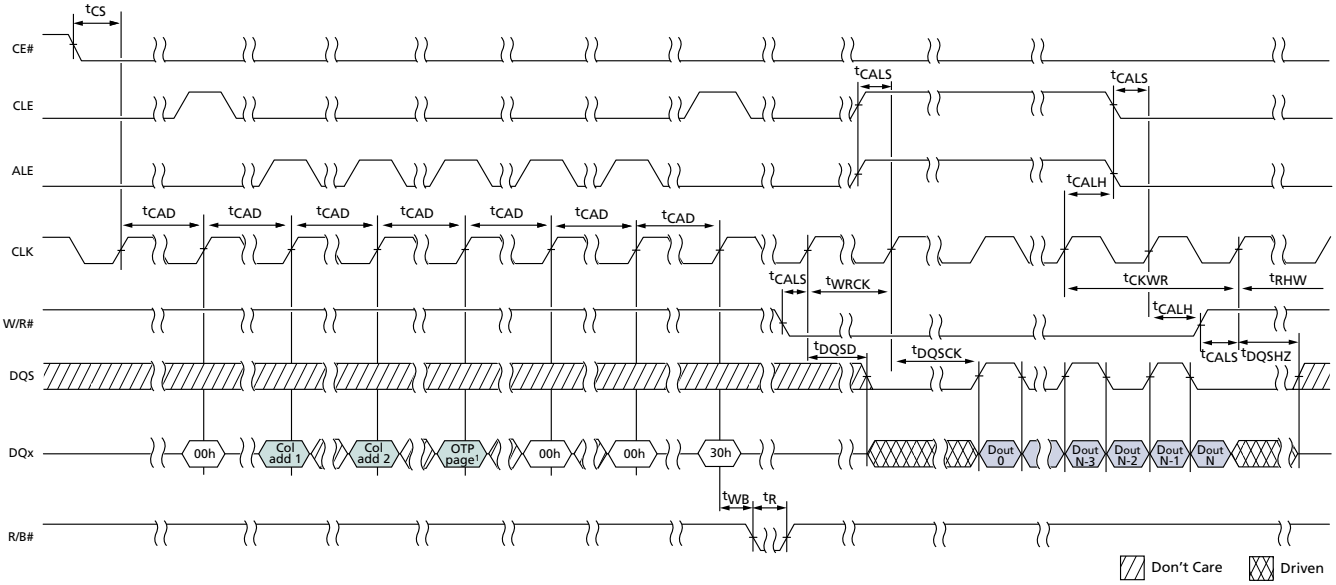


Figure 150: PROGRAM OTP PAGE (1 of 2)

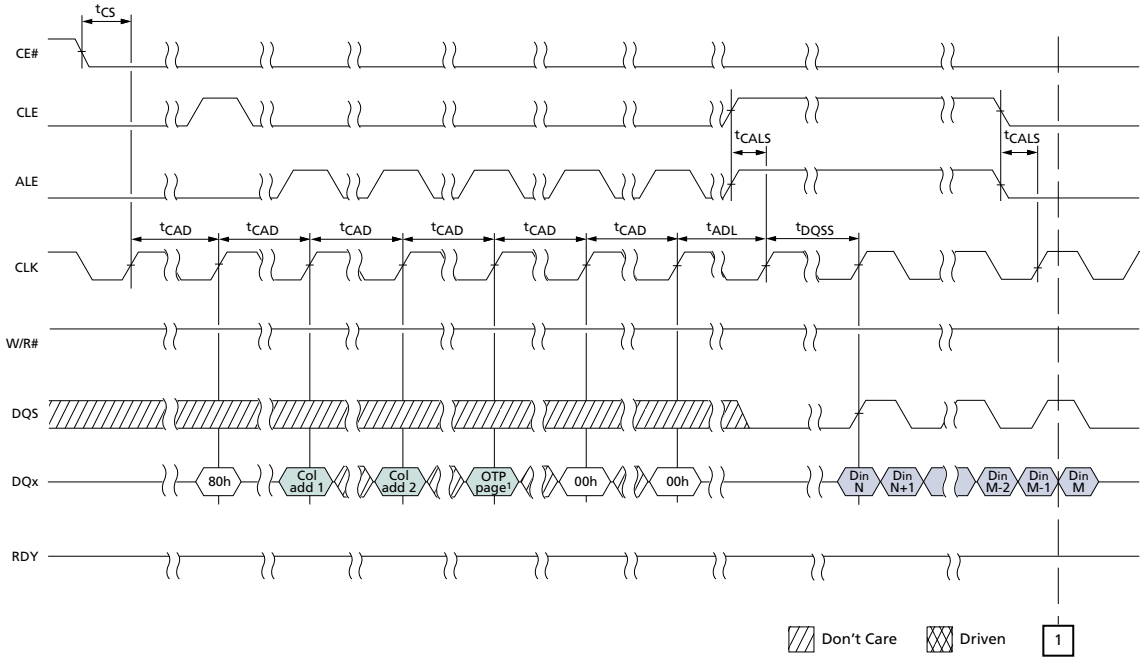


Figure 151: PROGRAM OTP PAGE (2 of 2)

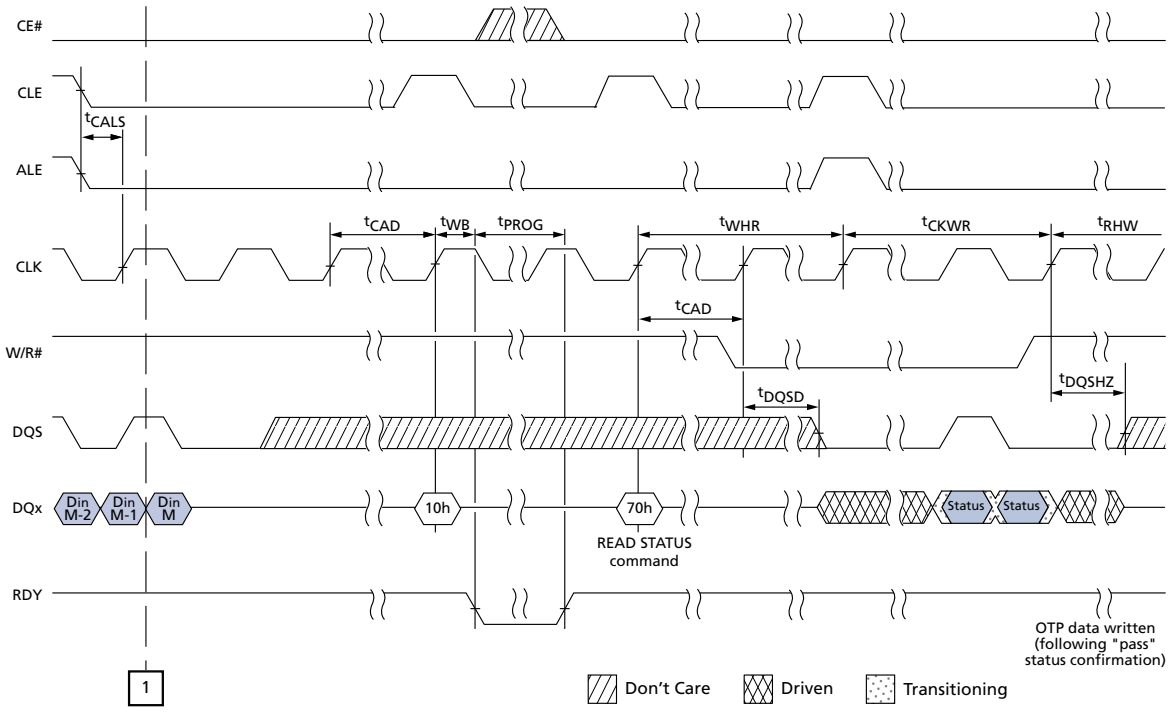
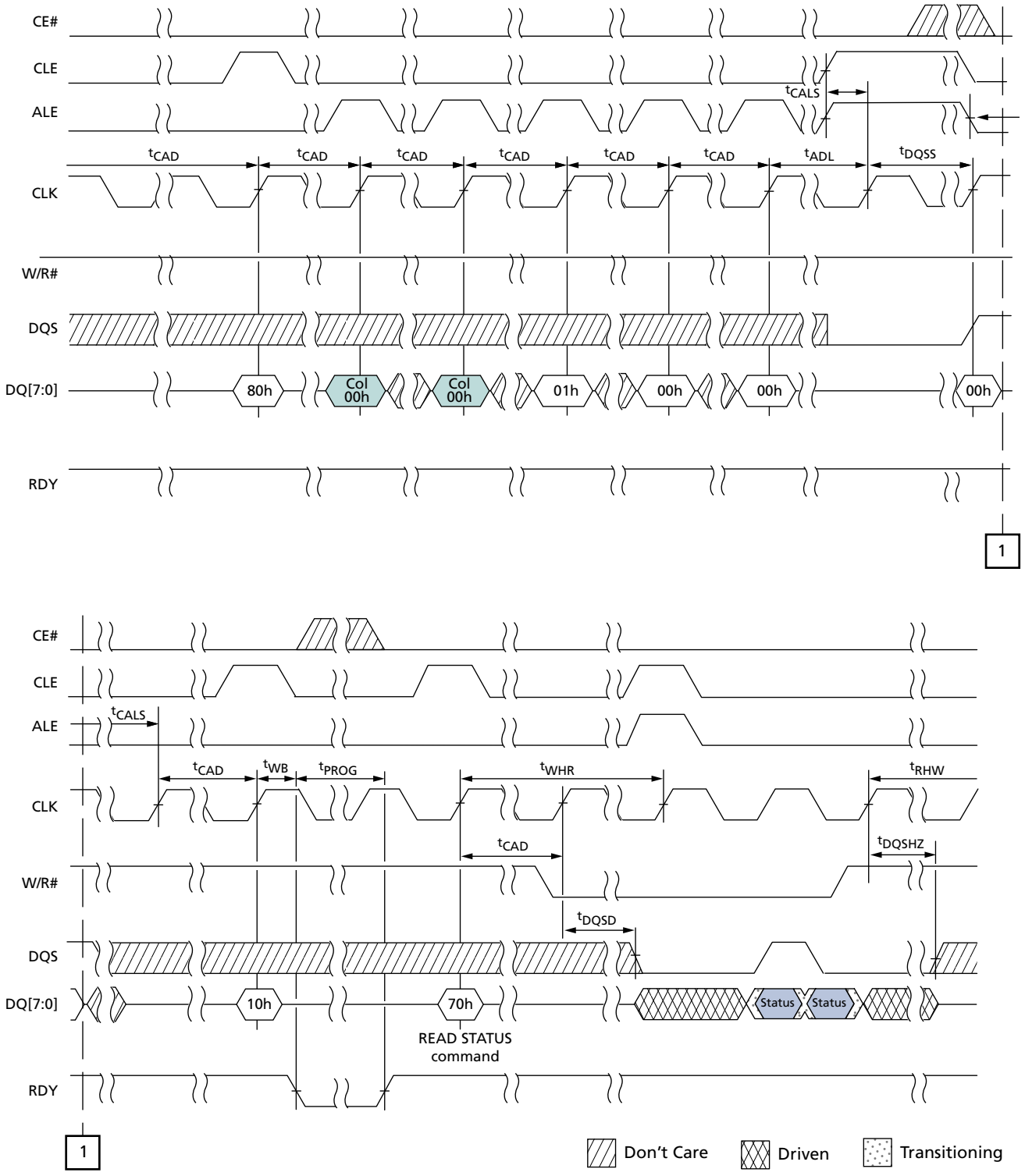
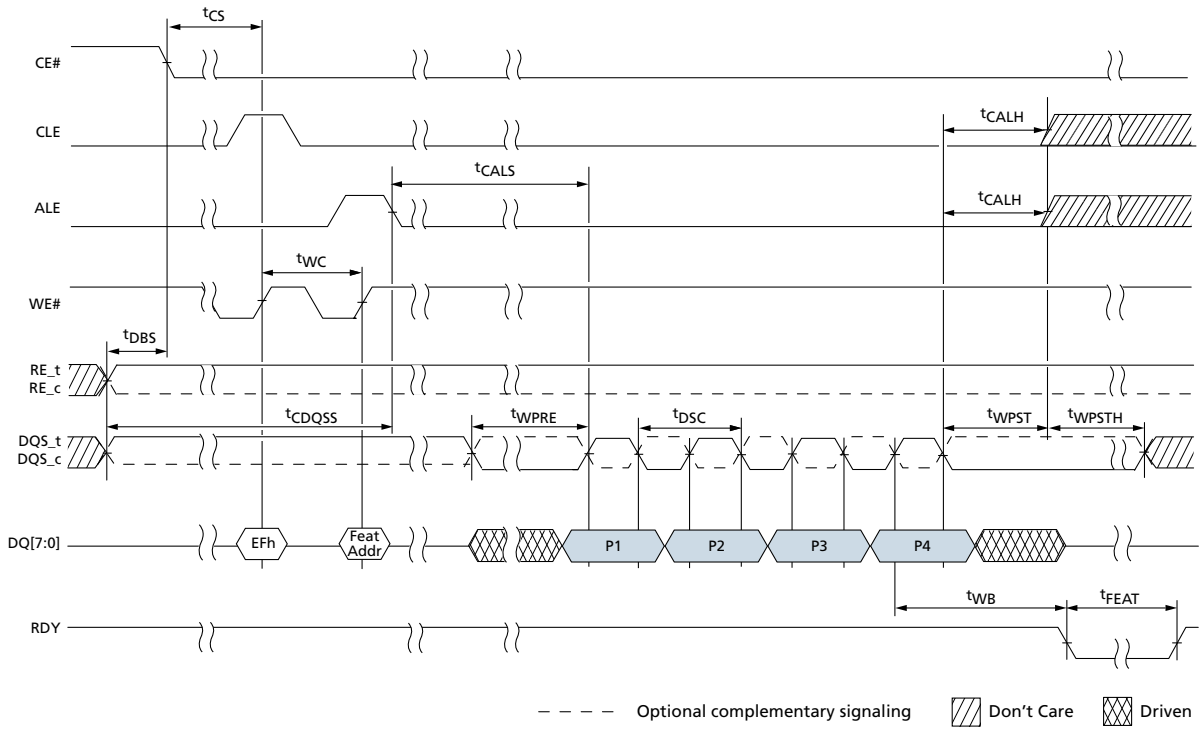


Figure 152: PROTECT OTP AREA



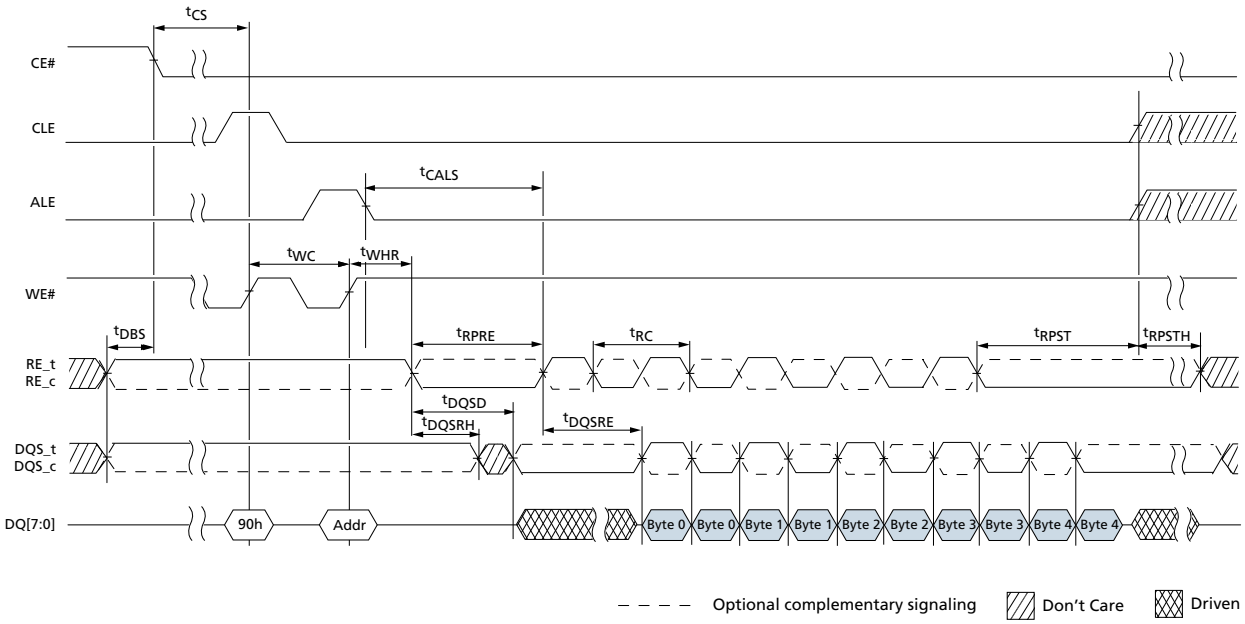
NV-DDR2 and NV-DDR3 Interface Timing Diagrams

Figure 153: SET FEATURES Operation



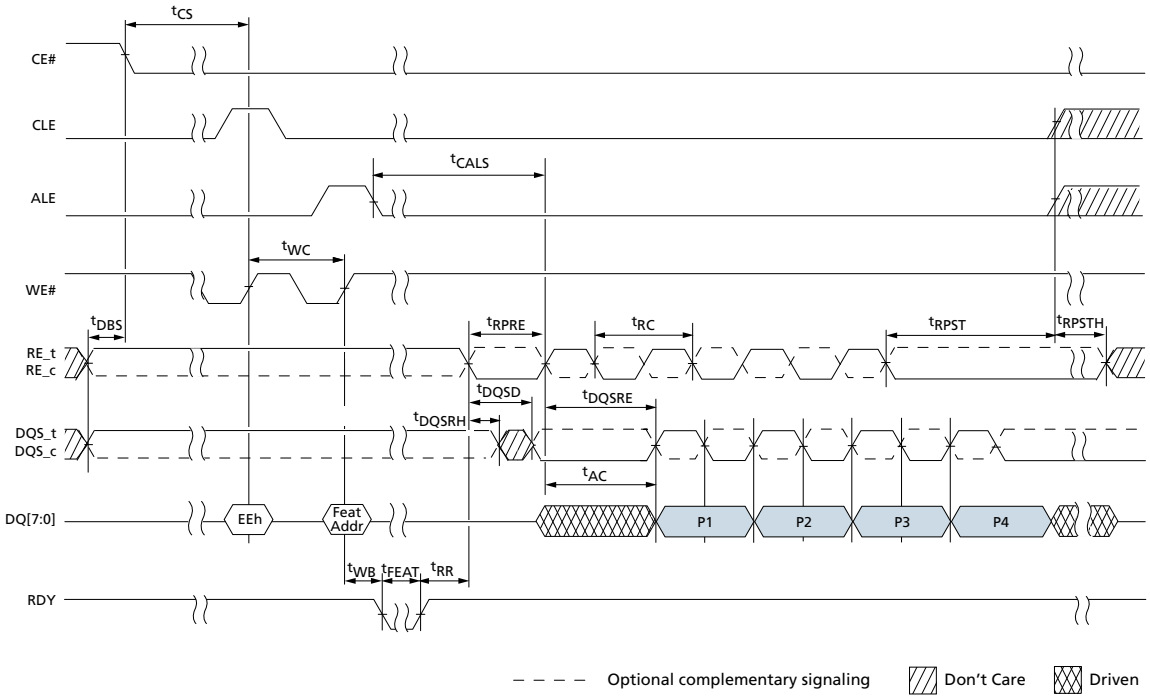
Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 154: READ ID Operation



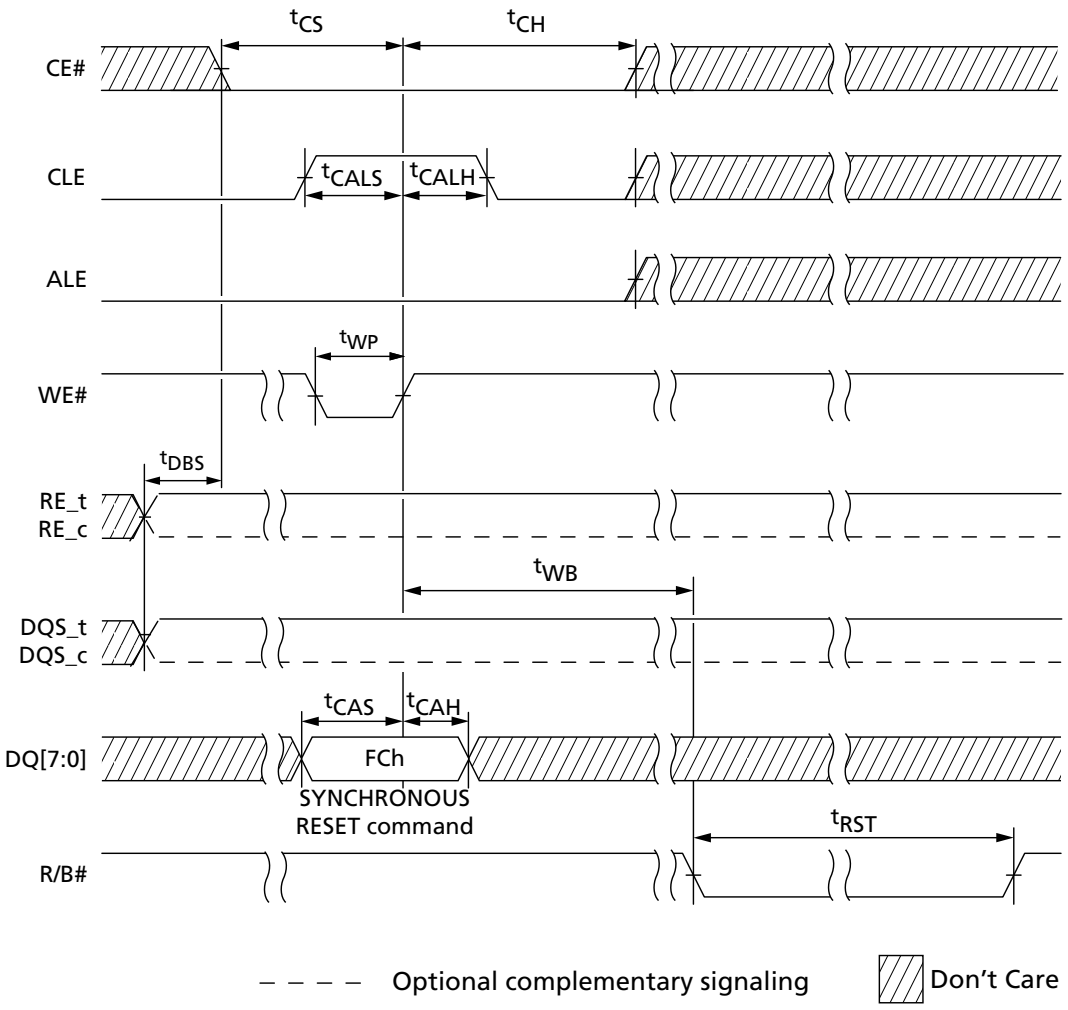
Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 155: GET FEATURES Operation



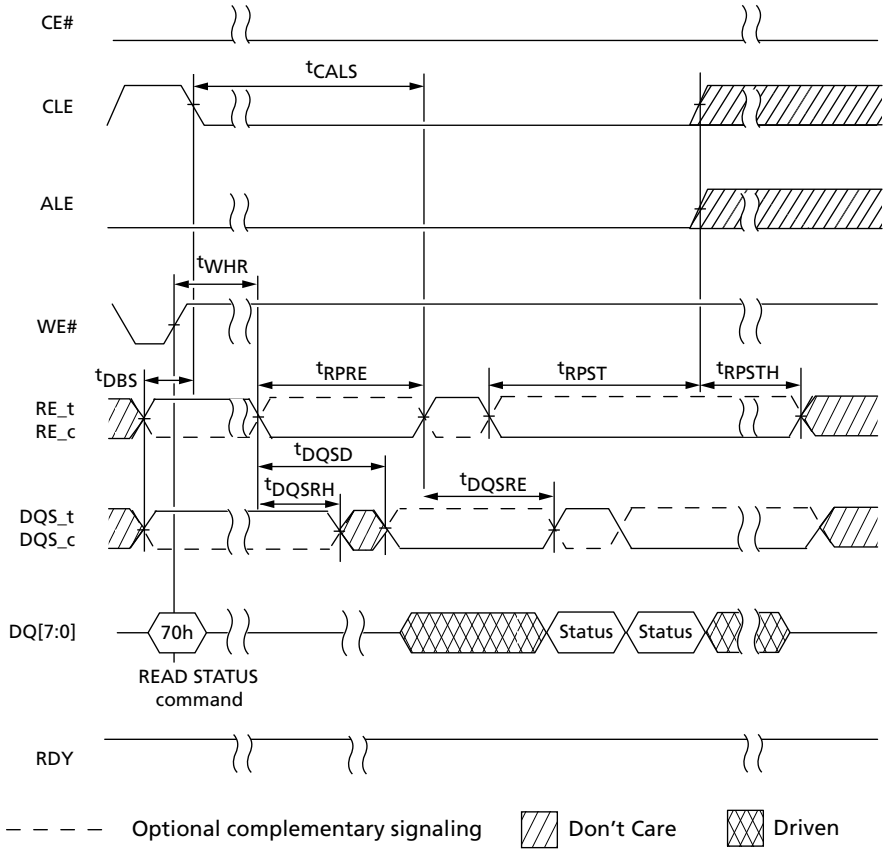
Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 156: RESET (FCh) Operation



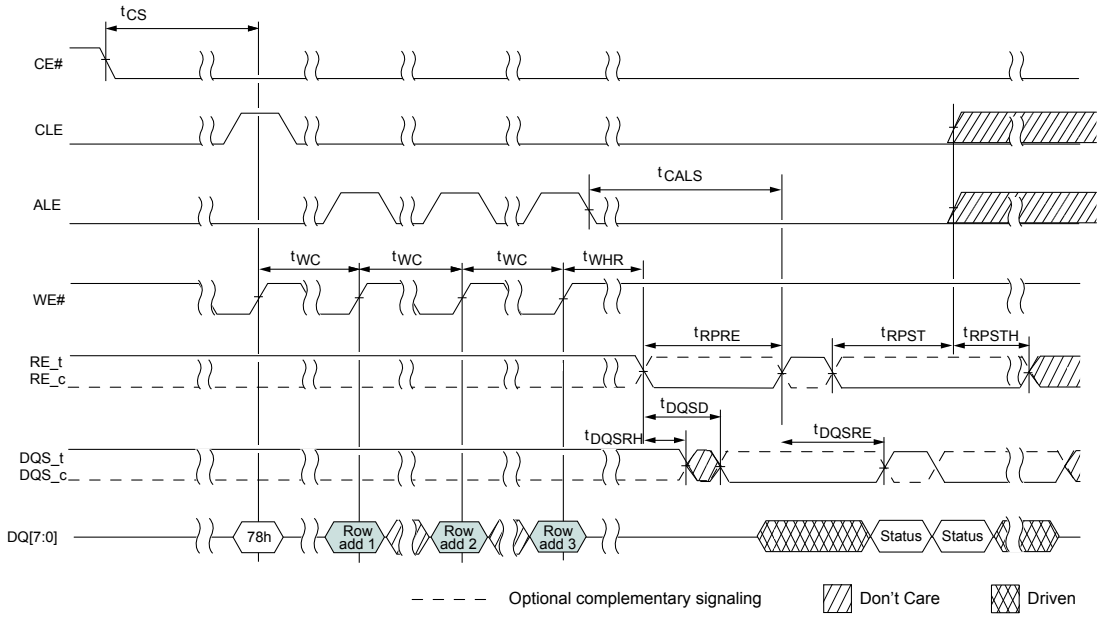
Note: 1. DQS is "don't care" during active command cycle (CLE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 157: READ STATUS Cycle



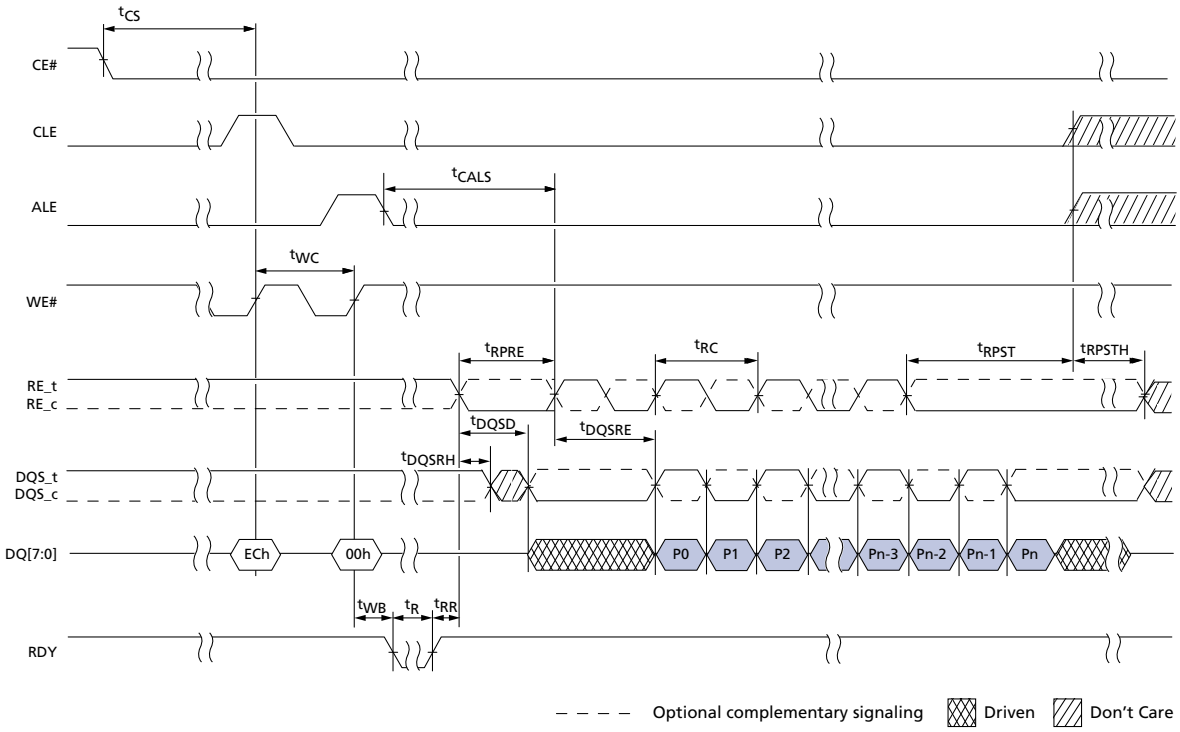
Note: 1. DQS is "don't care" during active command cycle (CLE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 158: READ STATUS ENHANCED Operation



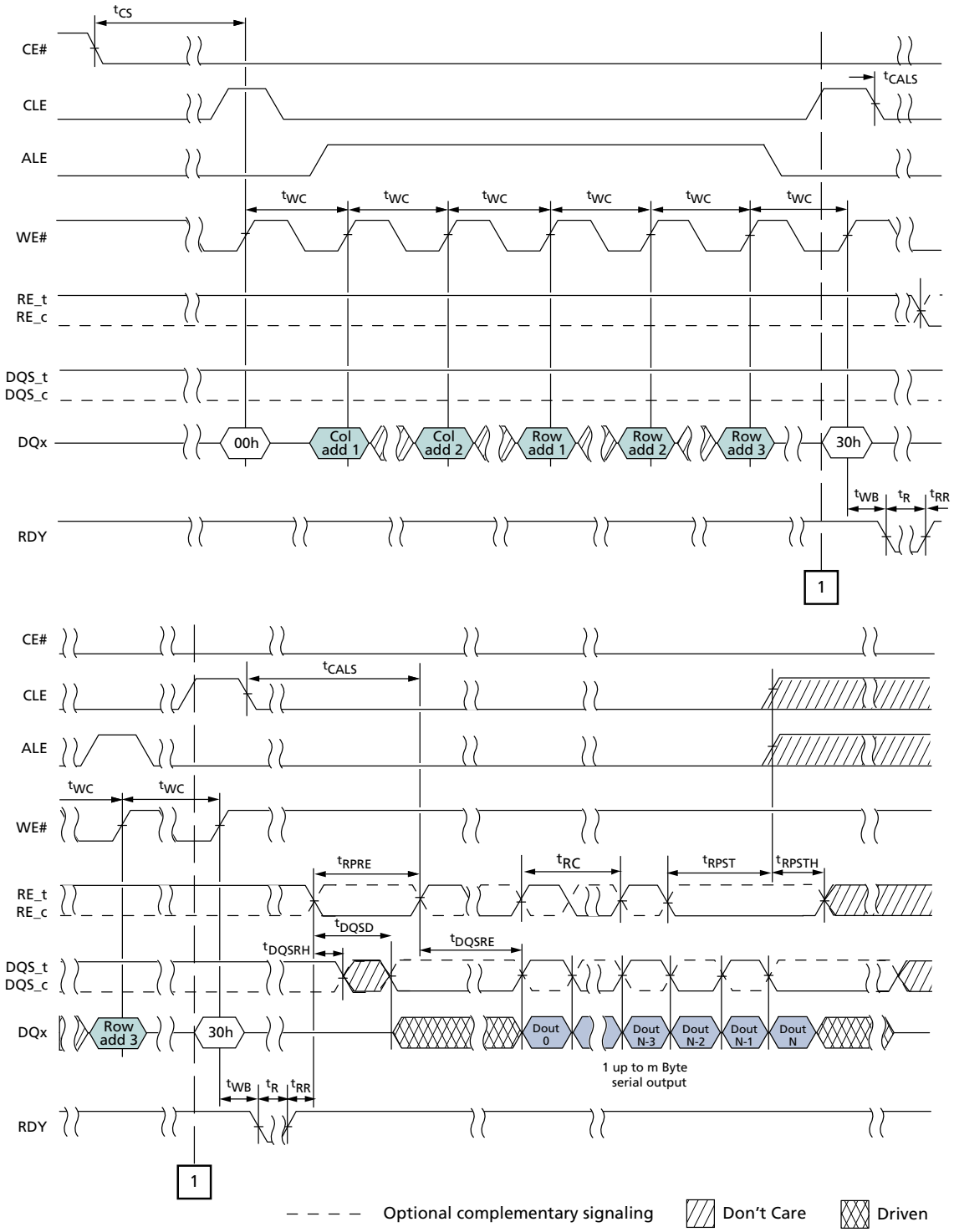
Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 159: READ PARAMETER PAGE Operation



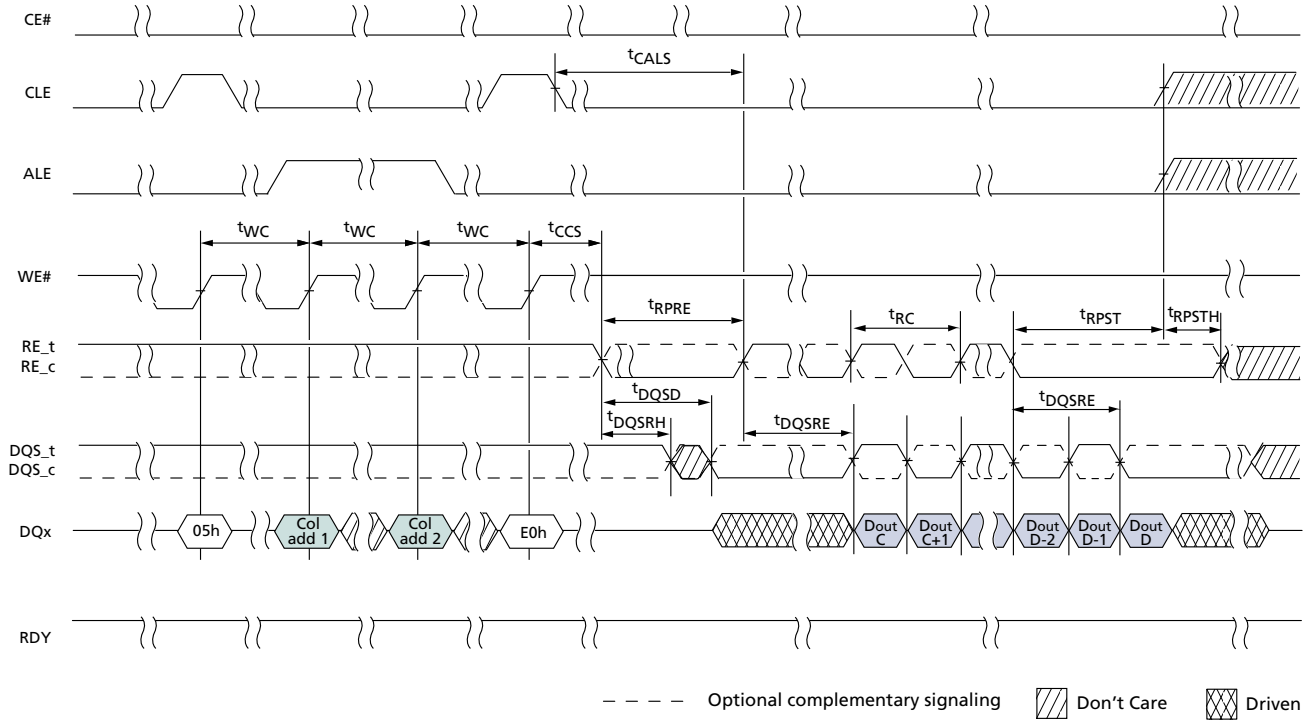
Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 160: READ PAGE Operation



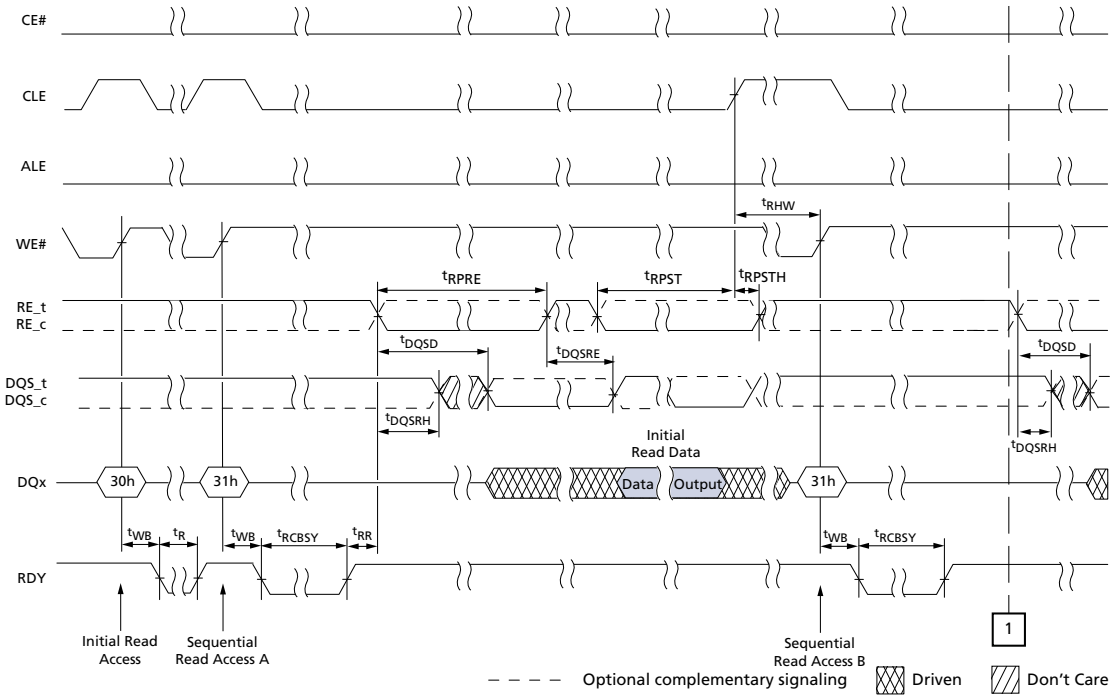
Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 161: CHANGE READ COLUMN



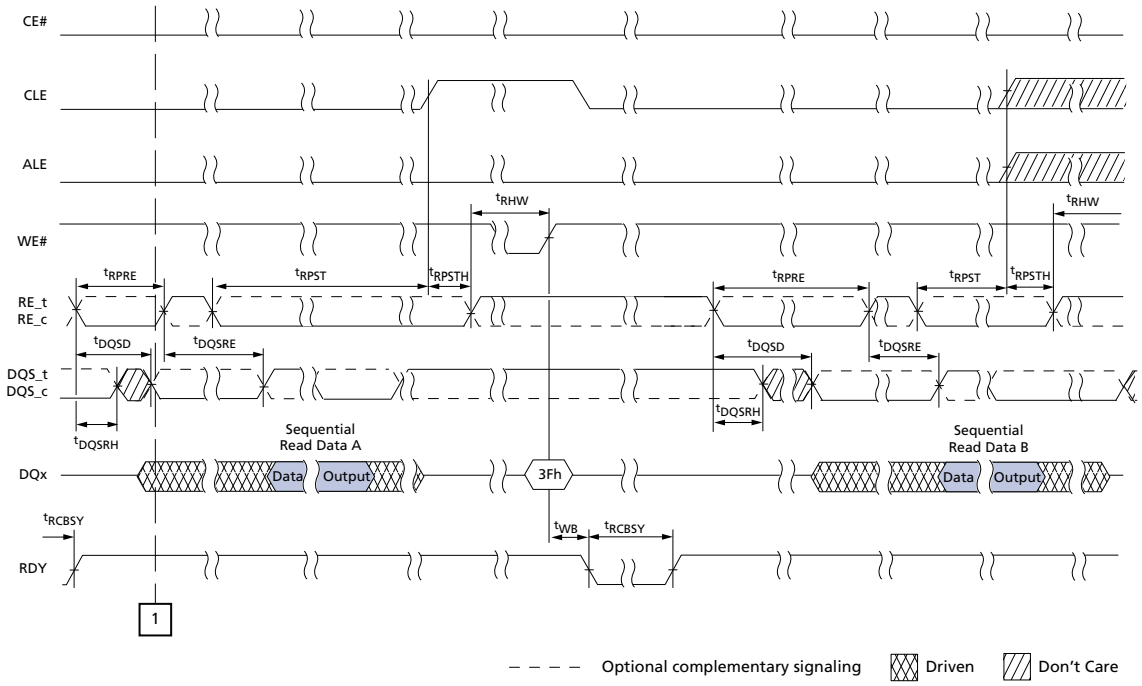
Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 162: READ PAGE CACHE SEQUENTIAL (1 of 2)



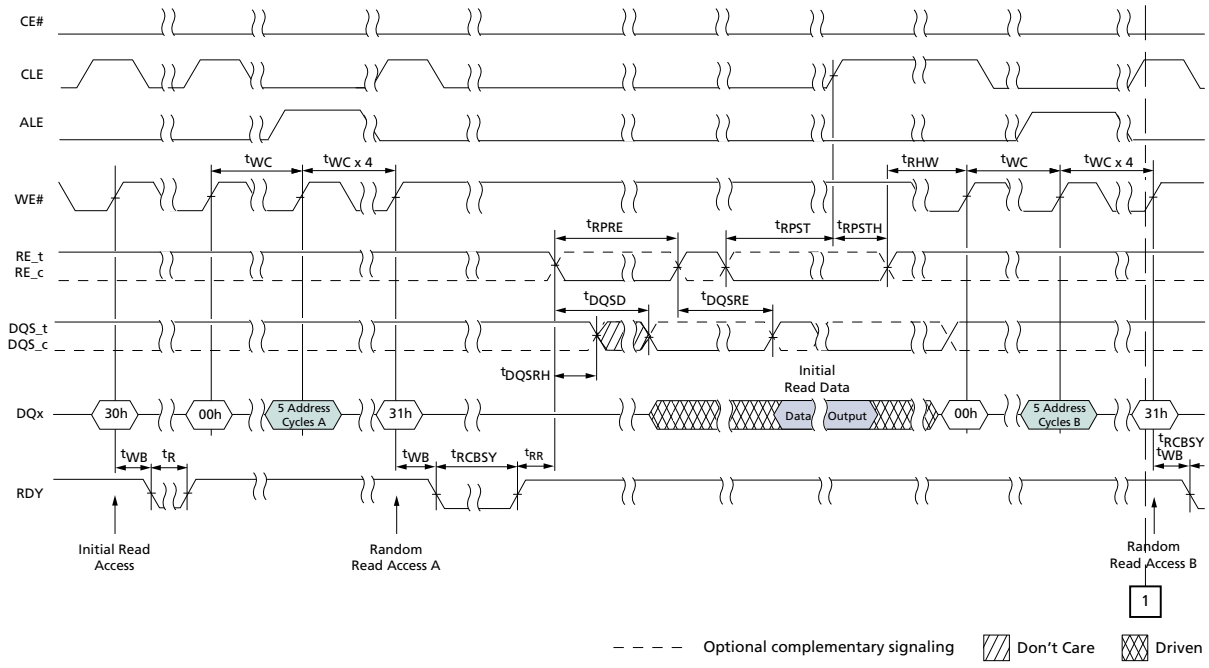
Note: 1. DQS is "don't care" during active command cycle (CLE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 163: READ PAGE CACHE SEQUENTIAL (2 of 2)



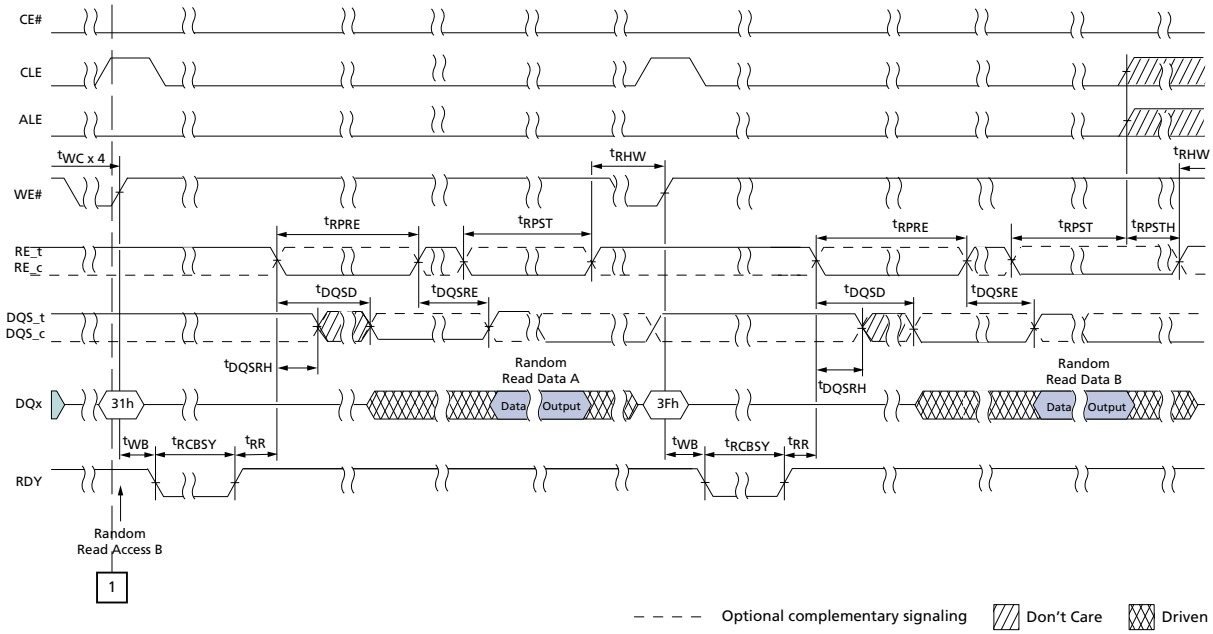
Note: 1. DQS is "don't care" during active command cycle (CLE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 164: READ PAGE CACHE RANDOM (1 of 2)



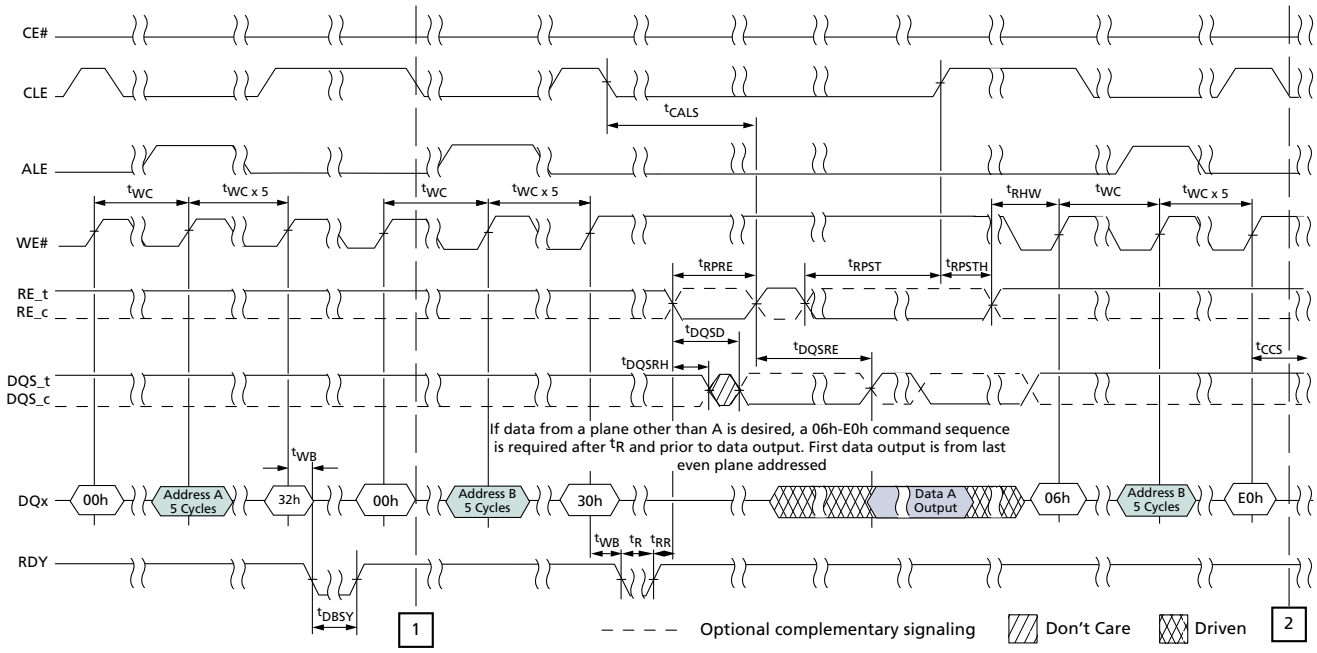
Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 165: READ PAGE CACHE RANDOM (2 of 2)



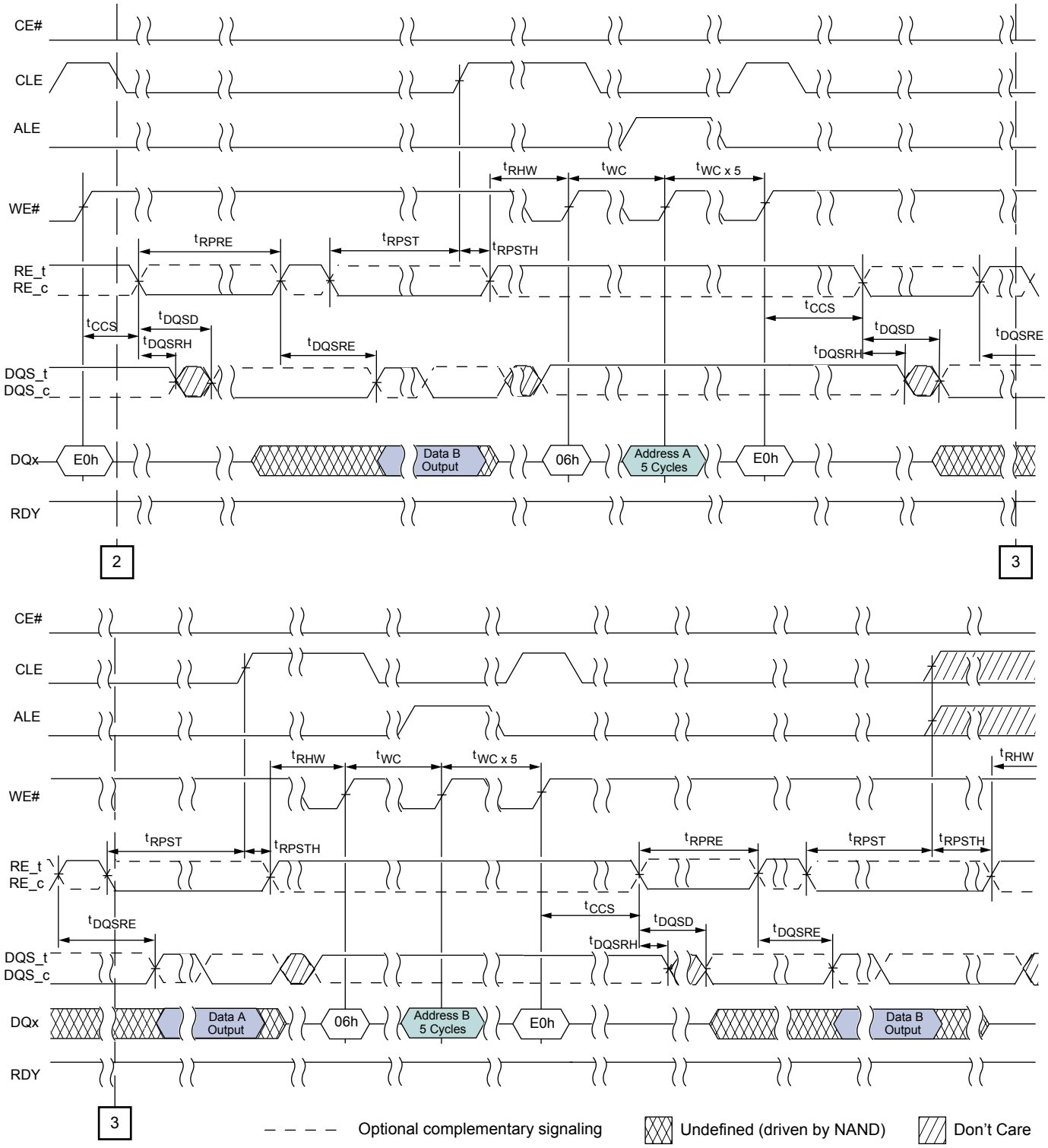
Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 166: Multi-Plane Read Page (1 of 2)



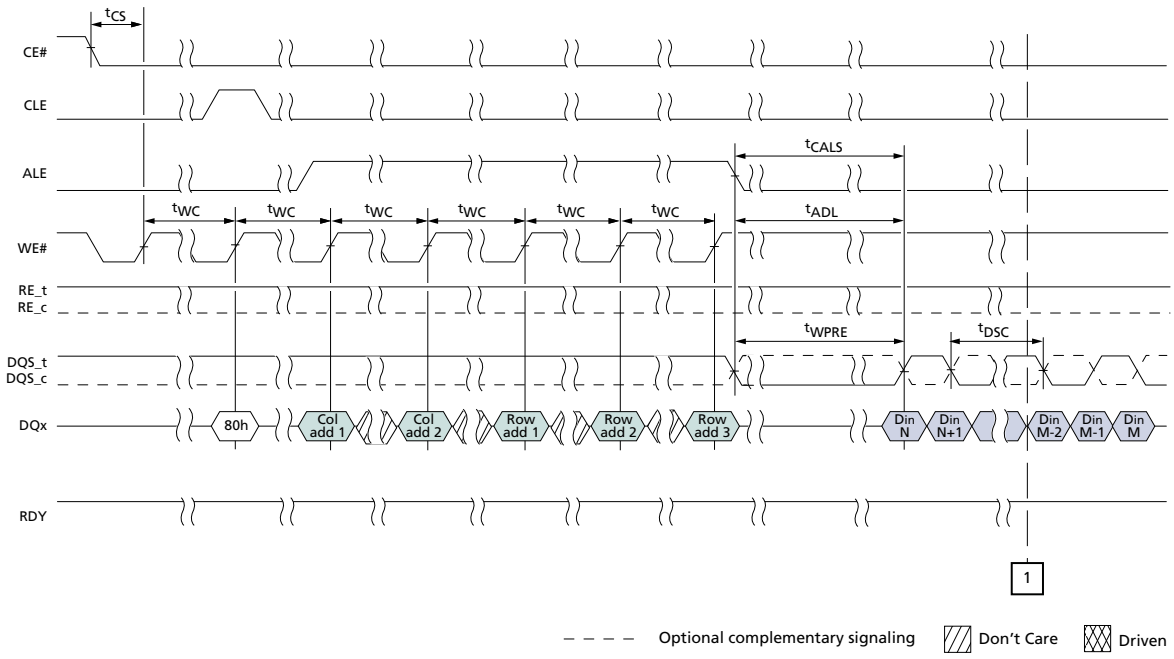
Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 167: Multi-Plane Read Page (2 of 2)



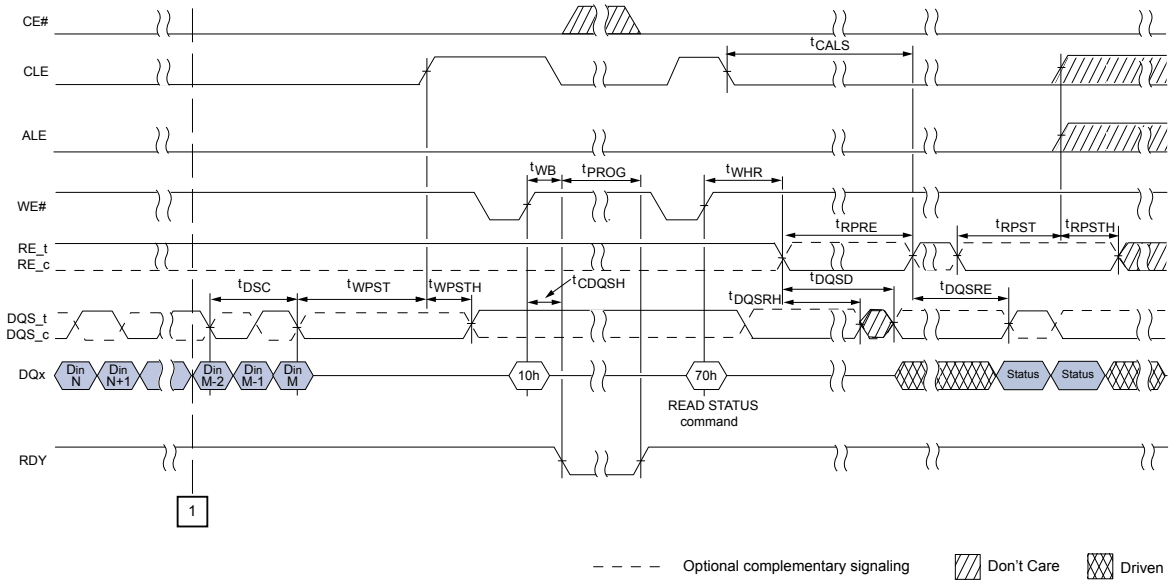
Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 168: PROGRAM PAGE Operation (1 of 2)



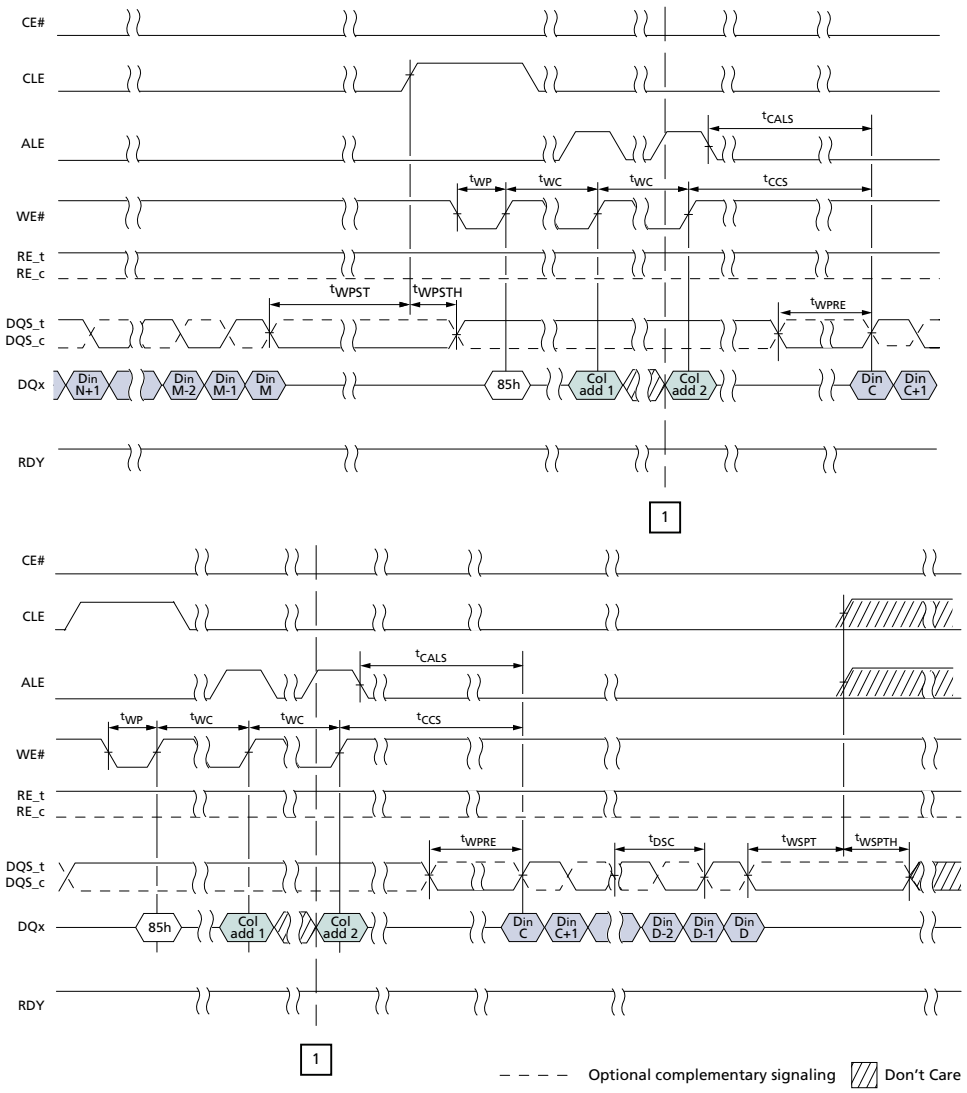
Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 169: PROGRAM PAGE Operation (2 of 2)



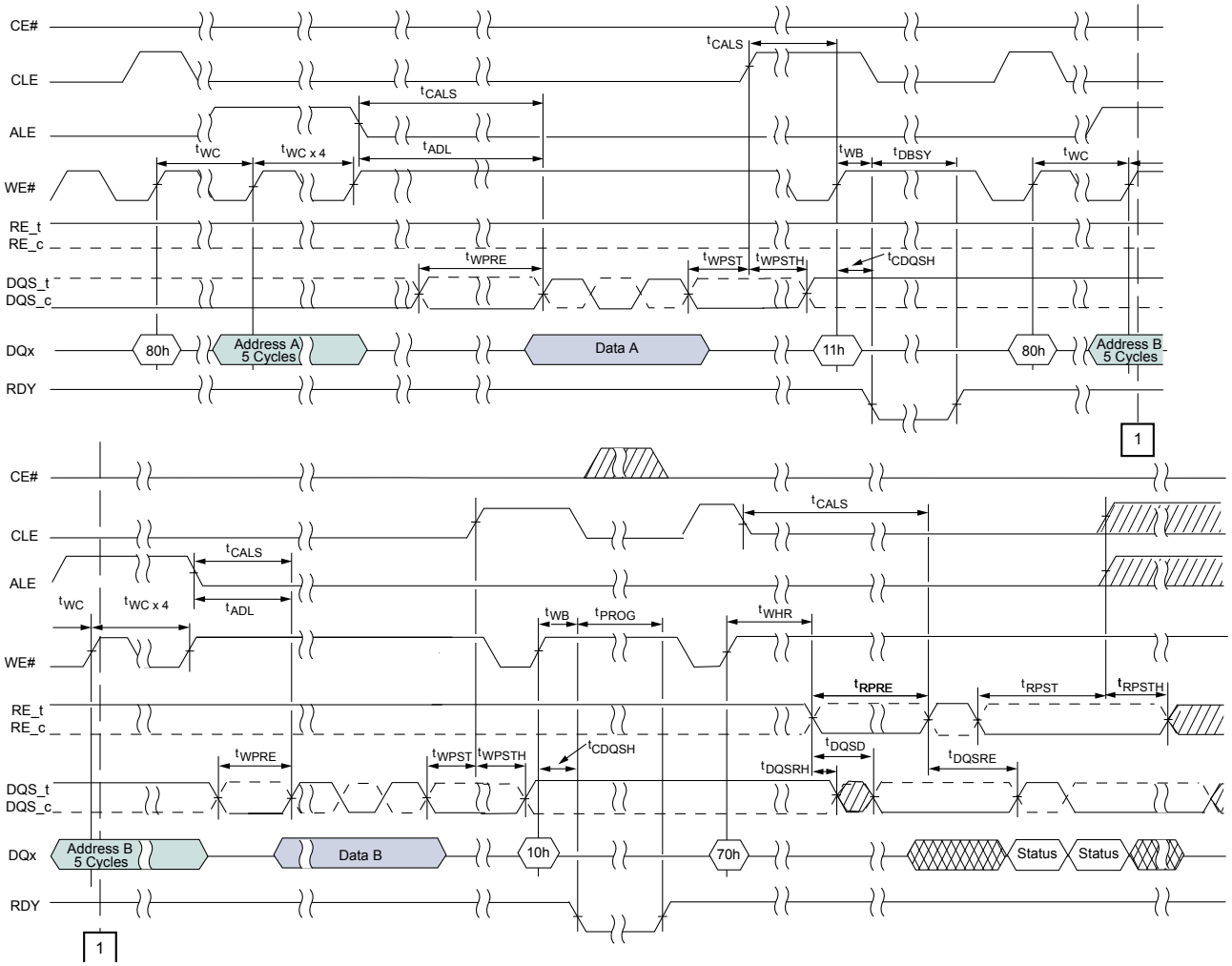
Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 170: CHANGE WRITE COLUMN



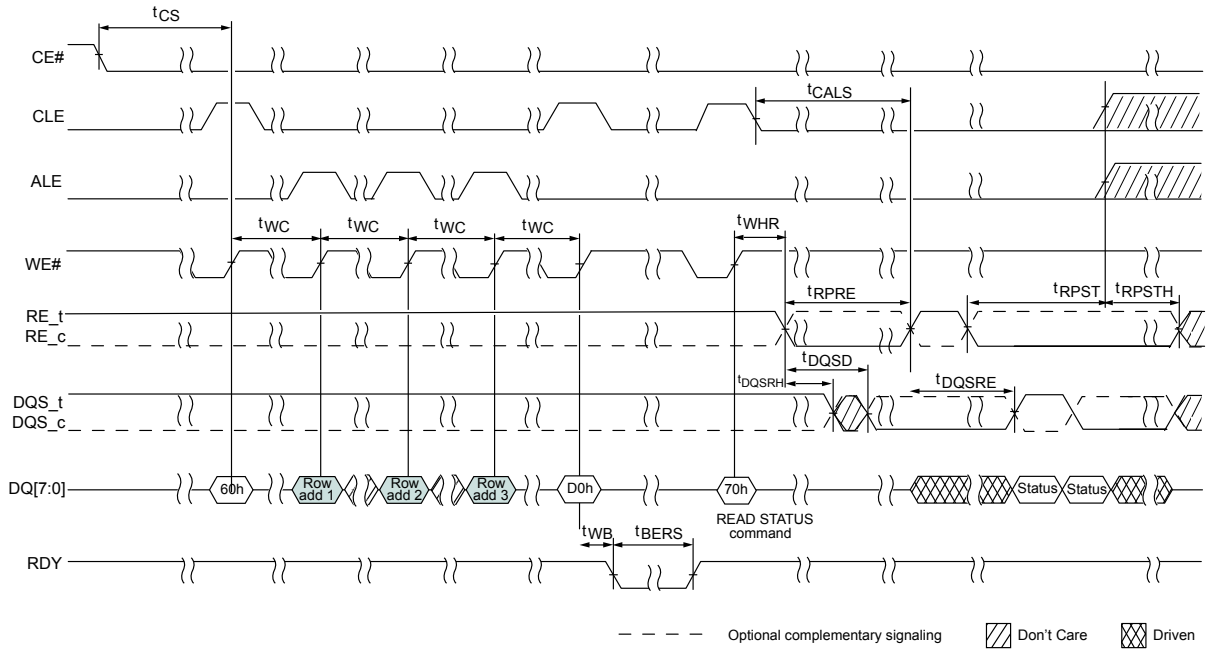
Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 171: Multi-Plane Program Page



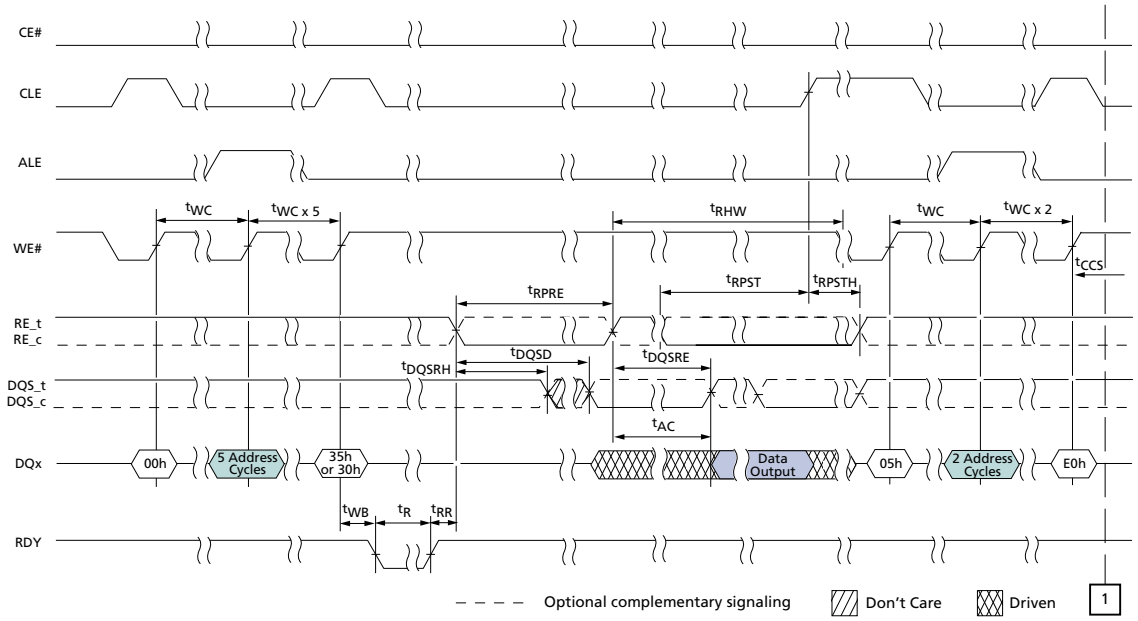
Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 172: ERASE BLOCK



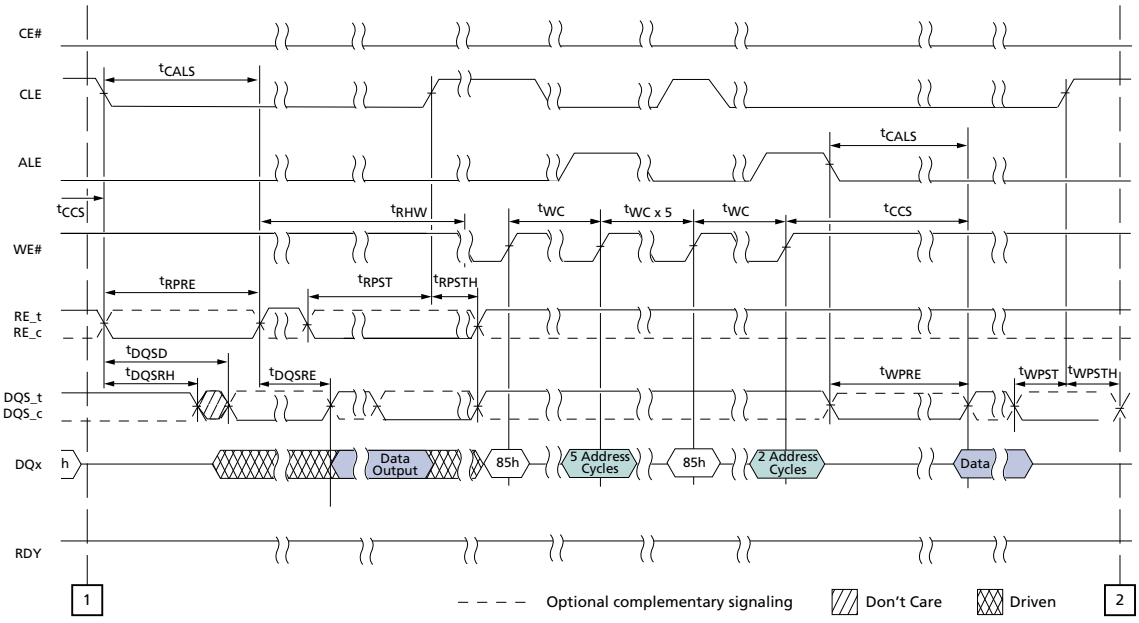
Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 173: COPYBACK (1 of 3)



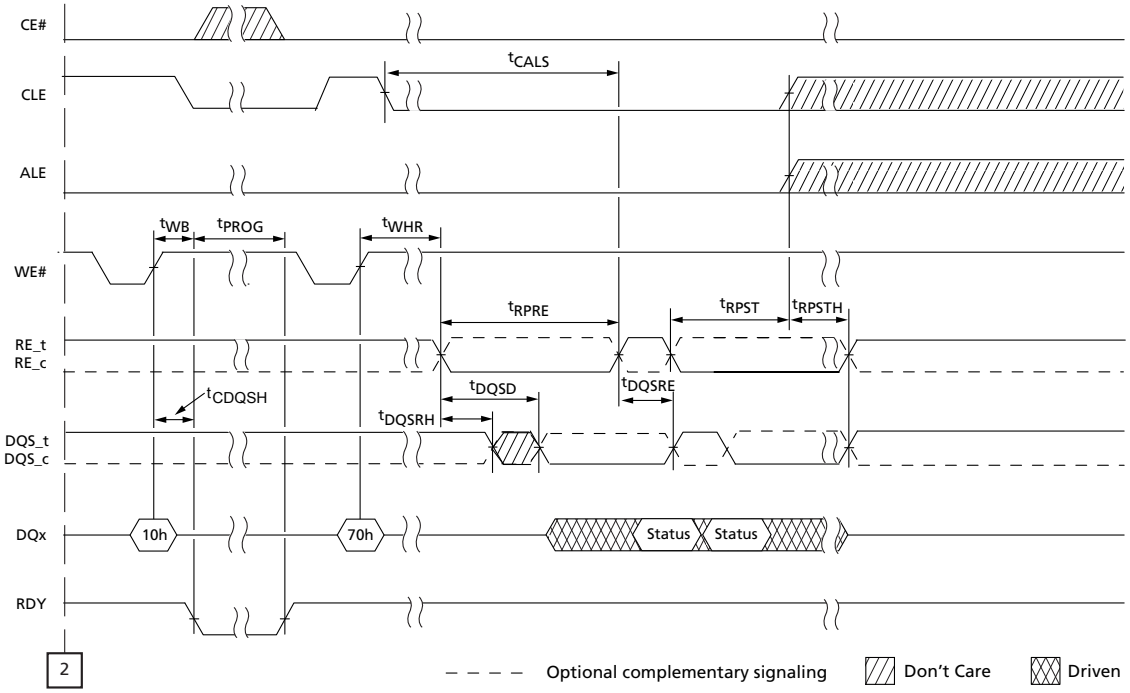
Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 174: COPYBACK (2 of 3)



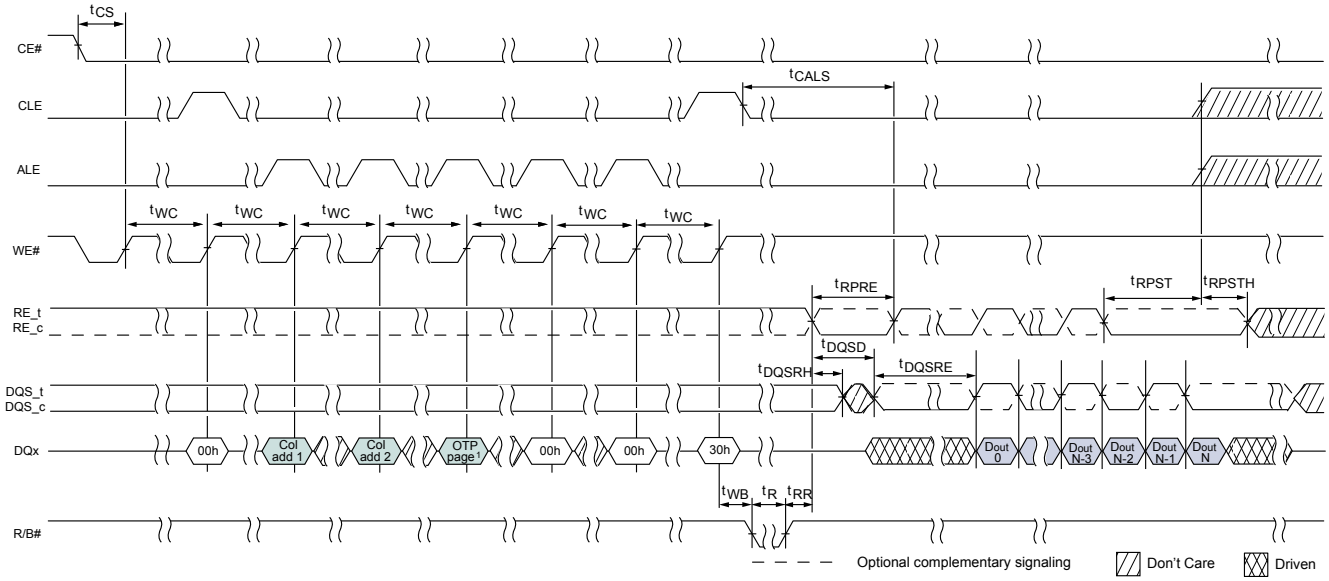
Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 175: COPYBACK (3 of 3)



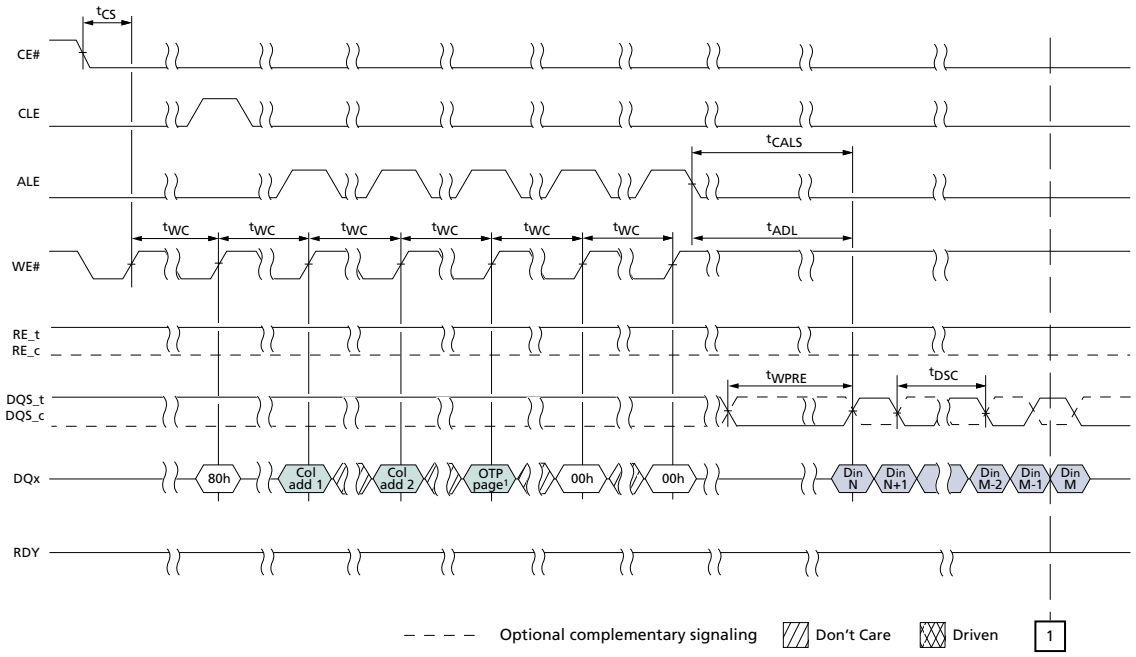
Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 176: READ OTP PAGE



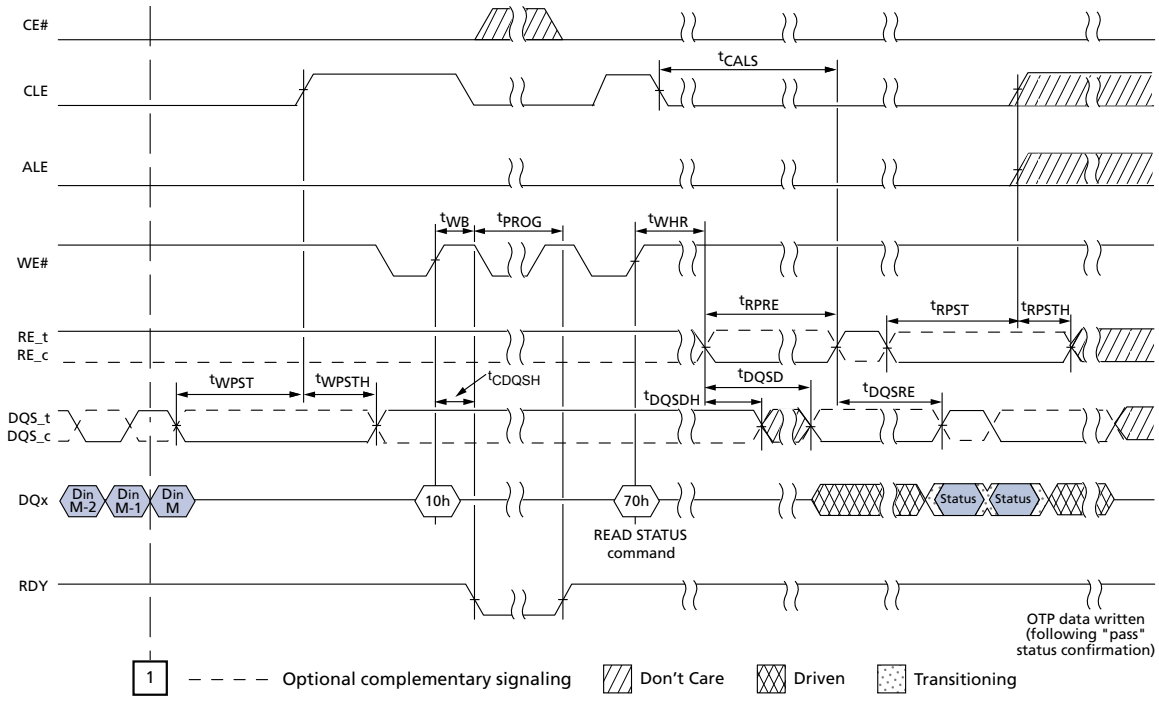
Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 177: PROGRAM OTP PAGE (1 of 2)



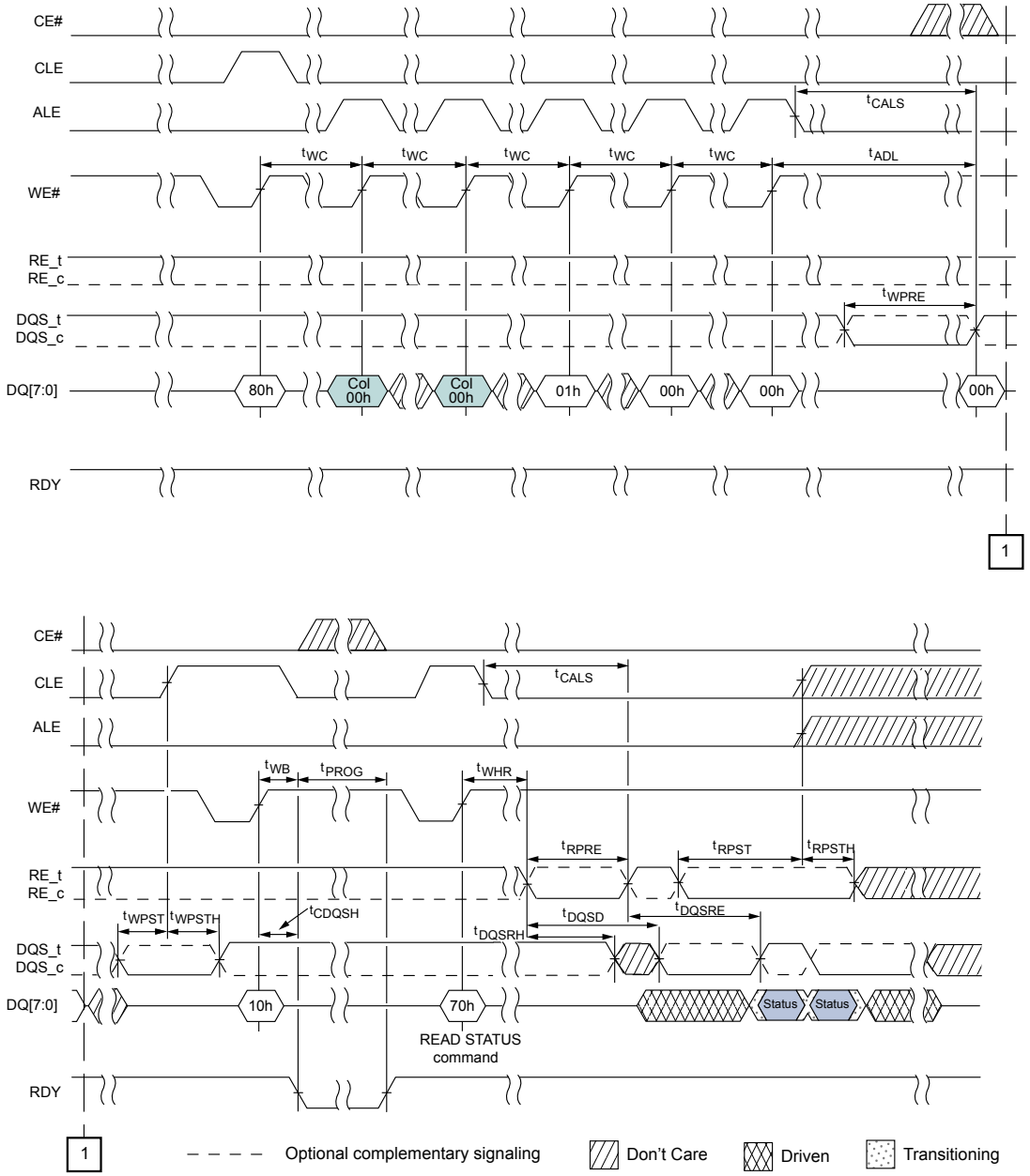
Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 178: PROGRAM OTP PAGE (2 of 2)



Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Figure 179: PROTECT OTP AREA



Note: 1. DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Revision History

Rev. E – 11/20/15

- Under Device and Array Organization section:
  - Corrected 'Device Organization for Eight-Die Package with four CE# (132-ball)' figure to reference the correct array organization figure for that configuration
  - Under Array Addressing for Logical Unit (LUN) table:
    - Added additional text to note 1 for added clarification of 'Consequently, the first and second cycles containing the column addresses are known as C1 and C2, and the third, fourth, and fifth cycles containing the row addresses cycles are known as R1, R2, and R3 respectively.'
    - Added additional text to note 3 for added clarification of 'CA[14:0] address column addresses 0 through 18,591 (16,384 + 2208) (489Fh), therefore...'
- Under CE# Pin Reduction and Volume Addressing section, subsection Selecting a Volume, added statement of 'After CE# is held LOW for at least 100ns...'
- Under Reset Operations section, for RESET (FFh), SYNCHRONOUS RESET (FCh) and RESET LUN (FAh) subsection changed the statement 'The data register and cache register contents are invalid' to 'The data register and cache register contents are **valid**'
- Under Status Operations section, Status Register Definition table for FAILC bit description, added additional description to further clarify that this status bit applies only to PROGRAM- and COPYBACK PROGRAM-series operations
- Under Configuration Operations section, Feature Address F5h: Partial Page Read / Express Read, changed Paritial Page Read function to Snap Read function:
  - Under Express Read function description, added "In addition to Read Status (70h/78h) and RESET (FFh/FCh/FAh) commands, the host is allowed to issue CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) when Status Register bit 5 (ARDY) is LOW and Status Register bit 6 (RDY) is HIGH during Express Read."
- Under ERASE SUSPEND (61h) and ERASE RESUME (D2h) section, updated paragraph:
  - 'While an erase is suspended, if host issues a program command to the suspended block or in the case of multi-plane program, if at least one of the blocks addressed has a suspended erase, the program is aborted with short busy time (t_{ESPDN}) and the LOCK status (SR[7] = 0) is set. In this case, the erase that was suspended keeps it's suspend state and can still be resumed. If host issues a program command to a block or LUN address other than the suspended block, also in case of a multi-plane program operation, as long as the suspended block is not one of the addressed blocks, then the program is performed and the erase that was suspended keeps it's suspend state. The program operation is not allowed to be suspended while there is a erase suspended for a given LUN that is in the erase suspend state.'
- Under Multi-Plane Operations section, separate last paragraph describing status checking for MULTI-PLANE PROGRAM/ERASE operations into two paragraphs, one for MULTI-PLANE PROGRAM operations and one for MULTI-PLANE ERASE operations to be more specific for each case
- Under Electrical Specifications section:
  - Under Recommended Operating Conditions table per updates to ONFI 4.0, updated note "AC Noise on the supply voltages shall not exceed +/- 100mV (250kHz to

Release: 11/30/15

20MHz). AC and DC noise together shall stay within the Min-Max range specified in this table." to "AC Noise on the supply voltages shall not exceed +/- 3% (10kHz to 800MHz). AC and DC noise together shall stay within the Min-Max range specified in this table." associated with V_{CC} specifications. This note now also associated with V_{CCQ} specifications.

  - Removed note "AC Noise on the supply voltages shall not exceed +/- 50mV (250kHz to 20MHz). AC and DC noise together shall stay within the Min-Max range specified in this table." that was associated with V_{CCQ} specifications

- Under Package Electrical Specification and Pad Capacitance sub-section:
  - Updated sentence "Z_{IO} and Td_{IO} apply to DQ[7:0]. DQS_t, DQS_c, RE_t and RE_c." to the following three sentences "Z_{IO} applies to DQ[7:0]. DQS_t, DQS_c, RE_t and RE_c. $Td_{IO\ RE}$ applies to RE_t and RE_c. Td_{IO} and $Td_{IO\ Mismatch}$ apply to DQ[7:0], DQS_t and DQS_c."
  - Added parameter $Td_{IO\ RE}$ parameter to table Package Electrical Specifications
  - Changed Td_{IO} Max for 667MT/s column in table Package Electrical Specifications to 145ps
  - Changed $Td_{IO\ Mismatch}$ for 533MT/s and 667MT/s columns in table Package Electrical Specifications to 40ps

- Under Shared Pages section, updated table for missing page relationships for pages 209, 211, 213, 215, 272, 274, 276, and 278
- Under Electrical Specifications – DC Characteristics and Operating Conditions (NV-DDR, NV-DDR2, NV-DDR3) section:
  - Under DC Characteristics and Operating Conditions (NV-DDR, NV-DDR2 Interface) 1.8V V_{CCQ} table:
    - Updated I_{CCQ4R_S} TYP to 28mA and Max 37mA for speeds up to 200MT/s
    - Updated I_{CCQ4R_S} TYP to 55mA and Max 72mA for speeds greater than 200MT/s up to 400MT/s
    - Updated I_{CCQ4R_S} TYP to 75mA and Max 98mA for speeds greater than 400MT/s
    - Created separate I_{CC5} parameter for the NV-DDR interface
  - Under DC Characteristics and Operating Conditions (NV-DDR3 Interface) 1.2V V_{CCQ} table:
    - Updated I_{CCQ4R_S} TYP to 38mA and Max 50mA for speeds greater than 200MT/s up to 400MT/s
    - Updated I_{CCQ4R_S} TYP to 68mA and Max 88mA for speeds greater than 400MT/s up to 667MT/s
    - Updated I_{SBQ} Max to 50µA
- Under Electrical Specifications – Array Characteristics section:
  - Removed ^{t}RPP and ^{t}RPPER parameters
  - Added ^{t}RSNAP parameter

Rev. D – 9/9/15

- Under Device and Array Organization section, Array Organization per Logical Unit (LUN) table, clarified note two to apply to NV-DDR/NV-DDR2/NV-DDR3 interfaces
- Updated Configuration Operations section

Rev. C – 8/15

- Under Features section:
  - Updated Erase Block time to 15ms (TYP)
  - Updated Combined PARTIAL PAGE READ and EXPRESS READ operation time without/with V_{PP} to Single-Plane EXPRESS READ operation without/with V_{PP} to 64µs/61µs (TYP)
  - Single-Plane READ PAGE operation time without/with V_{PP} to 66µs/63µs (TYP)
  - Multi-Plane READ PAGE operation time without/with V_{PP} 77/63µs (TYP)
  - Under Quality and reliability heading, added Testing methodology description and updated text for Data retention
- Under Part Numbering Information section, removed 132-ball BGA J6 package code and replaced with M5 package code
- Under Package Dimensions section, removed 132-Ball LBGA – 12mm x 18mm (Package Code: J6) figure and replaced with 132-Ball LBGA – 12mm x 18mm (Package Code: M5) figure
- Under ONFI Parameter Page Data Structure table:
  - Updated for removal of MT29F4T08CTHBBJ6 part number and additional of MT29F4T08CTHBBM5 part number
  - Updated bytes 135–136 to C8h, AFh
  - Updated byte 137 to 5Dh
  - Updated byte 152 to 75h
  - Updated byte 162 to 03h
  - Updated byte 180 to 10h
  - Updated byte 253 to 02h
  - Updated bytes 254–255 for all devices
- Under JEDEC Parameter Page Data Structure table:
  - Updated for removal of MT29F4T08CTHBBJ6 part number and additional of MT29F4T08CTHBBM5 part number
  - Updated bytes 155–156 to C8h, AFh
  - Updated bytes 157 to 5Dh
  - Updated bytes 159 to 75h
  - Updated byte 420 to 02h
  - Updated byte 422 to 10h
  - Updated bytes 510–511 for all devices
- Under Electrical Specifications - Array Characteristics section:
  - Updated ^{t}BERS TYP to 15ms and ^{t}BERS Max to 45ms
  - Updated ^{t}ESPD Max to 800µs
  - Updated ^{t}R TYP without/with V_{PP} to 77µs/63µs and ^{t}R Max without/with V_{PP} to 117µs/88µs
  - Updated ^{t}R_SP TYP without/with V_{PP} to 66µs/63µs and ^{t}R Max without/with V_{PP} to 93µs/88µs
  - Updated ^{t}RER TYP without/with V_{PP} to 75µs/61µs and ^{t}RER Max without/with V_{PP} to 115µs/86µs

- Updated ^{t}RER_SP TYP without/with V_{PP} to 64µs/61µs and ^{t}RER_SP Max without/with V_{PP} to 61µs/86µs
- Updated ^{t}RPP TYP without/with V_{PP} to 69µs/66µs and ^{t}RPP Max without/with V_{PP} to 96µs/91µs
- Updated ^{t}RPPER TYP without/with V_{PP} to 67µs/64µs and ^{t}RPPER Max without/with V_{PP} to 94µs/89µs

Rev. B – 7/31/15

- Under ONFI Parameter Page Data Structure table:
  - Corrected text typo to byte 14 to 3Dh
- Under JEDEC Parameter Page Data Structure table:
  - Corrected text typo to byte 157 to 73h
  - Corrected text typo to byte 159 to 89h

Rev. A – 7/22/15

- Initial release

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