TOSHIBA MULTI-CHIP INTEGRATED CIRCUIT SILICON GATE CMOS

TENTATIVE

Low Power SDRAM, Nand E²PROM and Giga Byte Nand E²PROM Mixed Multi-Chip Package

Lead-Free

DESCRIPTION

The TYAD00AC00BUGK is a mixed multi-chip package containing a 1,073,741,824-bit (536,870,912-bit × 2devices) Low Power Synchronous DRAMs and a 1,107,296,256-bit Nand E²PROM and a 1G-Byte Nand E²PROM device which has NAND memory controller function internally (GBNand).
The TYAD00AC00BUGK is available in a 224-pin BGA package making it suitable for a variety of applications.

Features

- Power supply voltage
  - Low power SDRAM : 1.7 to 1.9 V
  - Nand E²PROM : 1.7 to 1.95 V
  - GBNand : 2.7 to 3.6 V
- Operating temperature of –30° to 85°C
- Package
  - P-FBGA224-1218-0.80BZ (Weight: g)
- Lead-Free

Low Power SDRAM Features

- Organization : 2pcs of 4M × 32 bits × 4 banks (32 bits I/O)
- Power dissipation (Each devices)
  - Operating : 75 mA maximum
  - Burst operating: 95mA maximum
  - Refresh : 90 mA maximum
  - Self refresh : 800 μA maximum
- Programmable driver strength
- Clock frequency: 133MHz (max.)
- Row address : A0 to A12
- Column address : A0 to A8
- 4 internal banks for concurrent operation
- Interface : LVCMOS
- Burst lengths (BL) : 1, 2, 4, 8, full page
- Burst type (BT) :
  - Sequential (1, 2, 4, 8, full page)
  - Interleave (1, 2, 4, 8)
- $\overline{\text{CAS}}$ Latency (CL) : 2, 3
- Precharge :
  - auto precharge operation for each burst access
- Driver strength: normal/weak
- Refresh : auto-refresh, self-refresh
- Refresh cycles : 8192 refresh cycles/64ms
  - Average refresh period : 7.8μs
- Operating junction temperature range
- Single pulsed $\overline{\text{RAS}}$
- Burst read/write operation and burst read/single write operation capability
- Byte control by DQM
- Programmable Partial Array Self Refresh
- Auto Temperature Compensated Self Refresh by built-in temperature sensor
- Deep power down mode
- Burst termination by burst stop command and Precharge command

Nand E²PROM Features

- Organization
  - Memory cell array : 264 × 256K × 16 bits
  - Register : 264 × 16 bits
  - Page size : 264 words
  - Block size : (8K + 264) bytes
- Power dissipation
  - Read operating : 30 mA maximum
  - Program / Erase operating : 30 mA maximum
  - Standby : 50 μA maximum
- Access time :
  - Cell array register : 25 μs @CL=30pF
  - Serial read cycle : 50 ns @CL=30pF
- Modes :
  - Read , Reset , Auto page program
  - Auto block erase , Status read
- Mode control
  - Serial input / output , Command control
- Program/Erase cycles
  - 100,000 cycles (with external ECC control)

GB Nand E²PROM Features

- Host interface is based on SD card.
  Host can read/write high capacity NAND flash memory easily and efficiently without implementing complex flash memory access procedure.
- Media Format
  - Security Functions:
    - SD Security Specification Ver.1.01 Compliant (CPRM Based)
    - *CPRM: Contents Protection for Recording Media Specification
  - Logical Format:
    - SD File System Specification Ver.1.01 Compliant (DOS-FAT Based formatted)
- Interfaces:
  - SD Card Interface, (SD: 4 or 1bit)
  - SPI Mode Compatible
  - SD Physical Layer Specification Ver.1.01 Compliant

PIN ASSIGNMENT (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
	○													
A	NC	NC	NC	NC							NC	NC	NC	NC
B	NC	NC	NC	NC							NC	NC	NC	NC
C	NC	NC	V_{CCd}	DQ0	DQ2	DNU	V_{SS}	V_{CCn}	DNU	DNU	A1	V_{CCd}	NC	NC
D	NC	V_{SS}	DQ1	DQ3	DQ4	DQn15	DQn14	DQn13	DQn12	$\overline{CS1}$	BA1	A2	V_{SS}	NC
E	NC	V_{CCQd}	DQ5	DQM0	DQ6	DQn7	DQn5	DQn3	DQn1	$\overline{RAS}$	BA0	A0	A3	NC
F		V_{SS}	DNU	DQM1	DQ7	DQn11	DQn10	DQn9	DQn8	$\overline{CAS}$	$\overline{CS0}$	A10	V_{CCd}	
G		V_{CCQd}	DNU	DQ9	DQ8	DQn6	DQn4	DQn2	DQn0	$\overline{WEd}$	CLK	DNU	DNU	
H		DNU	DNU	DNU	DNU	V_{SS}			$V_{CCg}2$	DNU	DNU	DNU	DNU	
J		V_{SS}	DQ12	DQ11	DQ10	DNU			TESTOUT1	TST0	DNU	DNU	CKCRO	
K		V_{CCd}	DQ15	DQ14	DQ13	DNU			DNU	$V_{CCg}1$	V_{SS}	CKCRA	CKCRI	
L		V_{SS}	DQ16	DQ17	DQ18	DNU			DNU	SDCMD	$V_{CCg}1$	SDCLK	V_{SS}	
M		V_{CCQd}	DQ19	DQ20	DQ21	DNU			SDDAT3	SDDAT0	SDDAT1	SDDAT2	V_{SS}	
N		V_{SS}	DNU	DQ22	DQ23	DNU			DNU	TST2	V_{SS}	$V_{CCg}1$	DNU	
P		DNU	DNU	DNU	DNU	DNU	$V_{CCg}3$	V_{SS}	DNU	DNU	DNU	DNU	V_{SS}	
R		V_{CCQd}	DNU	DQM2	DQ24	DNU	$\overline{CE}$	$\overline{WEn}$	$\overline{WP}$	CKE1	CKE0	A11	V_{SS}	
T	NC	V_{SS}	DQ26	DQM3	DQ25	DNU	$\overline{RE}$	ALE	DNU	DNU	A12	A7	A4	NC
U	NC	V_{CCd}	DQ30	DQ28	DQ27	DNU	RY/$\overline{BY}$	CLE	DNU	A9	A8	A5	V_{CCd}	NC
V	NC	NC	V_{SS}	DQ31	DQ29	DNU	V_{SS}	V_{CCn}	DNU	DNU	A6	V_{SS}	NC	NC
W	NC	NC	NC	NC							NC	NC	NC	NC
Y	NC	NC	NC	NC							NC	NC	NC	NC

PIN NAMES

A0 to A12	Address inputs for Low Power SDRAM
BA0,BA1	Bank Select for Low Power SDRAM
DQ0 to DQ31	Data inputs / outputs for Low Power SDRAM
CLK	Clock input for Low Power SDRAM
CKE0 , CKE1	Clock enable for Low Power SDRAM
$\overline{CS0}$, $\overline{CS1}$	Chip select for Low Power SDRAM
$\overline{RAS}$	Row address strobe for Low Power SDRAM
$\overline{CAS}$	Column address strobe for Low Power SDRAM
$\overline{WEd}$	Write enable for Low Power SDRAM
DQM0, DQM1 DQM2, DQM3	Data mask enable for Low Power SDRAM
DQn0 to DQn15	I/O port Nand E^2PROM
$\overline{CE}$	Chip enable for Nand E^2PROM
$\overline{RE}$	Read enable for Nand E^2PROM
$\overline{WEn}$	Write enable for Nand E^2PROM
CLE	Command latch enable for Nand E^2PROM
ALE	Address latch enable for Nand E^2PROM
$\overline{WP}$	Write protect for Nand E^2PROM
RY/$\overline{BY}$	Ready/Busy for Nand E^2PROM
SDDAT0 to SDDAT3	Data Line for GBNand
SDCMD	Command/Response for GBNand
SDCLK	Clock input for GBNand
CKCRI CKCRO CKCRA	CR Clock Oscillator for GBNand (Connects to the external capacitor and resisters of oscillation.)
TST0 , TST2	Test Mode setting for GBNand
TESTOUT1	Test Clock Output for GBNand
V_{CCd}	Main power supply for Low Power SDRAM
V_{CCQd}	DQ power supply for Low Power SDRAM
V_{CCn}	Power supply for Nand E^2PROM
$V_{CCg}1$, $V_{CCg}2$, $V_{CCg}3$	Power supply for for GBNand
V_{SS}	Ground
DNU	Do not use (Must be OPEN)
NC	Not connected

PIN NAME CONVERSION TABLE

MCP Pin		512Mb LPSD(1)	512Mb LPSD(2)	1Gb Nand	1GB Nand
Loc	Name				
C3	VCCd	VDD	VDD	–	–
C4	DQ0	DQ0	DQ0	–	–
C5	DQ2	DQ2	DQ2	–	–
C6	DNU	–	–	–	–
C7	VSS	VSS*	VSS*	VSS	VSS
C8	VCCn	–	–	VCC	–
C9	DNU	–	–	–	–
C10	DNU	–	–	–	–
C11	A1	A1	A1	–	–
C12	VCCd	VDD	VDD	–	–
D2	VSS	VSS*	VSS*	VSS	VSS
D3	DQ1	DQ1	DQ1	–	–
D4	DQ3	DQ3	DQ3	–	–
D5	DQ4	DQ4	DQ4	–	–
D6	DQn15	–	–	I/O16	–
D7	DQn14	–	–	I/O15	–
D8	DQn13	–	–	I/O14	–
D9	DQn12	–	–	I/O13	–
D10	$\overline{CS}$1	–	$\overline{CS}$	–	–
D11	BA1	BA1	BA1	–	–
D12	A2	A2	A2	–	–
D13	VSS	VSS*	VSS*	VSS	VSS
E2	VCCQd	VDDQ	VDDQ	–	–
E3	DQ5	DQ5	DQ5	–	–
E4	DQM0	DQM0	DQM0	–	–
E5	DQ6	DQ6	DQ6	–	–
E6	DQn7	–	–	I/O8	–
E7	DQn5	–	–	I/O6	–
E8	DQn3	–	–	I/O4	–
E9	DQn1	–	–	I/O2	–
E10	$\overline{RAS}$	$\overline{RAS}$	$\overline{RAS}$	–	–
E11	BA0	BA0	BA0	–	–
E12	A0	A0	A0	–	–
E13	A3	A3	A3	–	–
F2	VSS	VSS*	VSS*	VSS	VSS
F3	DNU	–	–	–	–
F4	DQM1	DQM1	DQM1	–	–
F5	DQ7	DQ7	DQ7	–	–
F6	DQn11	–	–	I/O12	–
F7	DQn10	–	–	I/O11	–
F8	DQn9	–	–	I/O10	–
F9	DQn8	–	–	I/O9	–
F10	$\overline{CAS}$	$\overline{CAS}$	$\overline{CAS}$	–	–
F11	$\overline{CS}$0	$\overline{CS}$	–	–	–
F12	A10	A10	A10	–	–
F13	VCCd	VDD	VDD	–	–
G2	VCCQd	VDDQ	VDDQ	–	–
G3	DNU	–	–	–	–
G4	DQ9	DQ9	DQ9	–	–
G5	DQ8	DQ8	DQ8	–	–
G6	DQn6	–	–	I/O7	–
G7	DQn4	–	–	I/O5	–
G8	DQn2	–	–	I/O3	–
G9	DQn0	–	–	I/O1	–
G10	$\overline{WE}$d	$\overline{WE}$	$\overline{WE}$	–	–
G11	CLK	CLK	CLK	–	–
G12	DNU	–	–	–	–
G13	DNU	–	–	–	–

MCP Pin		512Mb LPSD(1)	512Mb LPSD(2)	1Gb Nand	1GB Nand
Loc	Name				
H2	DNU	–	–	–	–
H3	DNU	–	–	–	–
H4	DNU	–	–	–	–
H5	DNU	–	–	–	–
H6	VSS	VSS*	VSS*	VSS	VSS
H9	VCCg2	–	–	–	Vdd2
H10	DNU	–	–	–	–
H11	DNU	–	–	–	–
H12	DNU	–	–	–	–
H13	DNU	–	–	–	–
J2	VSS	VSS*	VSS*	VSS	VSS
J3	DQ12	DQ12	DQ12	–	–
J4	DQ11	DQ11	DQ11	–	–
J5	DQ10	DQ10	DQ10	–	–
J6	DNU	–	–	–	–
J9	TESTOUT1	–	–	–	TESTOUT1
J10	TST0	–	–	–	TST0
J11	DNU	–	–	–	–
J12	DNU	–	–	–	–
J13	CKCRO	–	–	–	CKCRO
K2	VCCd	VDD	VDD	–	–
K3	DQ15	DQ15	DQ15	–	–
K4	DQ14	DQ14	DQ14	–	–
K5	DQ13	DQ13	DQ13	–	–
K6	DNU	–	–	–	–
K9	DNU	–	–	–	–
K10	VCCg1	–	–	–	Vdd1
K11	VSS	VSS*	VSS*	VSS	VSS
K12	CKCRA	–	–	–	CKCRA
K13	CKCRI	–	–	–	CKCRI
L2	VSS	VSS*	VSS*	VSS	VSS
L3	DQ16	DQ16	DQ16	–	–
L4	DQ17	DQ17	DQ17	–	–
L5	DQ18	DQ18	DQ18	–	–
L6	DNU	–	–	–	–
L9	DNU	–	–	–	–
L10	SDCMD	–	–	–	–
L11	VCCg1	–	–	–	Vdd1
L12	SDCLK	–	–	–	SDCLK
L13	VSS	VSS*	VSS*	VSS	VSS
M2	VCCQd	VDDQ	VDDQ	–	–
M3	DQ19	DQ19	DQ19	–	–
M4	DQ20	DQ20	DQ20	–	–
M5	DQ21	DQ21	DQ21	–	–
M6	DNU	–	–	–	–
M9	SDDAT3	–	–	–	SDDAT3
M10	SDDAT0	–	–	–	SDDAT0
M11	SDDAT1	–	–	–	SDDAT1
M12	SDDAT2	–	–	–	SDDAT2
M13	VSS	VSS*	VSS*	VSS	VSS
N2	VSS	VSS*	VSS*	VSS	VSS
N3	DNU	–	–	–	–
N4	DQ22	DQ22	DQ22	–	–
N5	DQ23	DQ23	DQ23	–	–
N6	DNU	–	–	–	–
N9	DNU	–	–	–	–
N10	TST2	–	–	–	TST2
N11	VSS	VSS*	VSS*	VSS	VSS

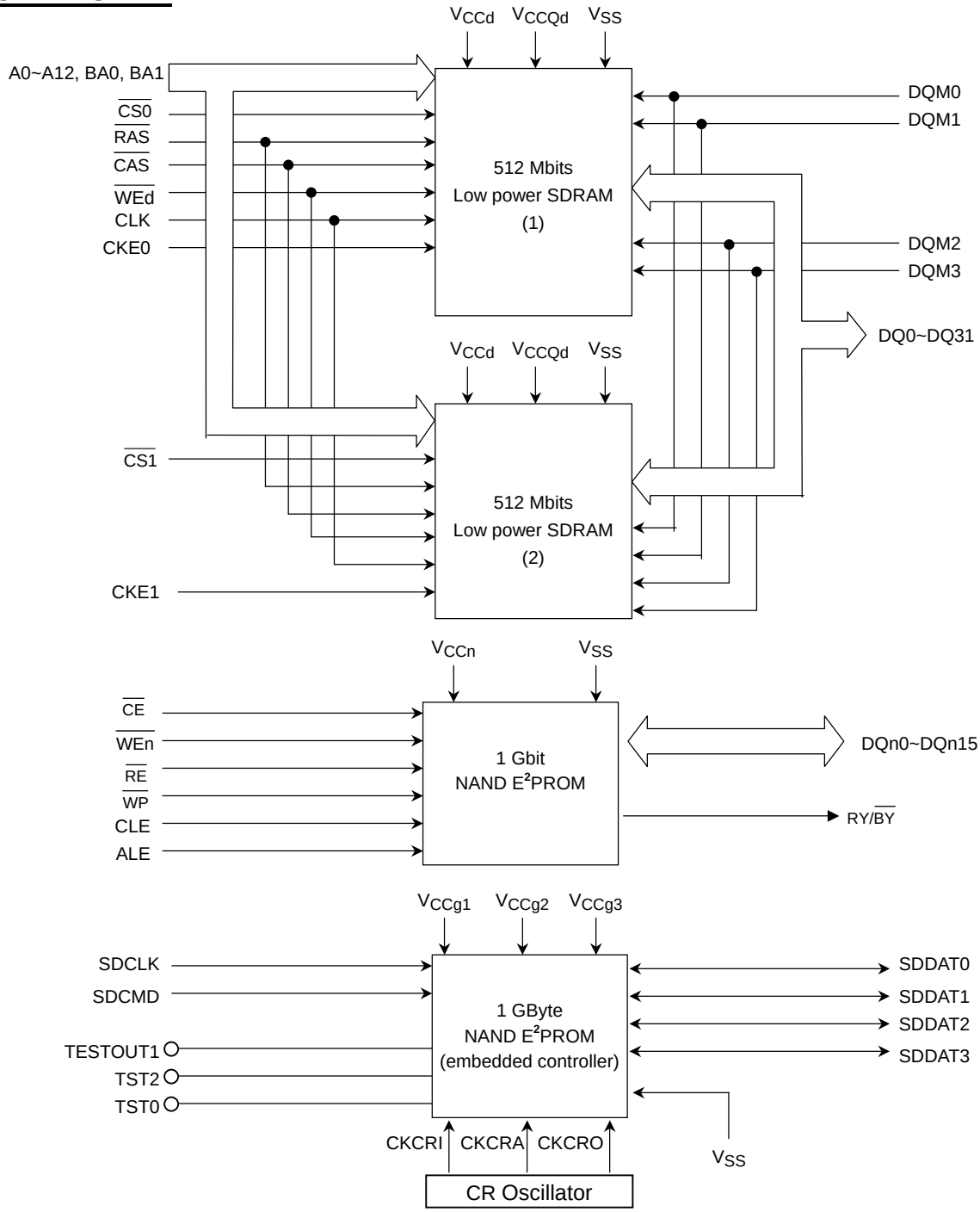
PIN NAME CONVERSION TABLE(Continue)

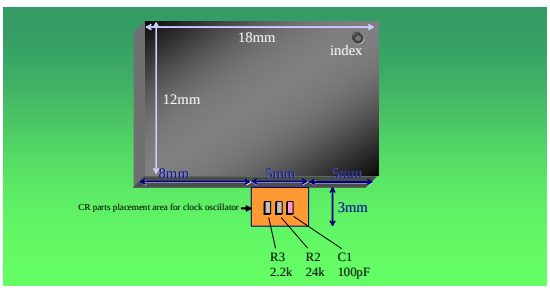
MCP Pin		512Mb LPSD(1)	512Mb LPSD(2)	1Gb Nand	1GB Nand
Loc	Name				
N12	VCCg1	–	–	–	Vdd1
N13	DNU	–	–	–	–
P2	DNU	–	–	–	–
P3	DNU	–	–	–	–
P4	DNU	–	–	–	–
P5	DNU	–	–	–	–
P6	DNU	–	–	–	–
P7	VCCg3	–	–	–	Vdd3
P8	VSS	VSS*	VSS*	VSS	VSS
P9	DNU	–	–	–	–
P10	DNU	–	–	–	–
P11	DNU	–	–	–	–
P12	DNU	–	–	–	–
P13	VSS	VSS*	VSS*	VSS	VSS
R2	VCCQd	VDDQ	VDDQ	–	–
R3	DNU	–	–	–	–
R4	DQM2	DQM2	DQM2	–	–
R5	DQ24	DQ24	DQ24	–	–
R6	DNU	–	–	–	–
R7	$\overline{CE}$	–	–	$\overline{CE}$	–
R8	$\overline{WEn}$	–	–	$\overline{WE}$	–
R9	$\overline{WP}$	–	–	$\overline{WP}$	–
R10	CKE1	–	CKE	–	–
R11	CKE0	CKE	–	–	–
R12	A11	A11	A11	–	–
R13	VSS	VSS*	VSS*	VSS	VSS
T2	VSS	VSS*	VSS*	VSS	VSS
T3	DQ26	DQ26	DQ26	–	–
T4	DQM3	DQM3	DQM3	–	–
T5	DQ25	DQ25	DQ25	–	–
T6	DNU	–	–	–	–
T7	$\overline{RE}$	–	–	$\overline{RE}$	–
T8	ALE	–	–	ALE	–
T9	DNU	–	–	–	–
T10	DNU	–	–	–	–
T11	A12	A12	A12	–	–
T12	A7	A7	A7	–	–
T13	A4	A4	A4	–	–
U2	VCCd	VDD	VDD	–	–
U3	DQ30	DQ30	DQ30	–	–
U4	DQ28	DQ28	DQ28	–	–
U5	DQ27	DQ27	DQ27	–	–
U6	DNU	–	–	–	–
U7	RY/$\overline{BY}$	–	–	RY/$\overline{BY}$	–
U8	CLE	–	–	CLE	–
U9	DNU	–	–	–	–
U10	A9	A9	A9	–	–
U11	A8	A8	A8	–	–
U12	A5	A5	A5	–	–
U13	VCCd	VDD	VDD	–	–

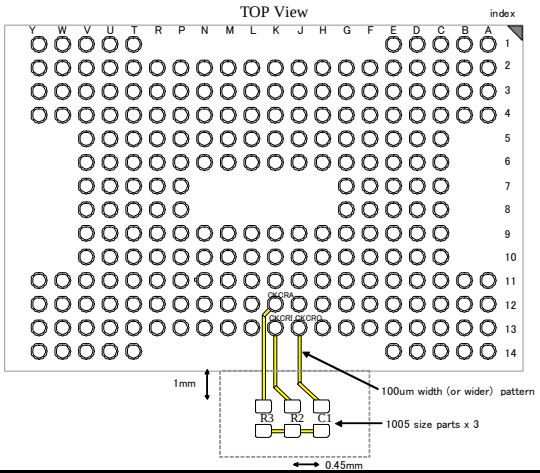
MCP Pin		512Mb LPSD(1)	512Mb LPSD(2)	1Gb Nand	1GB Nand
Loc	Name				
V3	VSS	VSS*	VSS*	VSS	VSS
V4	DQ31	DQ31	DQ31	–	–
V5	DQ29	DQ29	DQ29	–	–
V6	DNU	–	–	–	–
V7	VSS	VSS*	VSS*	VSS	VSS
V8	VCCn	–	–	VCC	–
V9	DNU	–	–	–	–
V10	DNU	–	–	–	–
V11	A6	A6	A6	–	–
V12	VSS	VSS*	VSS*	VSS	VSS
A1-4	NC	–	–	–	–
A11-14	NC	–	–	–	–
B1-4	NC	–	–	–	–
B11-14	NC	–	–	–	–
C1-2	NC	–	–	–	–
C13-14	NC	–	–	–	–
D1	NC	–	–	–	–
D14	NC	–	–	–	–
E1	NC	–	–	–	–
E14	NC	–	–	–	–
T1	NC	–	–	–	–
T14	NC	–	–	–	–
U1	NC	–	–	–	–
U14	NC	–	–	–	–
V1-2	NC	–	–	–	–
V13-14	NC	–	–	–	–
W1-4	NC	–	–	–	–
W11-14	NC	–	–	–	–
Y1-4	NC	–	–	–	–
Y11-14	NC	–	–	–	–

VSS* : VSS / VSSQ

BLOCK DIAGRAM







ELECTRICAL SPECIFICATIOS (LPSDRAM)

- All voltages are referenced to VSS (GND).
- After power up, wait more than 200 μs and then, execute Power on sequence and two Auto Refresh before proper device operation is achieved.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RANGE	UNIT
V_{CCd}	LPSDRAM V_{CCd} Supply Voltage		−0.5~2.3	V
V_{CCQd}	LPSDRAM V_{CCQd} Supply Voltage (DQ)		−0.5~2.3	V
V_{CCn}	Nand E^2PROM V_{CCn} Supply Voltage		−0.5~4.6	V
V_{CCg}	GB Nand E^2PROM $V_{CCg1,2,3}$ Supply Voltage		−0.3~4.6	V
V_{IN}	Input Voltage	LPSDRAM	−0.5~2.3	V
		Nand E^2PROM	−0.5~4.6	V
		GB Nand E^2PROM	−0.3~V_{CCg} + 0.3 (≤ 4.6)	V
V_{DQ}	Input/Output Voltage	LPSDRAM	−0.5~ 2.3	V
		Nand E^2PROM	−0.5~V_{CCn} + 0.3 (≤ 4.6)	V
		GB Nand E^2PROM	−0.3~V_{CCg} + 0.3 (≤ 4.6)	V
T_{opr}	Operating Temperature		−30~85	°C
P_D	Power Dissipation		0.6	W
T_{solder}	Soldering Temperature		260	°C
I_{OSHORT}	Output Short Circuit Current(1)		50	mA
T_{stg}	Storage Temperature		−55~125	°C

Note : (1) Output shorted for no more than one second. No more than one output shorted at a time

Caution

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS (Ta = –30°~85°C)

SYMBOL	PARAMETER		MIN	TYP.	MAX	UNIT
V_{CCd}	LPSDRAM V_{CCd} Supply Voltage		1.7	—	1.9	V
V_{CCQd}	LPSDRAM V_{CCQd} Supply Voltage (DQ)		1.7	—	1.9	
V_{CCn}	Nand E^2PROM V_{CCn} Supply Voltage		1.7	—	1.95	
V_{CCg}	GBNand E^2PROM $V_{CCg1,2,3}$ Supply Voltage		2.7	—	3.6	
V_{IH}	Input High-Level Voltage	LPSDRAM	$0.8 \times V_{CCQd}$	—	$V_{CCQd} + 0.3$ (1)	
		Nand E^2PROM	$0.78 \times V_{CCn}$	—	$V_{CCn} + 0.3$ (2)	
		GBNand E^2PROM	$0.625 \times V_{CCg}$	—	$V_{CCg} + 0.3$	
V_{IL}	Input Low-Level Voltage	LPSDRAM	–0.3 (3)	—	0.3	
		Nand E^2PROM	–0.3 (4)	—	$0.22 \times V_{CCn}$	
		GBNand E^2PROM	–0.3	—	$0.25 \times V_{CCg}$	

Note: (1) $V_{IH(MAX)} = 2.3$ V for pulse width ≤ 5 ns

(2) $V_{CCn} + 1$ V for pulse width < 2 ns

(3) $V_{IH(MAX)} = –0.5$ V for pulse width ≤ 5 ns

(4) –2.0 V for pulse width ≤ 20 ns

CAPACITANCE (LPSDRAM / Nand E^2PROM) (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER		CONDITION	MIN	MAX	UNIT
C_{IN}	Input Capacitance	LPSDRAM	V_{IN} = GND	—	TBD	pF
		Nand E^2PROM		—	TBD	pF
C_{OUT}	Output Capacitance	LPSDRAM	V_{OUT} = GND	—	TBD	pF
		Nand E^2PROM		—	TBD	pF

Note: These parameters are sampled periodically and are not tested for every device.

CAPACITANCE (GB Nand)

ITEM	SYMBOL	MIN	MAX	UNIT	NOTE
Pull up Resistance	R_{CMD} R_{DAT}	10	100	K Ohm	
Bus Signal Line Capacitance	C_L	-	250	pF	F_{PP}<5MHz (21Cards)
Bus Signal Line Capacitance	C_L	-	100	pF	F_{PP}<20MHz (7Cards)
Single Card Capacitance	C_{CARD}	-	10	pF	
Pull up Resistance inside card(DAT3)	R_{DAT3}	10	90	K Ohm	

DC CHARACTERISTICS - 1 (LPSDRAM-1 ($\overline{CS0}$, CKE0))

(Ta = –30°~85°C, V_{CCd} / V_{CCQd} = 1.7V~1.9V, V_{CCn} = 1.7V~1.95V , V_{CCg} = 2.7V~3.6V)

SYMBOL	PARAMETER	CONDITION		MIN	MAX	UNIT
I_{CC1sd}	LPSDRAM Operating current(1)	Burst length=1 , tRC ≥ tRC min, I_{OUT} = 0 mA , One bank active		—	75	mA
I_{CC2Psd}	LPSDRAM Standby current in power down	CKE0 ≤ V_{IL} max, tCK = tCK min		—	0.8	mA
$I_{CC2PSsd}$	LPSDRAM Standby current in power down (Input signal stable)	CKE0 ≤ V_{IL} max, tCK = ∞		—	0.6	mA
I_{CC2Nsd}	LPSDRAM Standby current in non power down	CKE0 ≥ V_{IH} min, tCK = tCK min, $\overline{CS0}$ ≥ V_{IH} min Input signals are changed one time during 2tCK		—	4	mA
$I_{CC2NSsd}$	LPSDRAM Standby current in non power down (Input signal stable)	CKE0 ≥ V_{IH} min, tCK = ∞ , Input signals are stable		—	2	mA
I_{CC3Psd}	LPSDRAM Active standby Current in power down	CKE0 ≤ V_{IL} max, tCK = tCK min		—	3	mA
$I_{CC3PSsd}$	LPSDRAM Active standby Current in power down (Input signal stable)	CKE0 ≤ V_{IL} max, tCK = ∞		—	1.2	mA
I_{CC3Nsd}	LPSDRAM Active standby Current in non power down	CKE0 ≥ V_{IH} min , tCK = tCK min, $\overline{CS0}$ ≥ V_{IH} min Input signals are changed one time during 2tCK		—	10	mA
$I_{CC3NSsd}$	LPSDRAM Active standby Current in non power down (Input signal stable)	CKE0 ≥ V_{IH} min , tCK = ∞ , Input signals are stable		—	7	mA
I_{CC4sd}	LPSDRAM Burst operating current (2)	tCK ≥ tCK min, I_{OUT} = 0 mA , All banks active	$\overline{CAS}$ latency=2	—	55	mA
			$\overline{CAS}$ latency=3	—	95	mA
I_{CC5sd}	LPSDRAM Refresh current (3)	tRC1 ≥ tRC1 min		—	90	mA
I_{CC6sd}	LPSDRAM Self refresh current (4)	CKE0 ≤ 0.2V	PASR="000" (Full)	—	800	μA
			PASR="001" (2BK)	—	650	μA
			PASR="010" (1BK)	—	490	μA
		Ta ≤ 40°C CKE0 ≤ 0.2V	PASR="000" (Full)		300	μA
			PASR="001" (2BK)		240	μA
			PASR="010" (1BK)		210	μA
I_{CC7sd}	LPSDRAM Standby current in deep power down mode	CKE0 ≤ 0.2V		—	10	μA

DC CHARACTERISTICS - 2 (LPSDRAM-2 ($\overline{CS1}$, CKE1))

(Ta = –30°~85°C, V_{CCd} / V_{CCQd} = 1.7V~1.9V, V_{CCn} = 1.7V~1.95V , V_{CCg} = 2.7V~3.6V)

SYMBOL	PARAMETER	CONDITION		MIN	MAX	UNIT
I_{CC1sd}	LPSDRAM Operating current(1)	Burst length=1 , tRC ≥ tRC min, I_{OUT} = 0 mA , One bank active		—	75	mA
I_{CC2Psd}	LPSDRAM Standby current in power down	CKE1 ≤ V_{IL} max, tCK = tCK min		—	0.8	mA
$I_{CC2PSsd}$	LPSDRAM Standby current in power down (Input signal stable)	CKE1 ≤ V_{IL} max, tCK = ∞		—	0.6	mA
I_{CC2Nsd}	LPSDRAM Standby current in non power down	CKE1 ≥ V_{IH} min, tCK = tCK min, $\overline{CS1}$ ≥ V_{IH} min Input signals are changed one time during 2tCK		—	4	mA
$I_{CC2NSsd}$	LPSDRAM Standby current in non power down (Input signal stable)	CKE1 ≥ V_{IH} min, tCK = ∞ , Input signals are stable		—	2	mA
I_{CC3Psd}	LPSDRAM Active standby Current in power down	CKE1 ≤ V_{IL} max, tCK = tCK min		—	3	mA
$I_{CC3PSsd}$	LPSDRAM Active standby Current in power down (Input signal stable)	CKE1 ≤ V_{IL} max, tCK = ∞		—	1.2	mA
I_{CC3Nsd}	LPSDRAM Active standby Current in non power down	CKE1 ≥ V_{IH} min , tCK = tCK min, $\overline{CS1}$ ≥ V_{IH} min Input signals are changed one time during 2tCK		—	10	mA
$I_{CC3NSsd}$	LPSDRAM Active standby Current in non power down (Input signal stable)	CKE1 ≥ V_{IH} min , tCK = ∞ , Input signals are stable		—	7	mA
I_{CC4sd}	LPSDRAM Burst operating current (2)	tCK ≥ tCK min, I_{OUT} = 0 mA , All banks active	$\overline{CAS}$ latency=2	—	55	mA
			$\overline{CAS}$ latency=3	—	95	mA
I_{CC5sd}	LPSDRAM Refresh current (3)	tRC1 ≥ tRC1 min		—	90	mA
I_{CC6sd}	LPSDRAM Self refresh current (4)	CKE1 ≤ 0.2V	PASR="000" (Full)	—	800	μA
			PASR="001" (2BK)	—	650	μA
			PASR="010" (1BK)	—	490	μA
		Ta ≤ 40°C, CKE1 ≤ 0.2V	PASR="000" (Full)		300	μA
			PASR="001" (2BK)		240	μA
			PASR="010" (1BK)		210	μA
I_{CC7sd}	LPSDRAM Standby current in deep power down mode	CKE1 ≤ 0.2V		—	10	μA

DC CHARACTERISTICS - 3

(Ta = −30°~85°C, V_{CCd} / V_{CCQd} = 1.70V~1.90V, V_{CCn} = 1.7V~1.95V , V_{CCg} = 2.7V~3.6V)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
I_{CCO1n}	Nand Operating current (Serial Read)	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA , t_{cycle} = 50 ns	—	30	mA
I_{CCO3n}	Nand Operating current (Command input)	I_{OUT} = 0 mA, t_{cycle} = 50 ns	—	30	mA
I_{CCO4n}	Nand Operating current (Data input)	t_{cycle} = 50 ns	—	30	mA
I_{CCO5n}	Nand Operating current (Address input)	t_{cycle} = 50 ns	—	30	mA
I_{CCO7n}	Nand Programming current	—	—	30	mA
I_{CCO8n}	Nand Erasing current	—	—	30	mA
I_{CCS1n}	Nand Standby current	$\overline{CE}$ = V_{IH}, $\overline{WP}$ = 0 V or V_{CCn}	—	1	mA
I_{CCS2n}	Nand Standby current	$\overline{CE}$ = V_{CCn} − 0.2 V, $\overline{WP}$ = 0 V or V_{CCn}	—	50	μA
I_{CCOg}	GB-Nand Operating current	F_{PP} = 25MHz	—	80	mA
I_{CCSg}	GB-Nand Standby current	Clock 25MHz	—	30	mA
		Clock stop, Ta = 25°C	—	0.25	mA
Vrs	GB-Nand Input voltage Setup time	—	—	250	ms
I_{IL}	Input leakage current	V_{IN} = 0 V~V_{CCn} (V_{CCQd})	—	±10	μA
I_{OHsd}	LPSDRAM Output high current	V_{OH} = V_{CCQd} − 0.2 V	−0.1	—	mA
I_{OLsd}	LPSDRAM Output low current	V_{OL} = 0.2 V	0.1	—	mA
I_{OHn}	Nand E^2PROM Output high current	V_{OH} = V_{CCn} − 0.2 V	−0.1	—	mA
I_{OLn}	Nand E^2PROM Output low current	V_{OL} = 0.2 V	0.1	—	mA
I_{OLn} ($R\overline{Y/BY}$)	Nand E^2PROM Output Current of $R\overline{Y/BY}$ pin	V_{OL} = 0.2 V	—	4(5)	mA
I_{OHg}	GB Nand E^2PROM Output high current	V_{OH} = V_{CCg} × 0.75	−0.1	—	mA
I_{OLh}	GB Nand E^2PROM Output low current	V_{OL} = V_{CCg} × 0.125	0.1	—	mA
I_{LO}	Output leakage current	V_{OUT} = 0 V~ V_{CCn}(V_{CCQd}), I/O disable	—	±10	μA

Note :

(1) I_{CC1sd} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1sd} is measured on condition that addresses are changed only one time during tCK (min.).

(2) I_{CC4sd} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CCO4sd} is measured condition that addresses are changed only one time during tCK (min.)

(3) I_{CC5sd} is measured on condition that addresses are changed only one time during tCK (min.).

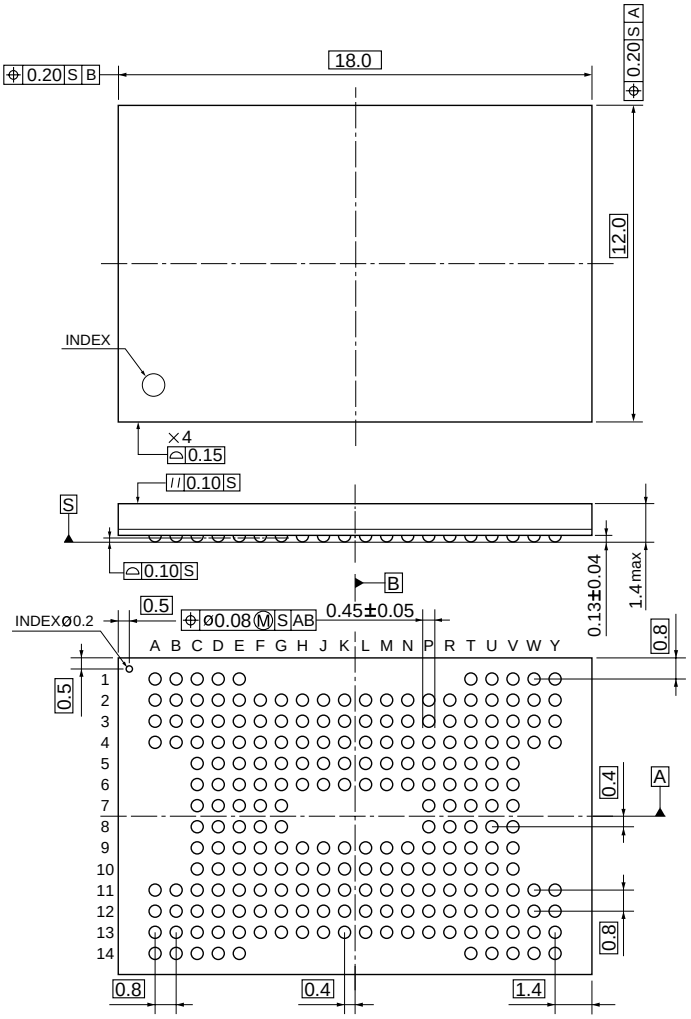
(4) I_{CC6sd} is specified when self refresh state is maintained long enough under the specified Ta condition, after a busy sequence of read and write operations. Ta is surface temperature.

(5) Typical

PACKAGE DIMENSION

Unit : mm

P-FBGA224-1218-0.80BZ



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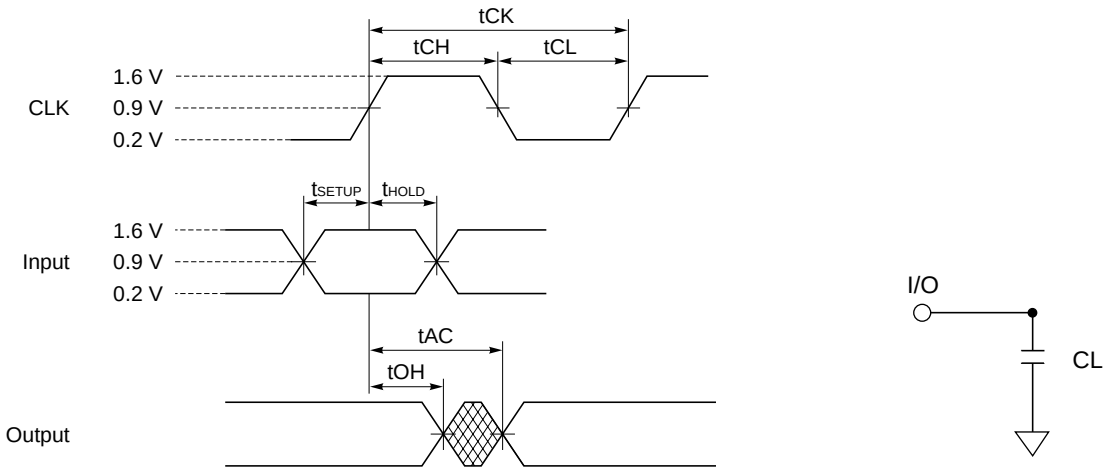
512 Mbits Low Power Synchronous Dynamic RAM

Organization : 4M words × 32 bits × 4 banks

AC Characteristics (TA = –30 to +85°C, VDD, VDDQ = 1.8V ± 0.1V, VSS, VSSQ = 0V)

Test Conditions

- AC high level input voltage / low level input voltage: 1.6 / 0.2V
- Input timing measurement reference level: 0.9V
- Transition time (Input rise and fall time): 0.5ns
- Output timing measurement reference level: 0.9V
- Output load: CL = 30pF



Synchronous Characteristics (Reference)

Parameter	Symbol	min.	max.	Unit	Note
Clock cycle time (CL= 2)	tCK2	15	—	ns	
(CL= 3)	tCK3	7.5	—	ns	
Access time from CLK (CL= 2)	tAC2	—	8	ns	1
(CL= 3)	tAC3	—	6	ns	1
CLK high level width	tCH	2.5	—	ns	
CLK low level width	tCL	2.5	—	ns	
Data-out hold time	tOH	2.6	—	ns	1
Data-out low-impedance time	tLZ	0	—	ns	
Data-out high-impedance time (CL= 2)	tHZ2	0	8	ns	
(CL= 3)	tHZ3	0	6	ns	
Data-in setup time	tDS	1.9	—	ns	
Data-in hold time	tDH	0.9	—	ns	
Address setup time	tAS	1.9	—	ns	
Address hold time	tAH	0.9	—	ns	
CKE setup time	tCKS	1.9	—	ns	
CKE hold time	tCKH	0.9	—	ns	
CKE setup time (Power down exit)	tCKSP	1.9	—	ns	
Command (/CS, /RAS, /CAS, /WE, DQM) setup time	tCMS	1.9	—	ns	
Command (/CS, /RAS, /CAS, /WE, DQM) hold time	tCMH	0.9	—	ns	

Note: 1. Output load.

Asynchronous Characteristics (Reference)

Parameter	Symbol	min.	max.	Unit	Notes
ACT to REF/ACT command period (operation)	tRC	90	—	ns	
REF to REF/ACT command period (refresh)	tRC1	112.5	—	ns	
Self refresh exit to REF/ACT command period	tRC2	120	—	ns	
ACT to PRE command period	tRAS	60	120000	ns	
PRE to ACT command period	tRP	22.5	—	ns	
Delay time ACT to READ/WRITE command	tRCD	30	—	ns	
ACT (one) to ACT (another) command period	tRRD	2	—	CLK	
Data-in to PRE command period	tDPL	2	—	CLK	
Data-in to ACT (REF) command period (Auto precharge) (CL = 2)	tDAL2	2CLK + 22.5	—	ns	
(CL = 3)	tDAL3	2CLK + 22.5	—	ns	
Mode register set cycle time	tRSC	2	—	CLK	
Transition time	tT	0.5	30	ns	
Refresh time (8,192 refresh cycles)	tREF	—	64	ms	

Pin Function

CLK (input pin)

CLK is the master clock input. Other inputs signals are referenced to the CLK rising edge.

CKE (input pins)

CKE determine validity of the next CLK (clock). If CKE is high, the next CLK rising edge is valid; otherwise it is invalid. If the CLK rising edge is invalid, the internal clock is not issued and the LPSDRAM suspends operation. When the LPSDRAM is not in burst mode and CKE is negated, the device enters power down mode. During power down mode, CKE must remain low.

/CS (input pins)

/CS low starts the command input cycle. When /CS is high, commands are ignored but operations continue.

/RAS, /CAS, and /WE (input pins)

/RAS, /CAS and /WE have the same symbols on conventional DRAM but different functions. For details, refer to the command table.

A0 to A12 (input pins)

Row Address is determined by A0 to A12 at the CLK (clock) rising edge in the active command cycle. It does not depend on the bit organization.
Column Address (See "Address Pins Table") is determined by A0 to A8 at the CLK rising edge in the read or write command cycle.

[Address Pins Table]

	Address (A0 to A12)	
Page size	Row address	Column address
2KB	AX0 to AX12	AY0 to AY8

A10 defines the precharge mode. When A10 is high in the precharge command cycle, all banks are precharged; when A10 is low, only the bank selected by BA0 and BA1 is precharged.
When A10 is high in read or write command cycle, the precharge starts automatically after the burst access.

BA0 and BA1 (input pin)

BA0 and BA1 are bank select signal. (See Bank Select Signal Table)

[Bank Select Signal Table]

	BA0	BA1
Bank A	L	L
Bank B	H	L
Bank C	L	H
Bank D	H	H

Remark: H: VIH. L: VIL. ×: VIH or VIL

DQM0 to DQM3 (input pins)

DQM controls I/O buffers. In read mode, DQM controls the output buffers like a conventional /OE pin. DQM high and DQM low turn the output buffers off and on, respectively. The DQM latency for the read is two clocks. In write mode, DQM controls the word mask. Input data is written to the memory cell if DQM is low but not if DQM is high. The DQM latency for the write is zero.

Each DQM pin corresponds to eight DQ pins, respectively (See DQM Correspondence Table).

[DQM Correspondence Table]

Organization	Data mask	DQs
x32	DQM0	DQ0 to DQ7
	DQM1	DQ8 to DQ15
	DQM2	DQ16 to DQ23
	DQM3	DQ24 to DQ31

DQ0 to DQ31 (input/output pins)

DQ pins have the same function as I/O pins on a conventional DRAM.

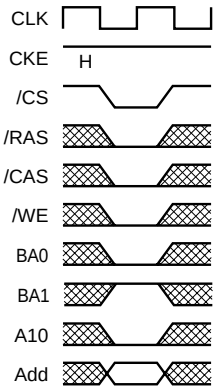
VDD, VSS, VDDQ, VSSQ (Power supply)

VDD and VSS are power supply pins for internal circuits. VDDQ and VSSQ are power supply pins for the output buffers.

Command Operation

Extended Mode register set command (/CS, /RAS, /CAS, /WE, BA0 = Low, BA1 = High)

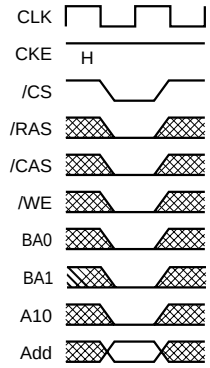
The LPSDRAM has an extended mode register that defines low power functions. In this command, A0 through A12 are the data input pins.
After power on, the extended mode register set command must be executed to fix low power functions.
The extended mode register can be set only when all banks are in idle state.
During tRSC following this command, the LPSDRAM can not accept any other commands.



Extended Mode register set command

Mode register set command (/CS, /RAS, /CAS, /WE, BA0, BA1 = Low)

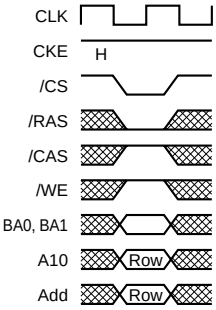
The LPSDRAM has a mode register that defines how the device operates. In this command, A0 through A12 are the data input pins. After power on, the mode register set command must be executed to initialize the device. The mode register can be set only when all banks are in idle state. During tRSC following this command, the LPSDRAM cannot accept any other commands.



Mode register set command

Activate command (/CS, /RAS = Low, /CAS, /WE = High)

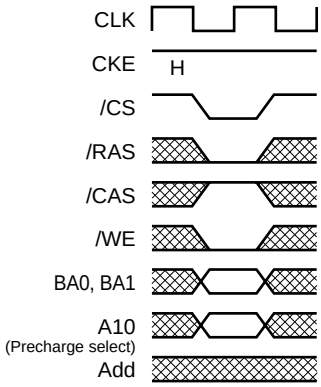
The LPSDRAM has four banks, each with 8,192 rows. This command activates the bank selected by BA0 and BA1 and a row address selected by A0 through A12. This command corresponds to a conventional DRAM's /RAS falling.



Activate command

Precharge command (/CS, /RAS, /WE = Low, /CAS = High)

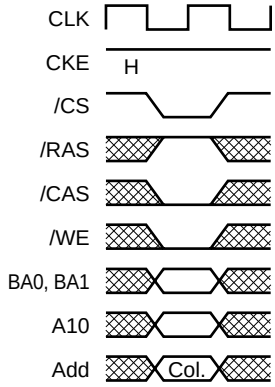
This command begins precharge operation of the bank selected by BA0 and BA1. When A10 is High, all banks are precharged, regardless of BA0 and BA1. When A10 is Low, only the bank selected by BA0 and BA1 is precharged. After this command, the LPSDRAM can't accept the activate command to the precharging bank during tRP (precharge to activate command period). This command corresponds to a conventional DRAM's /RAS rising.



Precharge command

Write command (/CS, /CAS, /WE = Low, /RAS = High)

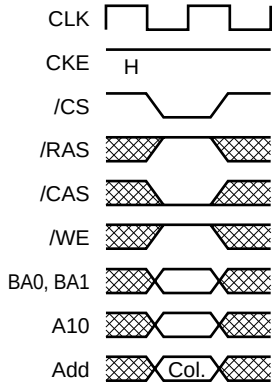
This command sets the burst start address given by the column address to begin the burst write operation. The first write data in burst mode can input with this command with subsequent data on following clocks.



Write command

Read command (/CS, /CAS = Low, /RAS, /WE = High)

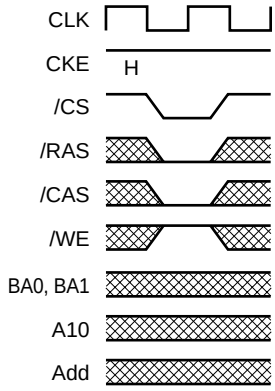
Read data is available after /CAS latency requirements have been met. This command sets the burst start address given by the column address.



Read command

Auto refresh command (/CS, /RAS, /CAS = Low, /WE, CKE = High)

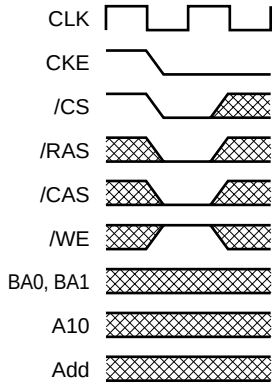
This command is a request to begin the Auto refresh operation. The refresh address is generated internally. Before executing Auto refresh, all banks must be precharged. After this cycle, all banks will be in the idle (precharged) state and ready for a row activate command. During tRC1 period (from refresh command to refresh or activate command), the LPSDRAM cannot accept any other command



Auto refresh command

Self refresh entry command (/CS, /RAS, /CAS, CKE = Low, /WE = High)

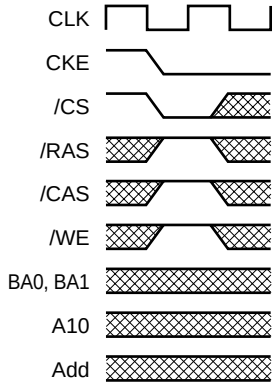
After the command execution, self refresh operation continues while CKE remains low. When CKE goes high, the LPSDRAM exits the self refresh mode. During self refresh mode, refresh interval and refresh operation are performed internally, so there is no need for external control. Before executing self refresh, all banks must be precharged.



Self refresh entry command

Power down entry command (/CS, CKE = Low, /RAS, /CAS, /WE = High)

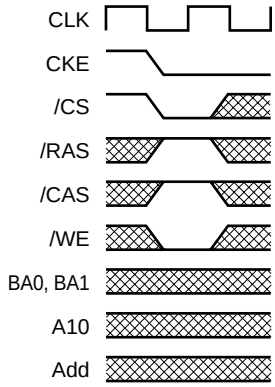
After the command execution, power down mode continues while CKE remains low. When CKE goes high, the LPSDRAM exits the power down mode. Before executing power down, all banks must be precharged.



Power down entry command

Deep power down entry command(/CS, CKE, /WE = Low, /RAS, /CAS = High)

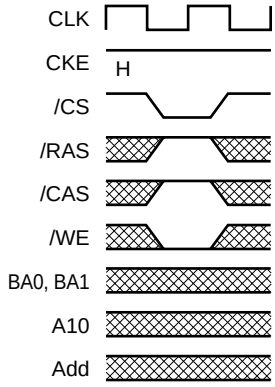
After the command execution, deep power down mode continues while CKE remains low. When CKE goes high, the LPSDRAM exits the deep power down mode. Before executing deep power down, all banks must be precharged.



Deep power down entry command

Burst stop command (/CS = /WE = Low, /RAS, /CAS = High)

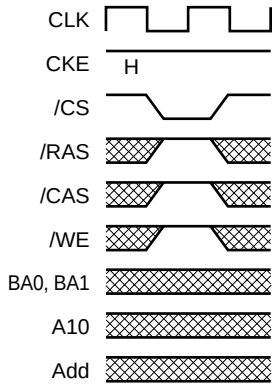
This command can stop the current burst operation.



Burst stop command

No operation (/CS = Low, /RAS, /CAS, /WE = High)

This command is not an execution command. No operations begin or terminate by this command.



No operation

Truth Table

Command Truth Table

Function	Symbol	CKE n – 1	CKE n	/CS	/RAS	/CAS	/WE	BA1	BA0	A10	A11, A12, A9 - A0
Device deselect	DESL	H	×	H	×	×	×	×	×	×	×
No operation	NOP	H	×	L	H	H	H	×	×	×	×
Burst stop	BST	H	H	L	H	H	L	×	×	×	×
Read	READ	H	×	L	H	L	H	V	V	L	V
Read with auto precharge	READA	H	×	L	H	L	H	V	V	H	V
Write	WRIT	H	×	L	H	L	L	V	V	L	V
Write with auto precharge	WRITA	H	×	L	H	L	L	V	V	H	V
Bank activate	ACT	H	×	L	L	H	H	V	V	V	V
Precharge select bank	PRE	H	×	L	L	H	L	V	V	L	×
Precharge all banks	PALL	H	×	L	L	H	L	×	×	H	×
Mode register set	MRS	H	×	L	L	L	L	L	L	L	V
Extended mode register set	EMRS	H	×	L	L	L	L	H	L	L	V

Remark: H: VIH. L: VIL. ×: VIH or VIL, V = Valid data

DQM Truth Table

Function	Symbol	CKE n – 1	CKE n	DQM 0	DQM 1	DQM 2	DQM 3
Data write / output enable	ENB	H	×	L	L	L	L
Data mask / output disable	MASK	H	×	H	H	H	H
DQ0 to DQ7 write enable/output enable	ENB0	H	×	L	×	×	×
DQ8 to DQ15 write enable/output enable	ENB1	H	×	×	L	×	×
DQ16 to DQ23 write enable/output enable	ENB2	H	×	×	×	L	×
DQ24 to DQ31 write enable/output enable	ENB3	H	×	×	×	×	L
DQ0 to DQ7 write inhibit/output disable	MASK0	H	×	H	×	×	×
DQ8 to DQ15 write inhibit/output disable	MASK 1	H	×	×	H	×	×
DQ16 to DQ23 write inhibit/output disable	MASK 2	H	×	×	×	H	×
DQ24 to DQ31 write inhibit/output disable	MASK 3	H	×	×	×	×	H

Remark: H: VIH. L: VIL. ×: VIH or VIL

CKE Truth Table

Current state	Function	Symbol	CKE n – 1	CKE n	/CS	/RAS	/CAS	/WE	Address
Activating	Clock suspend mode entry		H	L	×	×	×	×	×
Any	Clock suspend mode		L	L	×	×	×	×	×
Clock suspend	Clock suspend mode exit		L	H	×	×	×	×	×
Idle	Auto refresh command	REF	H	H	L	L	L	H	×
Idle	Self refresh entry	SELF	H	L	L	L	L	H	×
Idle	Power down entry	PD	H	L	L	H	H	H	×
			H	L	H	×	×	×	×
Idle	Deep power down entry	DPD	H	L	L	H	H	L	×
Self refresh	Self refresh exit		L	H	L	H	H	H	×
			L	H	H	×	×	×	×
Power down	Power down exit		L	H	L	H	H	H	×
			L	H	H	×	×	×	×
Deep power down	Deep power down exit		L	H	×	×	×	×	×

Remark: H: VIH. L: VIL. ×: VIH or VIL

Function Truth Table

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Idle	H	×	×	×	×	DESL	Nop	
	L	H	H	H	×	NOP	Nop	
	L	H	H	L	×	BST	Nop	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	→ Row activating	
	L	L	H	L	BA, A10	PRE/PALL	Nop	
	L	L	L	H	×	REF	Auto refresh	
	L	L	L	L	OC, BA1= L	MRS	Mode register set	
	L	L	L	L	OC, BA1= H	EMRS	Extended mode register set	
Row active	H	×	×	×	×	DESL	Nop	
	L	H	H	H	×	NOP	Nop	
	L	H	H	L	×	BST	Nop	
	L	H	L	H	BA, CA, A10	READ/READA	Begin read	3
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	Begin write	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	Precharge/Precharge all banks	4
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Read	H	×	×	×	×	DESL	Continue burst to end → Row active	
	L	H	H	H	×	NOP	Continue burst to end → Row active	
	L	H	H	L	×	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Terminate burst, begin new read	5
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Terminate burst, begin write	5, 6
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst → Precharging	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Write	H	×	×	×	×	DESL	Continue burst to end → Write recovering	
	L	H	H	H	×	NOP	Continue burst to end → Write recovering	
	L	H	H	L	×	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Terminate burst, start read : Determine AP	5, 6
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Terminate burst, new write : Determine AP	5
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst → Precharging	7
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Read with auto precharge	H	×	×	×	×	DESL	Continue burst to end → Precharging	
	L	H	H	H	×	NOP	Continue burst to end → Precharging	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Write with auto precharge	H	×	×	×	×	DESL	Continue burst to end → Write recovering with auto precharge	
	L	H	H	H	×	NOP	Continue burst to end → Write recovering with auto precharge	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Precharging	H	×	×	×	×	DESL	Nop → Enter idle after tRP	
	L	H	H	H	×	NOP	Nop → Enter idle after tRP	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	Nop → Enter idle after tRP	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Row activating	H	×	×	×	×	DESL	Nop → Enter bank active after tRCD	
	L	H	H	H	×	NOP	Nop → Enter bank active after tRCD	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2, 8
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	

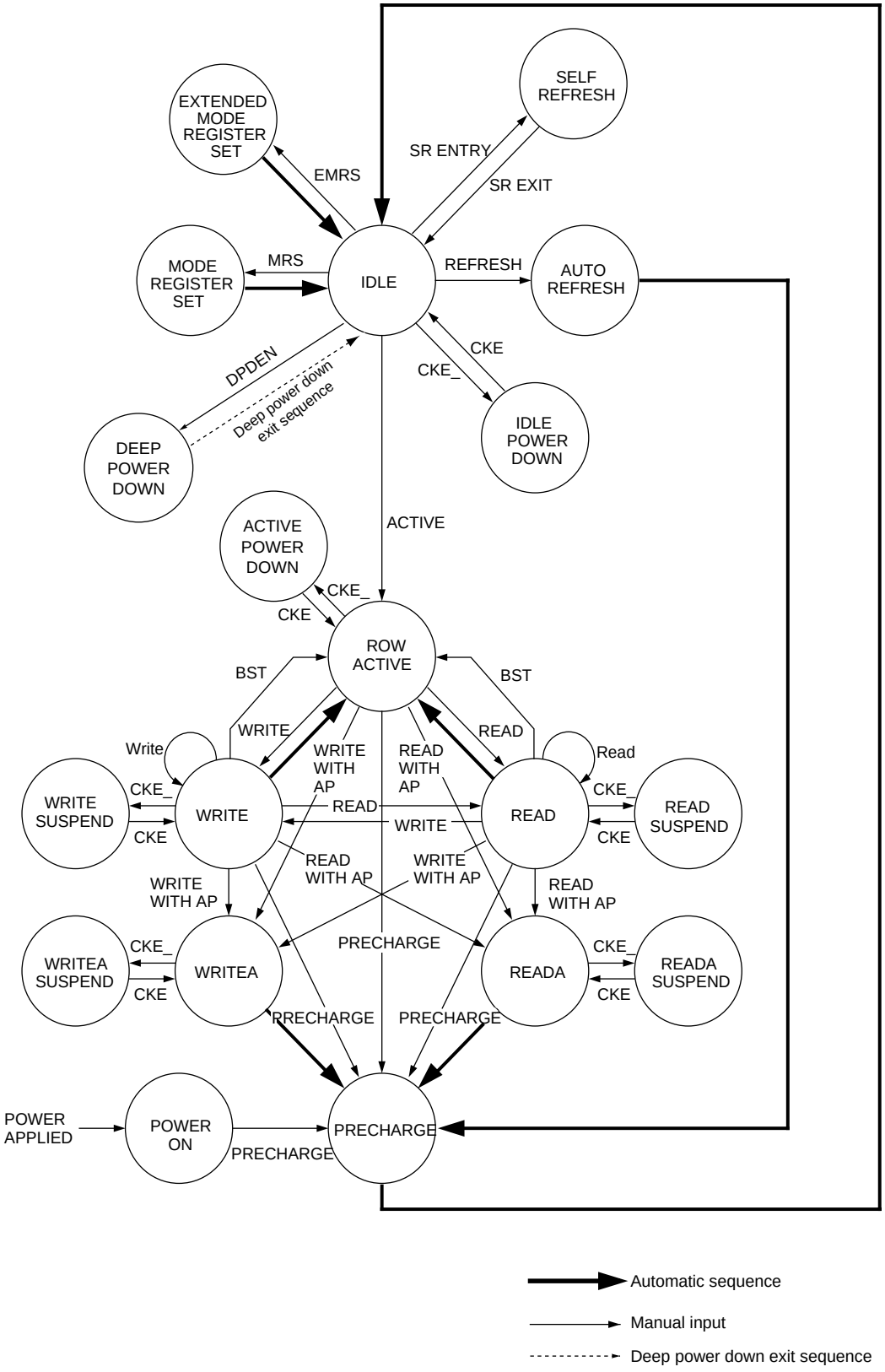
Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Write recovering	H	×	×	×	×	DESL	Nop → Enter row active after tDPL	
	L	H	H	H	×	NOP	Nop → Enter row active after tDPL	
	L	H	H	L	×	BST	Nop → Enter row active after tDPL	
	L	H	L	H	BA, CA, A10	READ/READA	Begin read	6
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	Begin new write	
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Write recovering	H	×	×	×	×	DESL	Nop → Enter precharge after tDPL	
with auto	L	H	H	H	×	NOP	Nop → Enter precharge after tDPL	
precharge	L	H	H	L	×	BST	Nop → Enter precharge after tDPL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	2, 6
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Refresh	H	×	×	×	×	DESL	Nop → Enter idle after tRC1	
	L	H	H	H	×	NOP	Nop → Enter idle after tRC1	
	L	H	H	L	×	BST	Nop → Enter idle after tRC1	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Mode register	H	×	×	×	×	DESL	Nop → Enter idle after tRSC	
accessing	L	H	H	H	×	NOP	Nop → Enter idle after tRSC	
	L	H	H	L	×	BST	Nop → Enter idle after tRSC	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Extended mode	H	×	×	×	×	DESL	Nop → Enter idle after tRSC	
register	L	H	H	H	×	NOP	Nop → Enter idle after tRSC	
accessing	L	H	H	L	×	BST	Nop → Enter idle after tRSC	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA0,BA1	MRS/EMRS	ILLEGAL	

Remark: H: VIH. L: VIL. ×: VIH or VIL, V = Valid data
BA: Bank Address, CA: Column Address, RA: Row Address, OC: Op-Code

Notes: 1. All entries assume that CKE is active (CKE_{n-1}=CKE_n=H).
2. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
3. Illegal if tRCD is not satisfied.
4. Illegal if tRAS is not satisfied.
5. Must satisfy burst interrupt condition.
6. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
7. Must mask preceding data which don't satisfy tDPL.
8. Illegal if tRRD is not satisfied.

Simplified State Diagram



Initialization

The synchronous DRAM is initialized in the power-on sequence according to the following.

(1) To stabilize internal circuits, when power is applied, a 200 μs or longer pause must precede any signal toggling.

(2) After the pause, all banks must be precharged using the Precharge command (The Precharge all banks command is convenient).

(3) Once the precharge is completed and the minimum tRP is satisfied, two or more Auto refresh must be performed.

(4) Both the mode register and the extended mode register must be programmed. After the mode register set cycle or the extended mode register set cycle, tRSC (2 CLK minimum) pause must be satisfied.

Remarks:

1 The sequence of Auto refresh, mode register programming and extended mode register programming above may be transposed.

2 CKE and DQM must be held high until the Precharge command is issued to ensure data-bus High-Z.

Programming Mode Registers

The mode register and extended mode register are programmed by the Mode register set command and Extended mode register command, respectively using address bits A12 through A0, BA0 and BA1 as data inputs. The registers retain data until they are re-programmed, or the device enters into the deep power down or the device loses power.

Mode register

The mode register has three fields;

Options	:	A12 through A7
/CAS latency	:	A6 through A4
Wrap type	:	A3
Burst length	:	A2 through A0

Following mode register programming, no command can be issued before at least 2 CLK have elapsed.

/CAS Latency

/CAS latency is the most critical of the parameters being set. It tells the device how many clocks must elapse before the data will be available. The value is determined by the frequency of the clock and the speed grade of the device.

Burst Length

Burst Length is the number of words that will be output or input in a read or write cycle. After a read burst is completed, the output bus will become High-Z. The burst length is programmable as 1, 2, 4, 8 or full page.

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. This order is programmable as either “Sequential” or “Interleave”. The method chosen will depend on the type of CPU in the system.

Some microprocessor cache systems are optimized for sequential addressing and others for interleaved addressing. “Burst Length Sequence” shows the addressing sequence for each burst length using them. Both sequences support bursts of 1, 2, 4 and 8. Additionally, sequence supports the full page length.

Extended Mode Register

The extended mode register has four fields;

Options	: A12 through A7, A4, A3
Auto Temperature Compensated Self Refresh	: A9
Driver Strength	: A6 through A5
Partial Array Self Refresh	: A2 through A0

Following extended mode register programming, no command can be issued before at least 2 CLK have elapsed.

Drive Strength

By setting specific parameter on A6 and A5, driving capability of data output drivers is selected.

Auto Temperature Compensated Self Refresh (ATCSR)

With the built-in temperature sensor, the internal self refresh frequency is controlled autonomously.

Partial Array Self Refresh

Memory array size to be refreshed during self refresh operation is programmable in order to reduce power. Data outside the defined area will not be retained during self refresh.

Mode Register Definition

BA0	BA1	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	0	LTMODE			WT	BL			Mode Register Set

	Bits6-4	/CAS latency
Latency mode	000	R
	001	R
	010	2
	011	3
	100	R
	101	R
	110	R
	111	R

	Bits2-0	WT = 0	WT = 1
Burst length	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
	111	Full page	R

Wrap type	0	Sequential
	1	Interleave

BA0	BA1	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	1	0	0	0	ATCSR	0	0	DS		0	0	PASR			Extended Mode Register Set

	Bit9	ATCSR
ATCSR	0	Enable
	1	R

	Bits2-0	Refresh Array
Partial Array Self Refresh	000	All banks
	001	Bank A & Bank B (BA1=0)
	010	Bank A (BA0=BA1=0)
	011	R
	100	R
	101	R
	110	R
	111	R

	Bits6-5	Strength
Driver Strength	00	Normal
	01	1/2 strength
	10	1/4 strength
	11	1/8 strength

Remark R : Reserved

Burst Length and Sequence

[Burst of Two]

Starting address (Column address A0, binary)	Sequential addressing sequence (decimal)	Interleave addressing sequence (decimal)
0	0, 1	0, 1
1	1, 0	1, 0

[Burst of Four]

Starting address (Column address A1–A0, binary)	Sequential addressing sequence (decimal)	Interleave addressing sequence (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

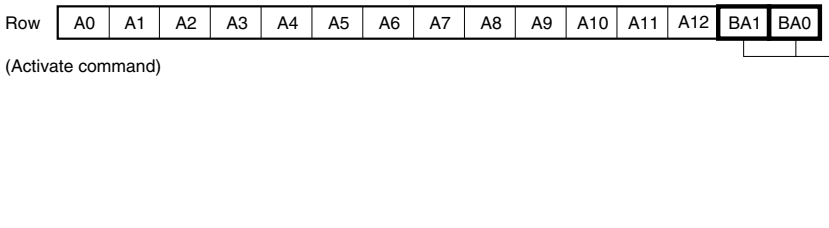
[Burst of Eight]

Full page burst is an extension of the above tables of sequential addressing, with the length being 512.

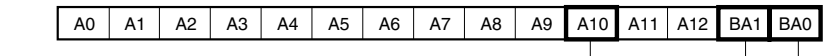
Starting address (Column address A2–A0, binary)	Sequential addressing sequence (decimal)	Interleave addressing sequence (decimal)
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Full page burst is an extension of the above tables of sequential addressing, with the length being 1024 (× 16 bits), 512 (× 32 bits).

Address Bits of Bank-Select and Precharge

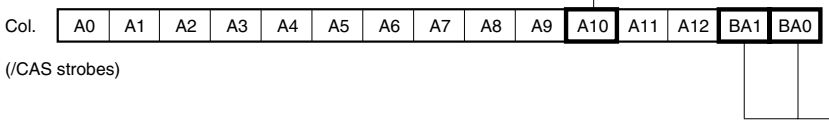


BA1	BA0	Result
0	0	**Select Bank A "Activate" command**
0	1	**Select Bank B "Activate" command**
1	0	**Select Bank C "Activate" command**
1	1	**Select Bank D "Activate" command**



A10	BA1	BA0	Result
0	0	0	**Precharge Bank A**
0	0	1	**Precharge Bank B**
0	1	0	**Precharge Bank C**
0	1	1	**Precharge Bank D**
1	x	x	**Precharge All Banks**

x : Don't care



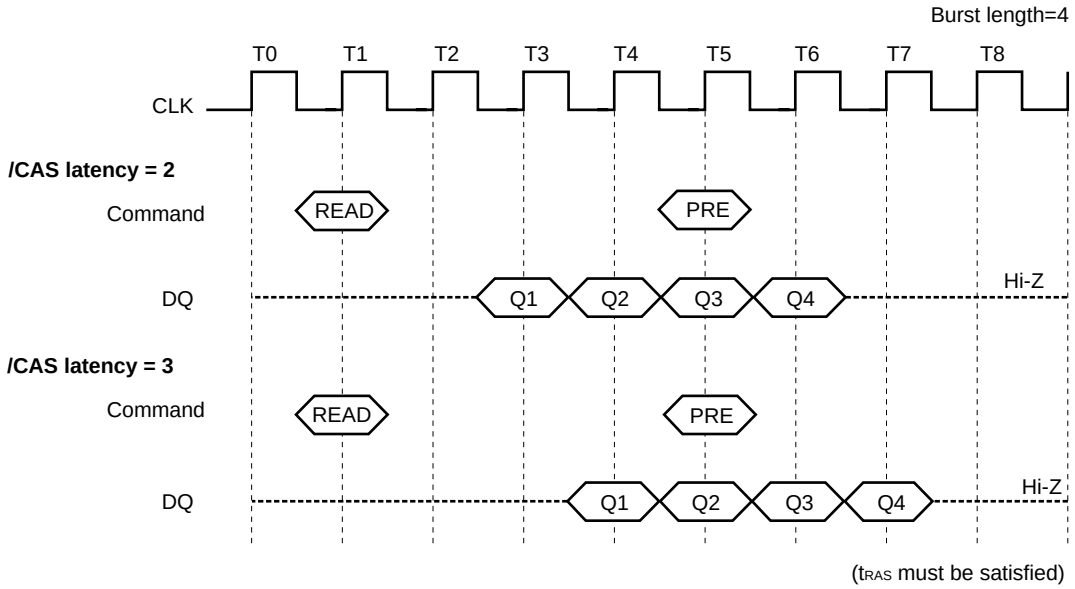
0	**disables Auto-Precharge (End of Burst)**
1	**enables Auto-Precharge (End of Burst)**

BA1	BA0	Result
0	0	**enables Read/Write commands for Bank A**
0	1	**enables Read/Write commands for Bank B**
1	0	**enables Read/Write commands for Bank C**
1	1	**enables Read/Write commands for Bank D**

Operation

Precharge

The precharge command can be issued anytime after tRAS min. is satisfied. Soon after the precharge command is issued, precharge operation performed and the synchronous DRAM enters the idle state after tRP is satisfied. The parameter tRP is the time required to perform the precharge. The earliest timing in a read cycle that a precharge command can be issued without losing any data in the burst is as follows.



Precharge

In order to write all data to the memory cell correctly, the asynchronous parameter tDPL must be satisfied. The tDPL (min.) specification defines the earliest time that a precharge command can be issued. Minimum number of clocks is calculated by dividing tDPL (min.) with clock cycle time. In summary, the precharge command can be issued relative to reference clock that indicates the last data word is valid. In the following table, minus means clocks before the reference; plus means time after the reference.

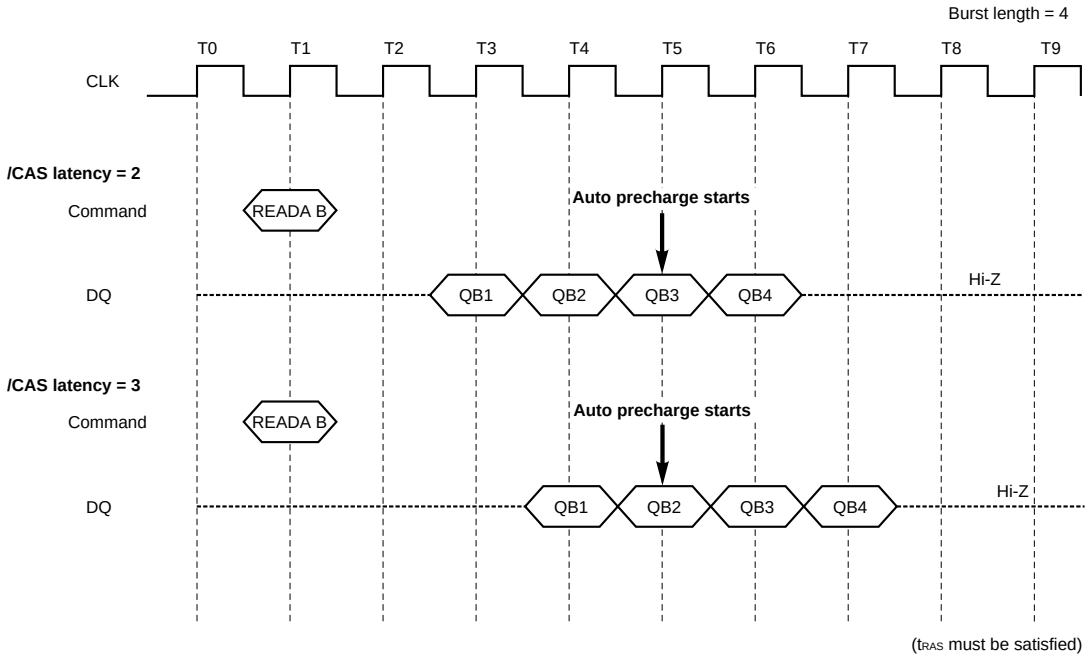
/CAS latency	Read	Write
2	-1	+tDPL(min.)
3	-2	+tDPL(min.)

Auto Precharge

During a read or write command cycle, A10 controls whether auto precharge is selected. A10 high in the Read or Write command (Read with Auto precharge command or Write with Auto precharge command), auto precharge is selected and begins automatically. The tRAS must be satisfied with a read with auto precharge or a write with auto precharge operation. In addition, the next activate command to the bank being precharged cannot be executed until the precharge cycle ends.
In read cycle, once auto precharge has started, an activate command to the bank can be issued after tRP has been satisfied.
In write cycle, the tDAL must be satisfied to issue the next activate command to the bank being precharged.
The timing that begins the auto precharge cycle depends on whether read or write cycle.

Read with Auto Precharge

During a read cycle, the auto precharge begins one clock earlier (/CAS latency of 2) or two clocks earlier (/CAS latency of 3) the last data word output.

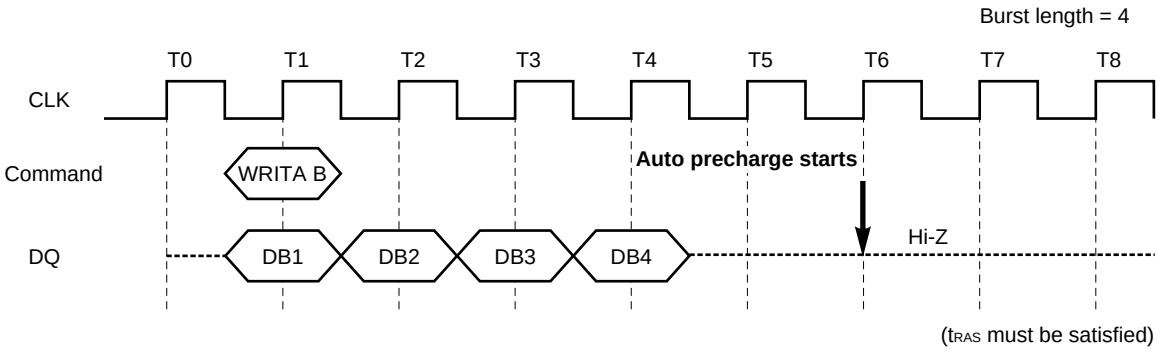


Read with Auto Precharge

Remark: READA means Read with Auto precharge

Write with Auto Precharge

During a write cycle, the auto precharge starts at the timing of 2 clocks after the last data word input to the device.



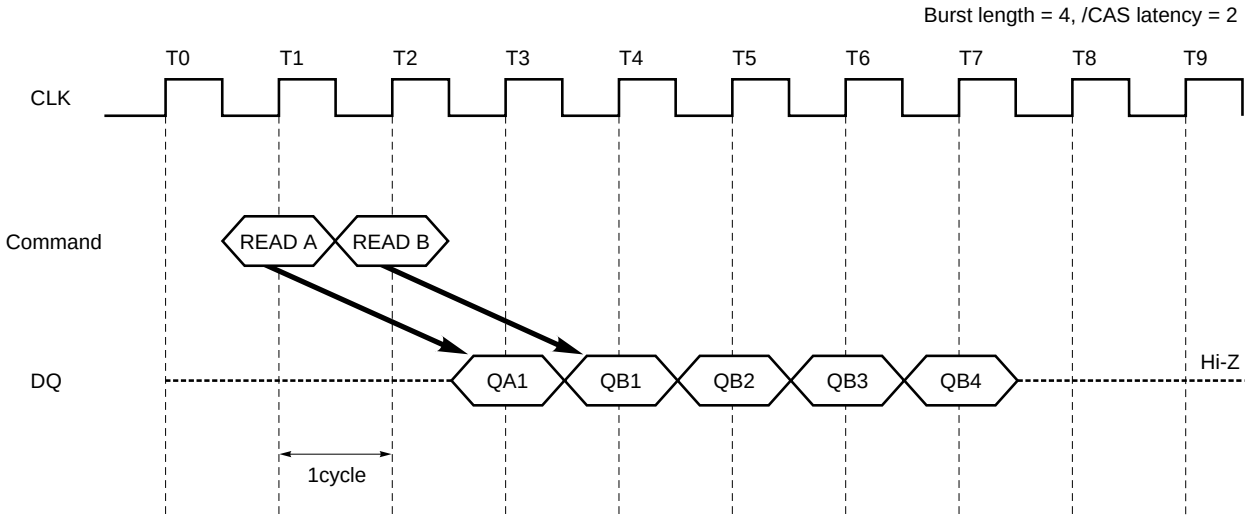
Write with Auto Precharge

Remark: WRITA means Write with Auto Precharge

Read / Write Command Interval

Read to Read Command Interval

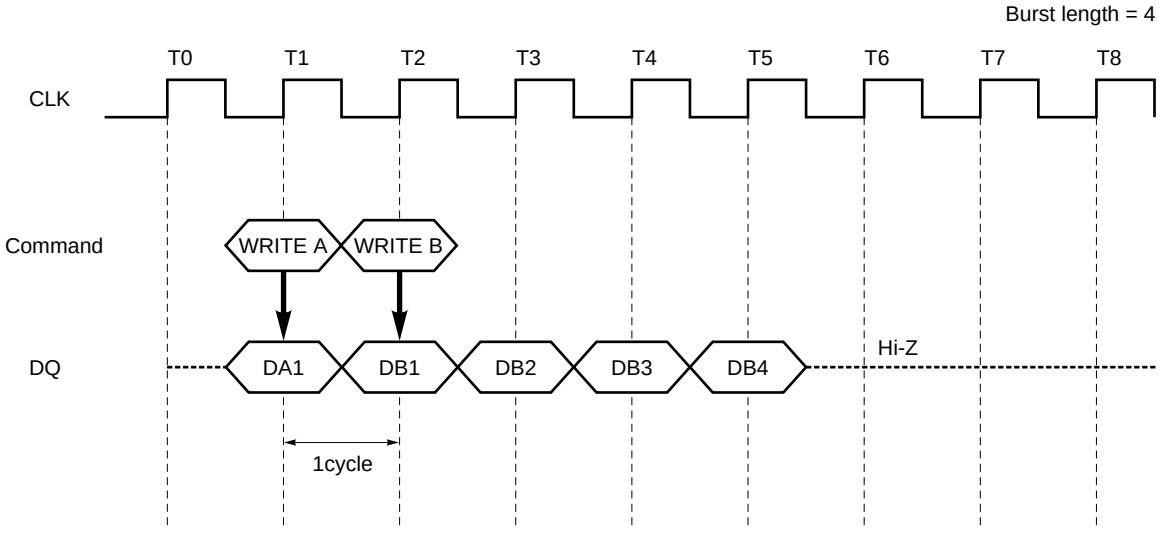
During a read cycle, when new Read command is issued, it will be effective after /CAS latency, even if the previous read operation does not completed. READ will be interrupted by another READ. The interval between the commands is 1 cycle minimum. Each Read command can be issued in every clock without any restriction.



Read to Read Command Interval

Write to Write Command Interval

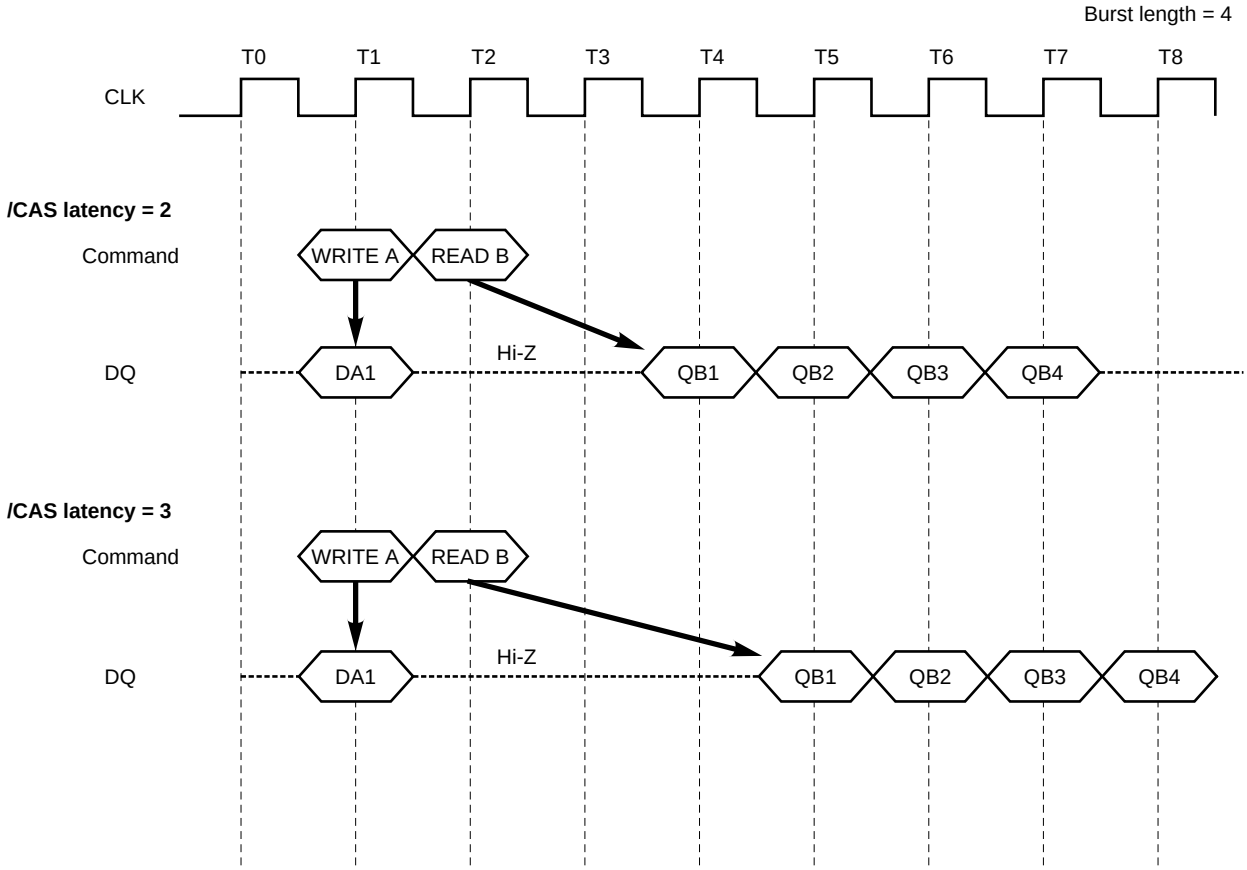
During a write cycle, when a new Write command is issued, the previous burst will terminate and the new burst will begin with a new Write command. WRITE will be interrupted by another WRITE. The interval between the commands is minimum 1 cycle. Each Write command can be issued in every clock without any restriction.



Write to Write Command Interval

Write to Read Command Interval

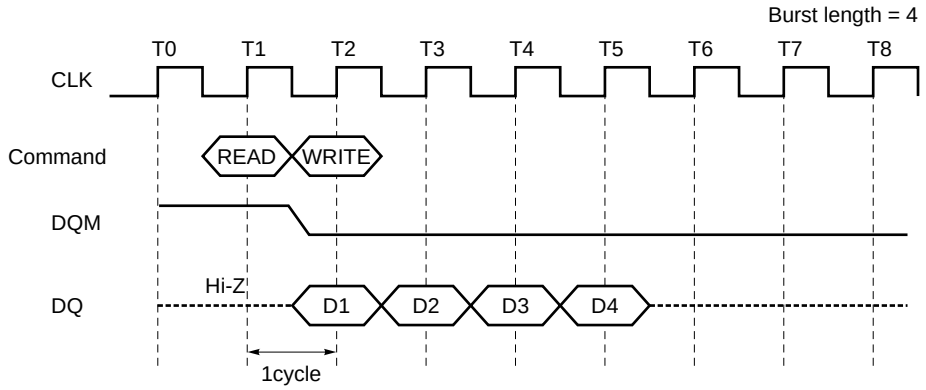
Write command and Read command interval is also 1 cycle. Only the write data before Read command will be written. The data bus must be High-Z at least one cycle prior to the first DOUT.



Write to Read Command Interval

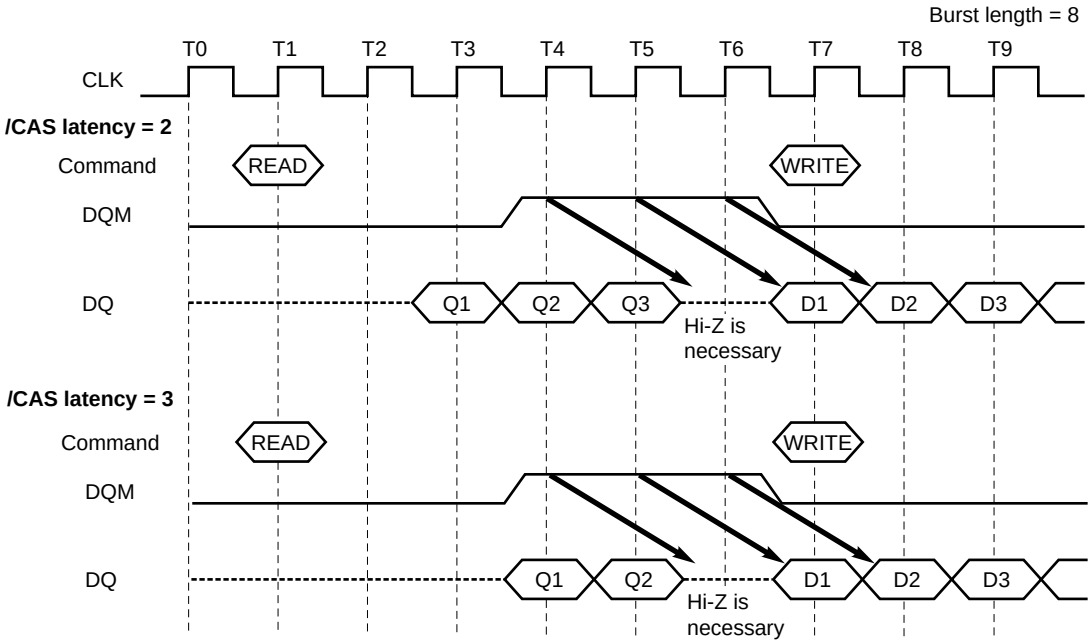
Read to Write Command Interval

During a read cycle, READ can be interrupted by WRITE. The Read and Write command interval is 1 cycle minimum. There is a restriction to avoid data conflict. The Data bus must be High-Z using DQM before WRITE.



Read to Write Command Interval 1

READ can be interrupted by WRITE. DQM must be High at least 3 clocks prior to the Write command.



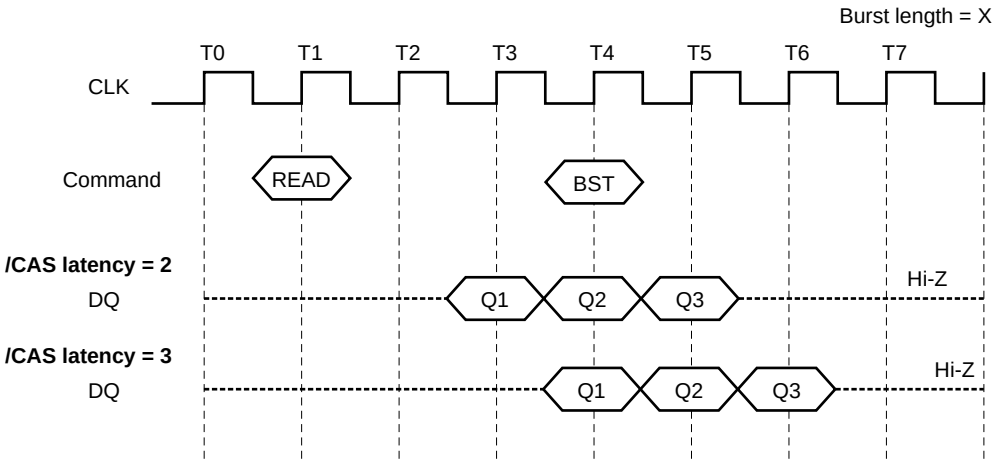
Read to Write Command Interval 2

Burst Termination

There are two methods to terminate a burst operation other than using a Read or a Write command. One is the burst stop command and the other is the precharge command.

Burst Termination in READ Cycle

During a read cycle, when the burst stop command is issued, the burst read data are terminated and the data bus goes to High-Z after the /CAS latency from the burst stop command.

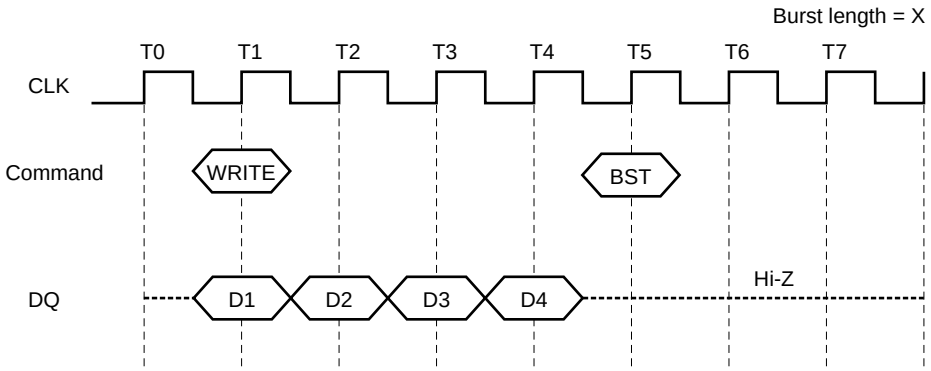


Burst Termination in READ Cycle

Remark: BST: Burst stop command

Burst Termination in WRITE Cycle

During a write cycle, when the burst stop command is issued, the burst write data are terminated and data bus goes to High-Z at the same clock with the burst stop command.



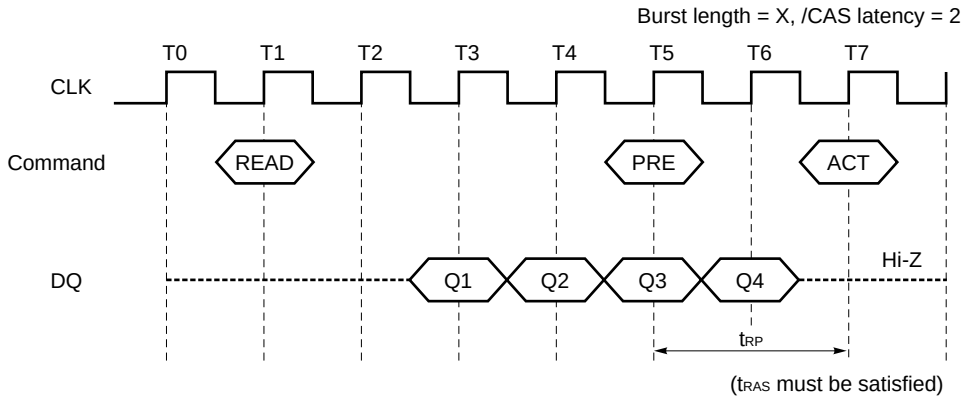
Burst Termination in WRITE Cycle

Remark: BST: Burst stop command

Precharge Termination in READ Cycle

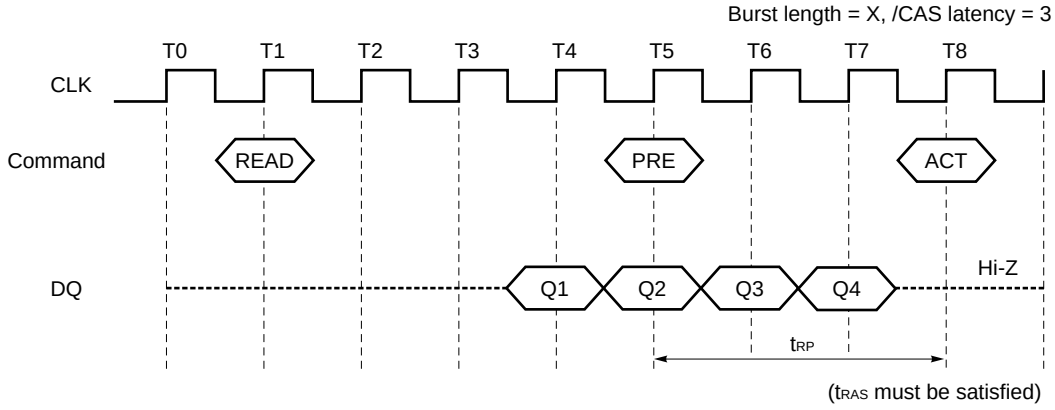
During a read cycle, the burst read operation is terminated by a precharge command. When the precharge command is issued, the burst read operation is terminated and precharge starts. The same bank can be activated again after tRP from the precharge command. To issue a precharge command, tRAS must be satisfied.

When /CAS latency is 2, the read data will remain valid until one clock after the precharge command.



Precharge Termination in READ Cycle (CL = 2)

When /CAS latency is 3, the read data will remain valid until two clocks after the precharge command.

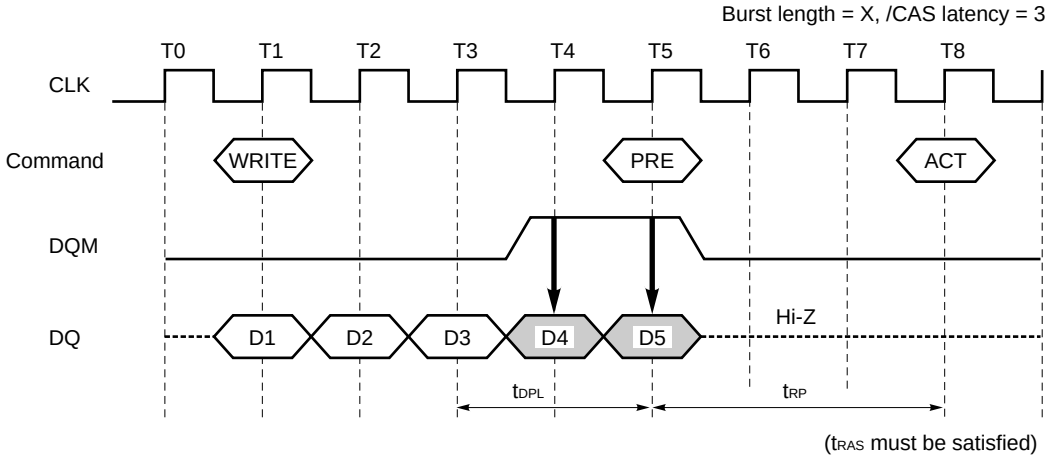


Precharge Termination in READ Cycle (CL = 3)

Precharge Termination in WRITE Cycle

During a write cycle, the burst write operation is terminated by a precharge command. When the precharge command is issued, the burst write operation is terminated and precharge starts. The same bank can be activated again after tRP from the precharge command. To issue a precharge command, tRAS must be satisfied.

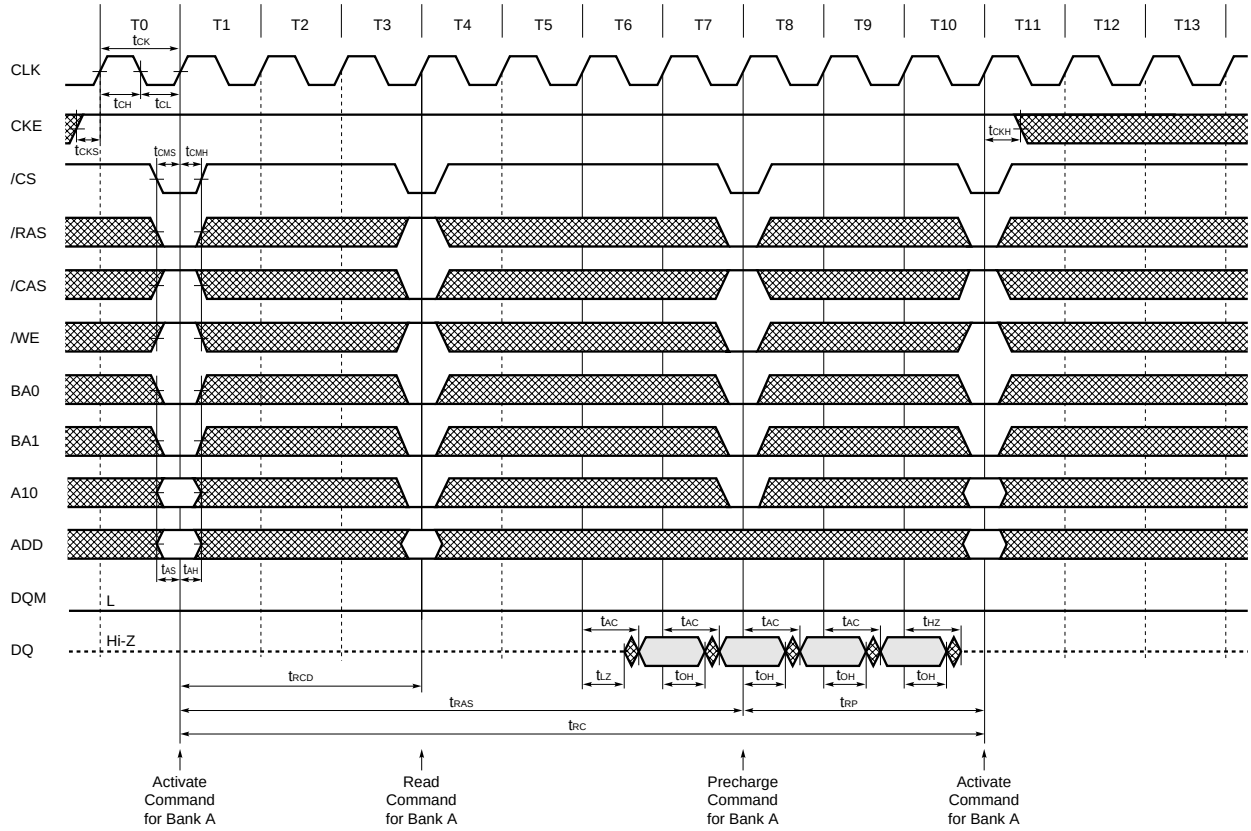
The write data written up to two clocks prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command and one clock before the precharge command. To prevent this from happening, DQM must be high and mask the invalid data.



Precharge Termination in WRITE Cycle

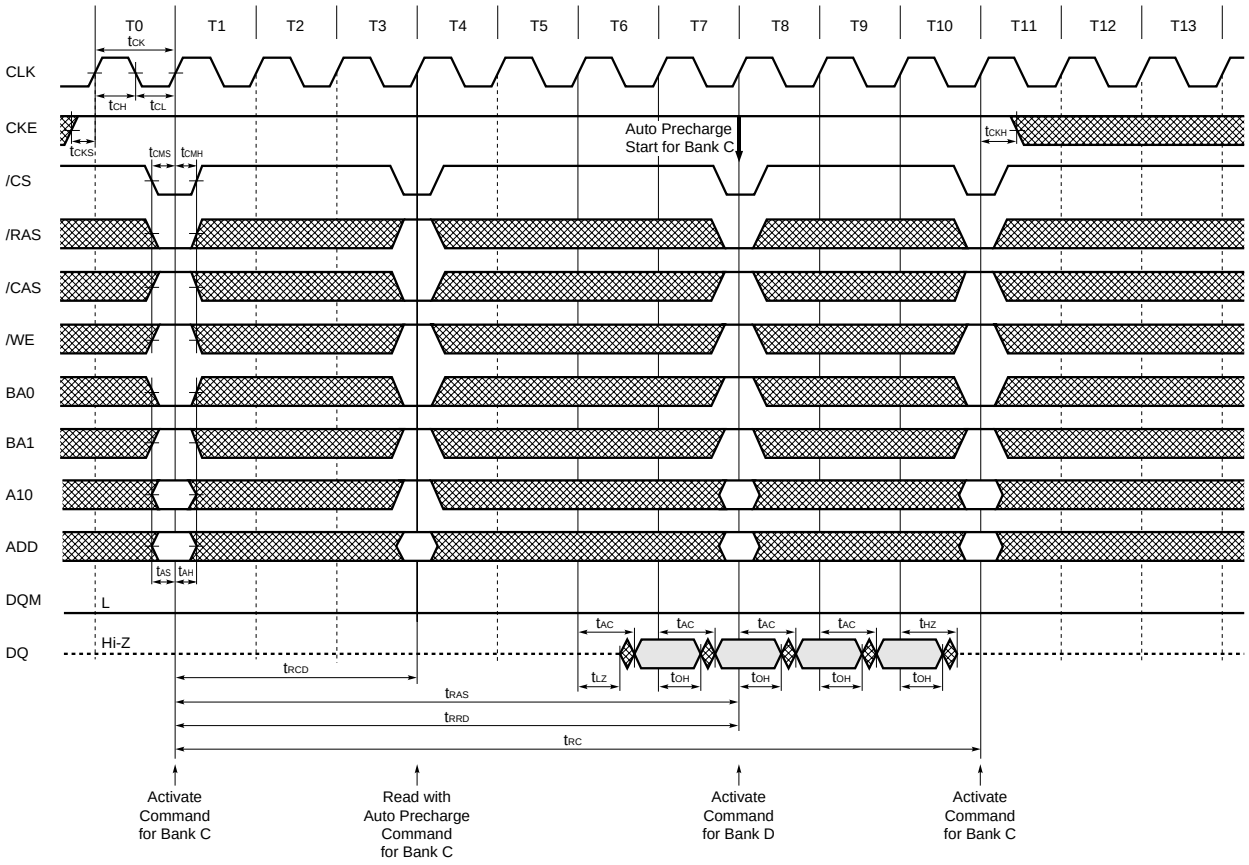
Timing Waveforms

AC Parameters for Read Timing with Manual Precharge



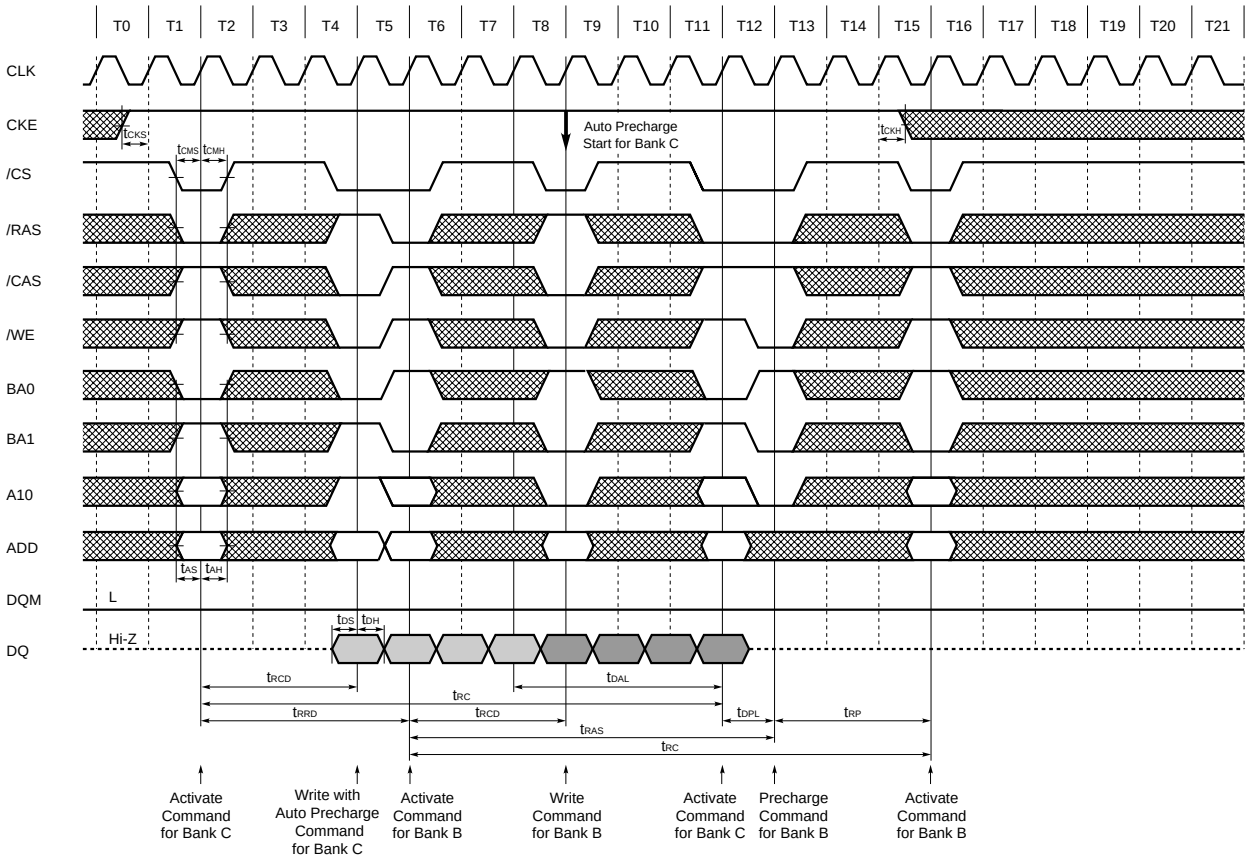
[Burst Length = 4, /CAS Latency = 3]

AC Parameters for Read Timing with Auto Precharge



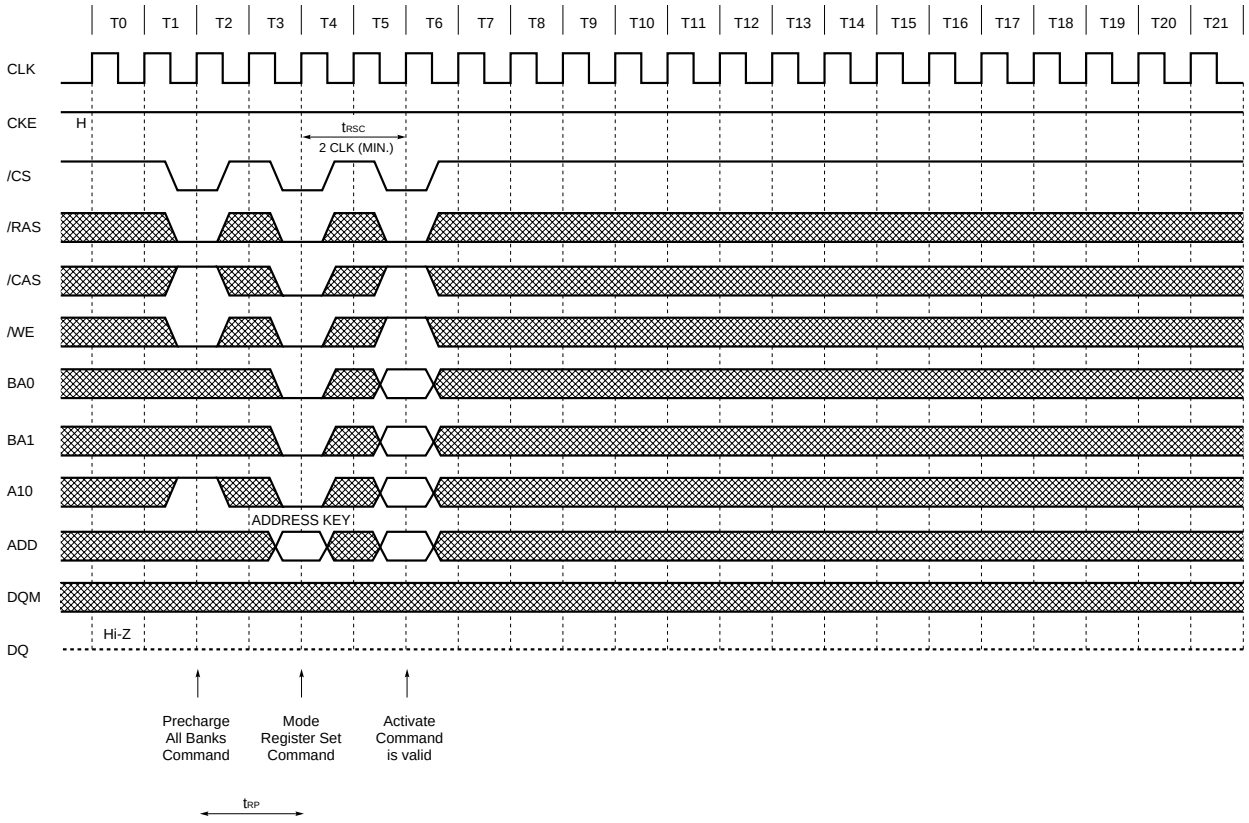
[Burst Length = 4, /CAS Latency = 3]

AC Parameters for Write Timing

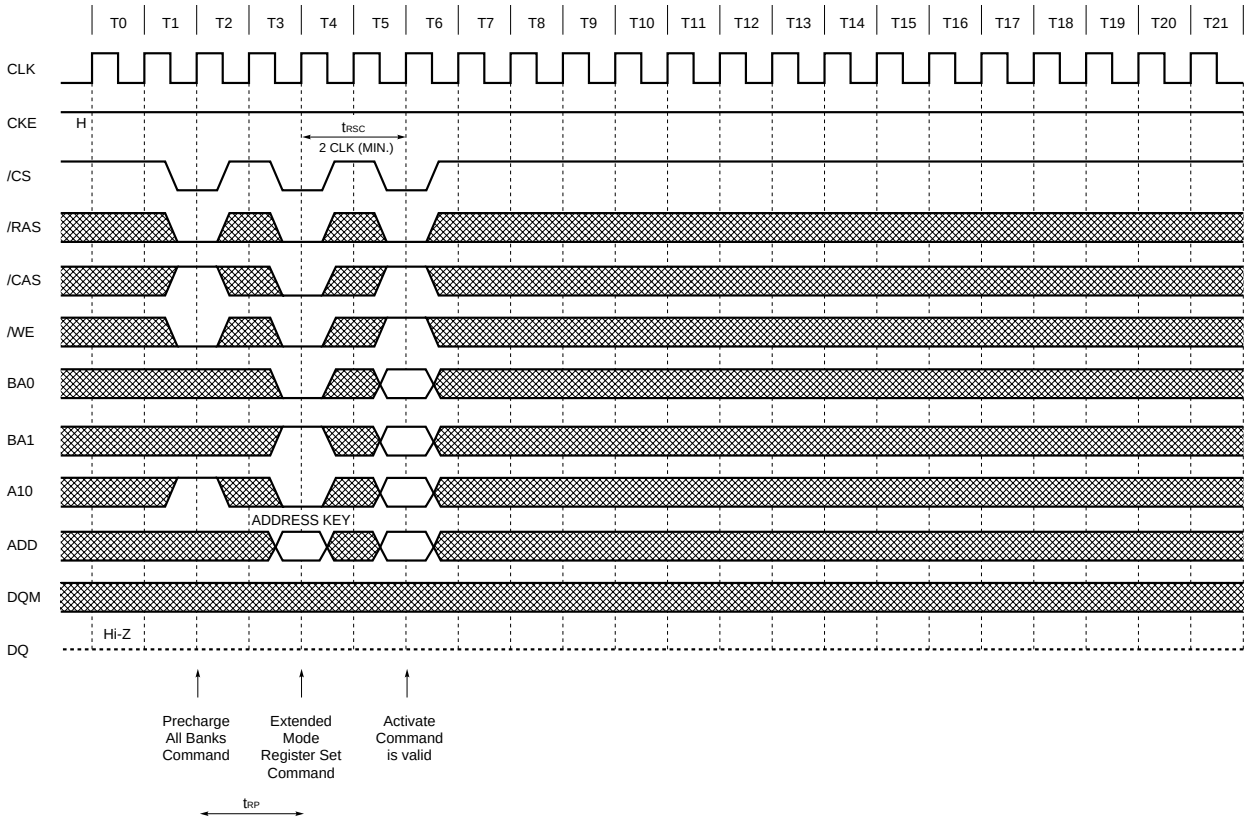


[Burst Length = 4]

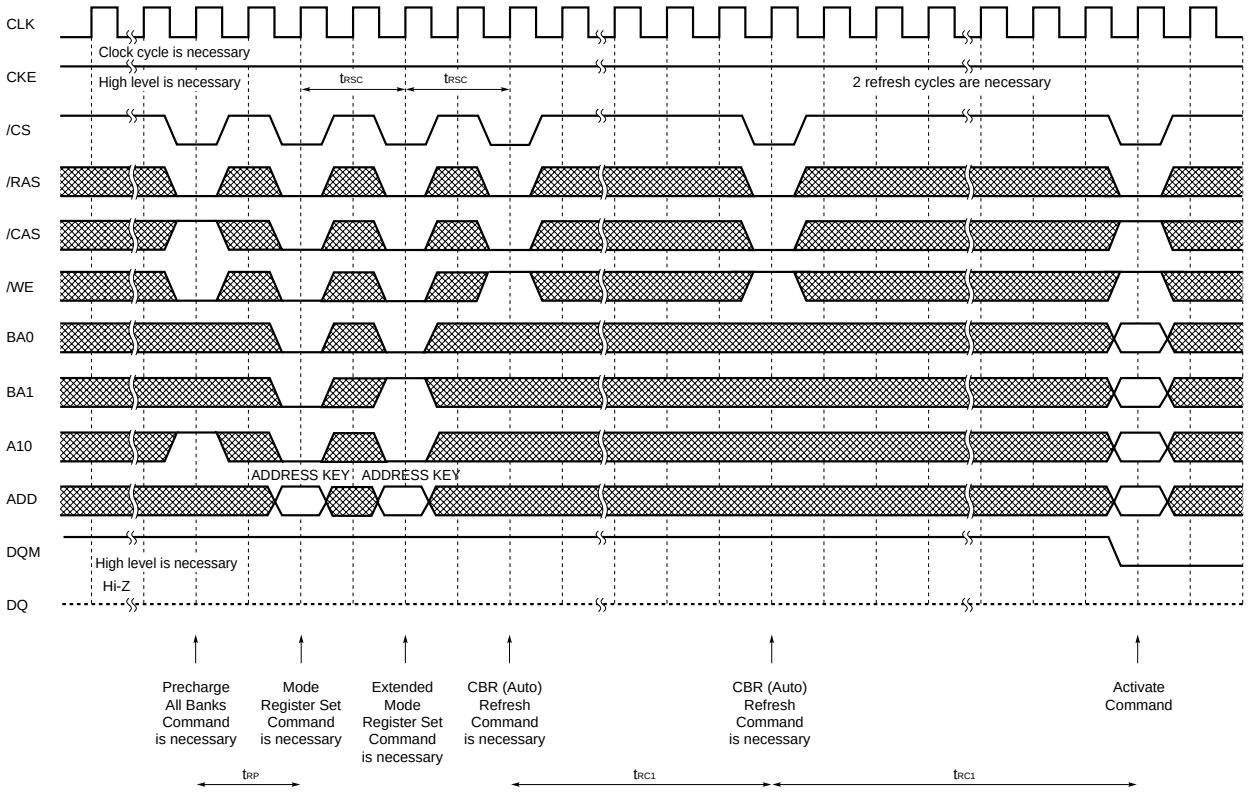
Mode Register Set



Extended Mode Register Set

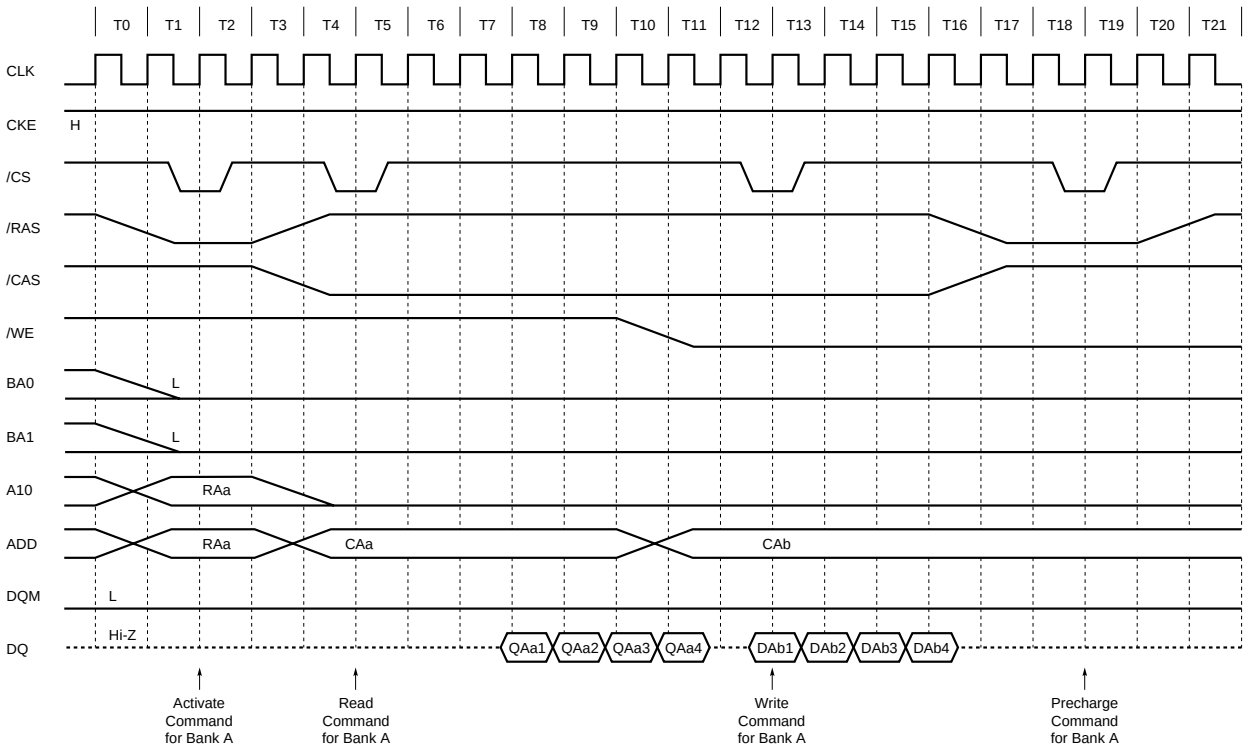


Power On Sequence



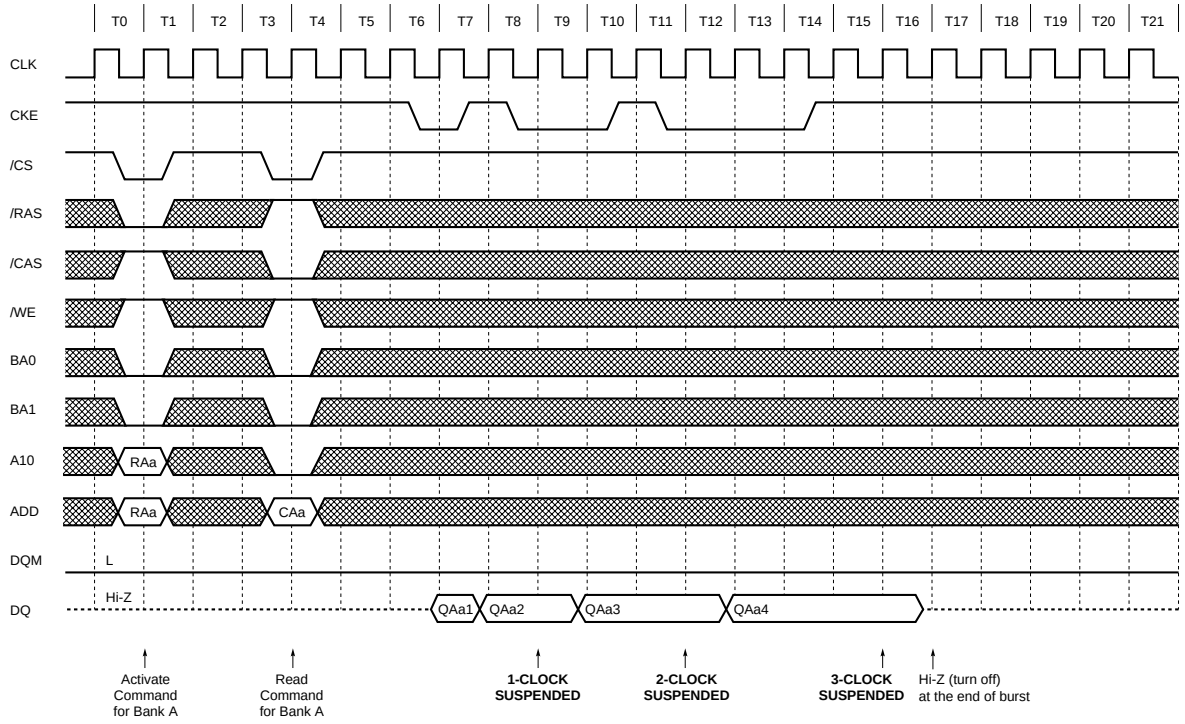
/CS Function

Only /CS signal needs to be issued at minimum rate

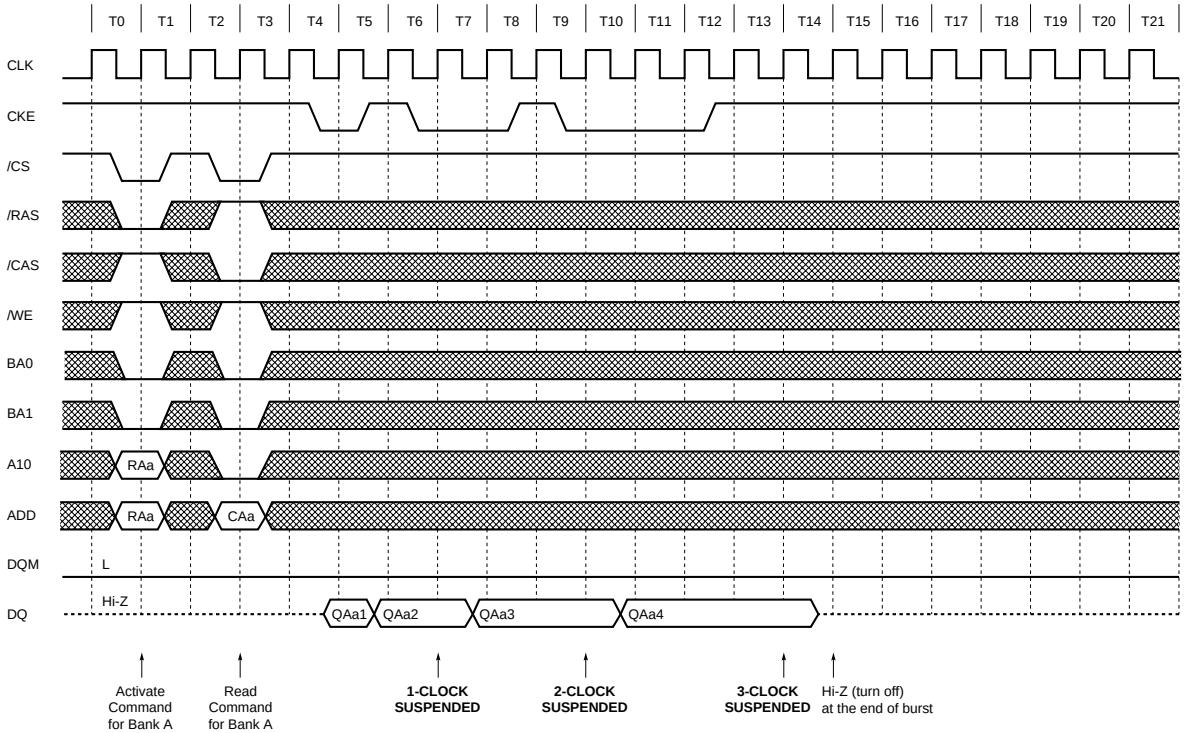


[Burst Length = 4, /CAS Latency = 3]

Clock Suspension during Burst Read

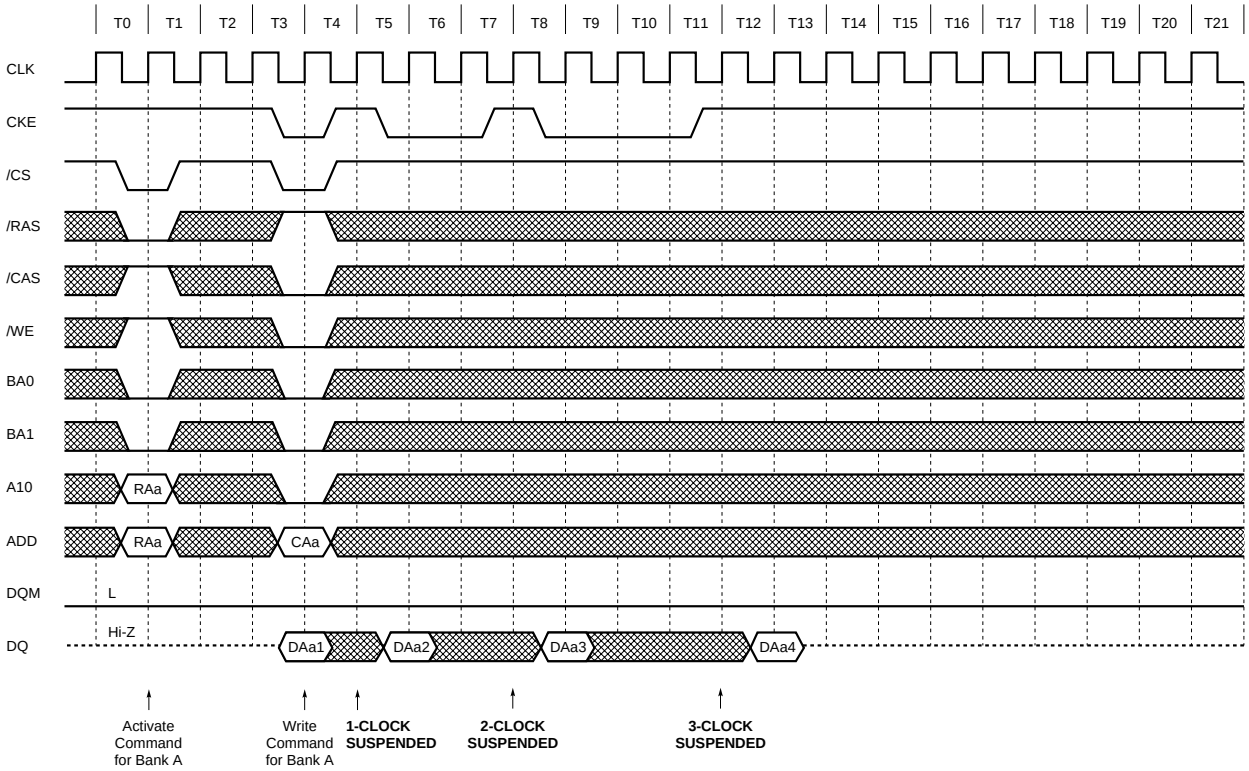


[Burst Length = 4, /CAS Latency = 3]

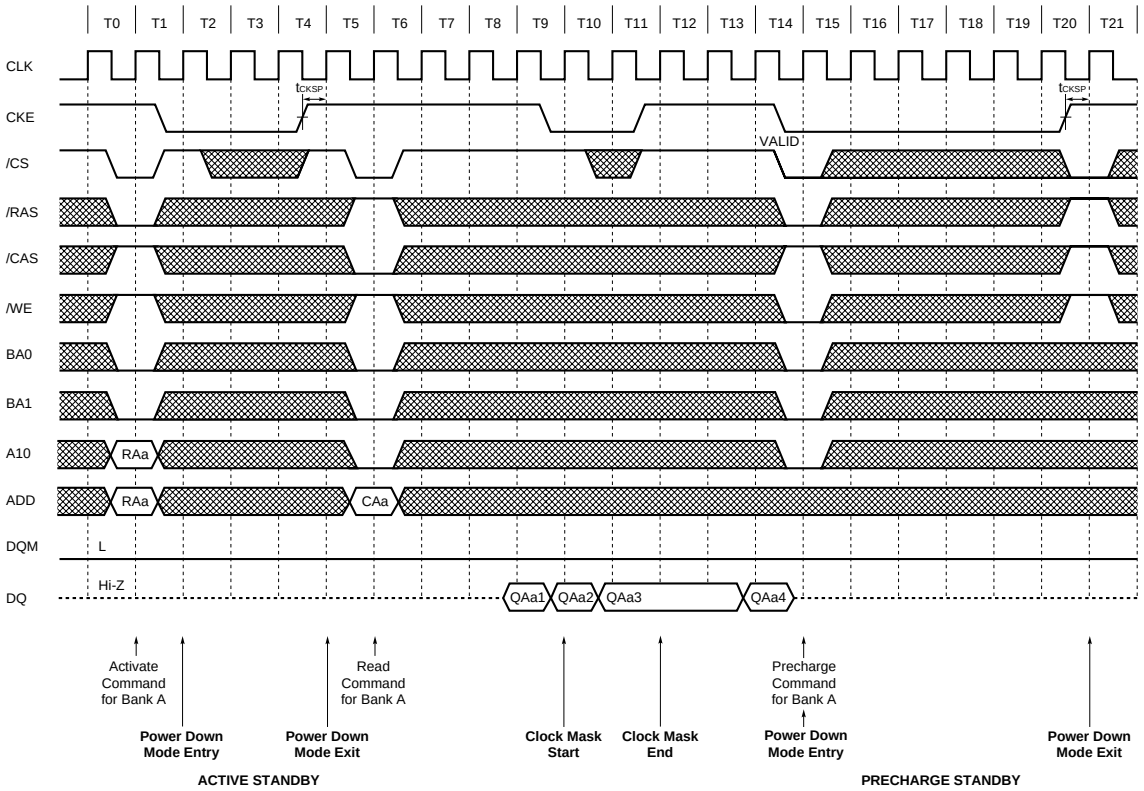


[Burst Length = 4, /CAS Latency = 2]

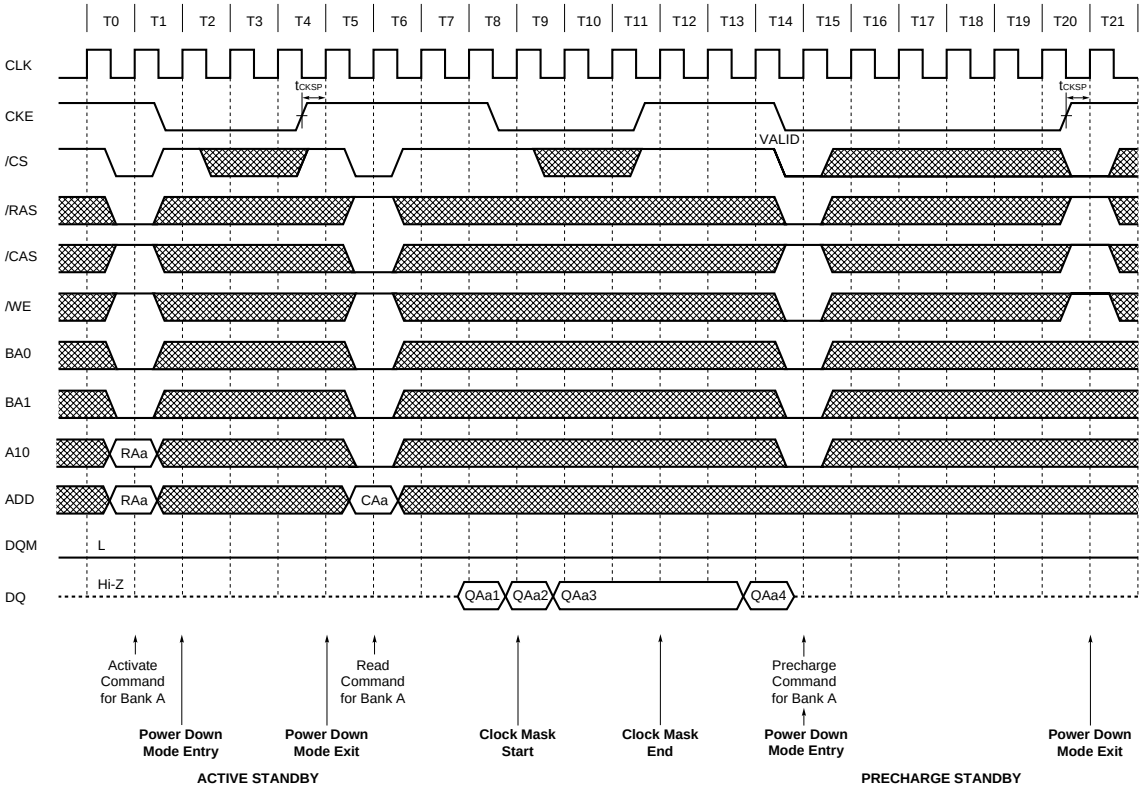
Clock Suspension during Burst Write



Power Down Mode and Clock Mask

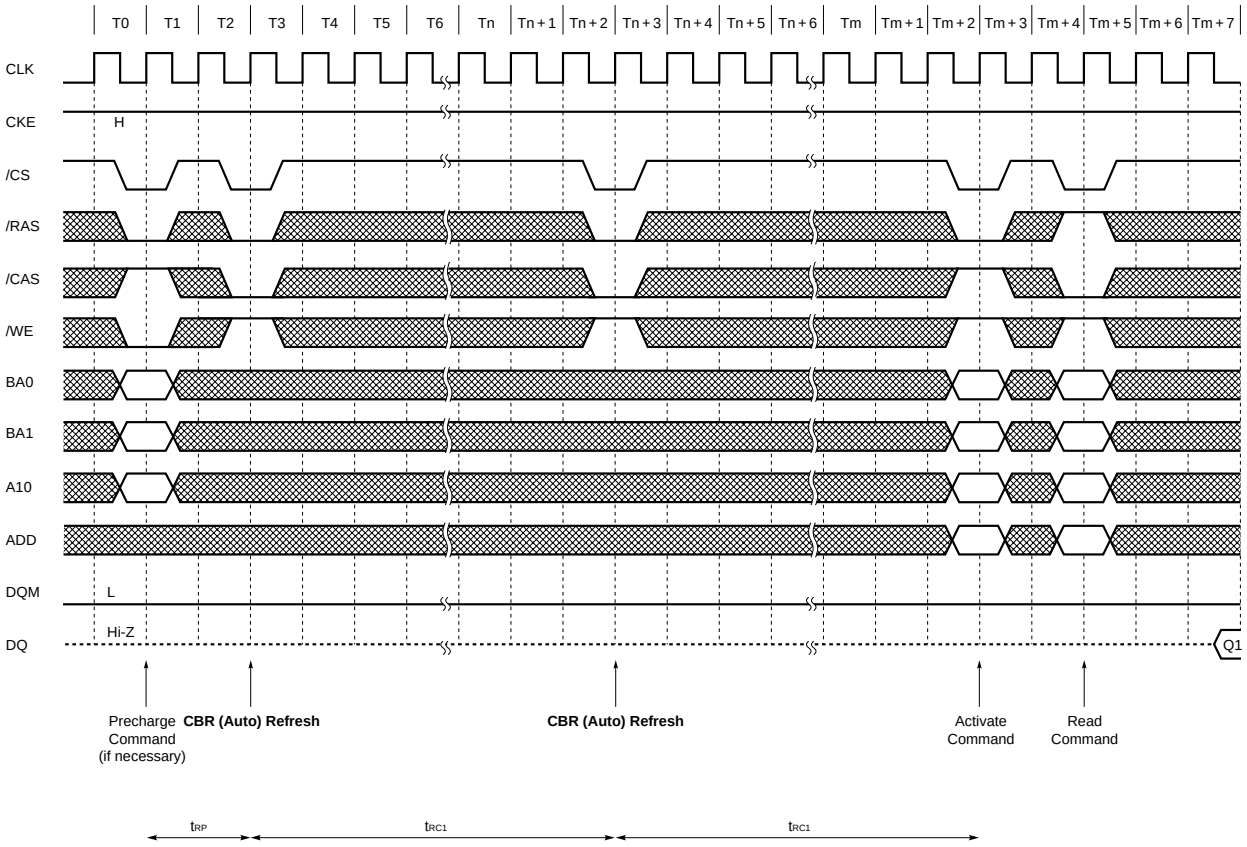


[Burst Length = 4, /CAS Latency = 3]

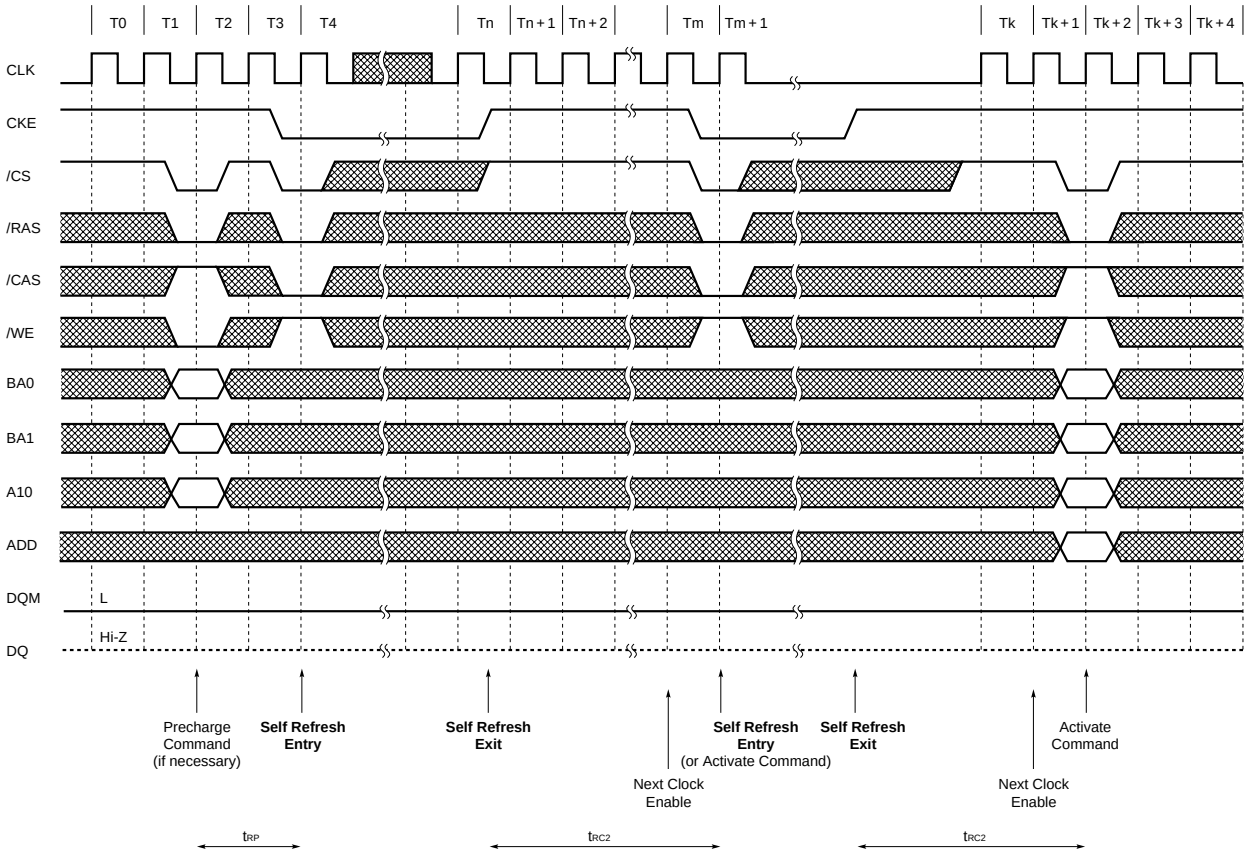


[Burst Length = 4, /CAS Latency = 2]

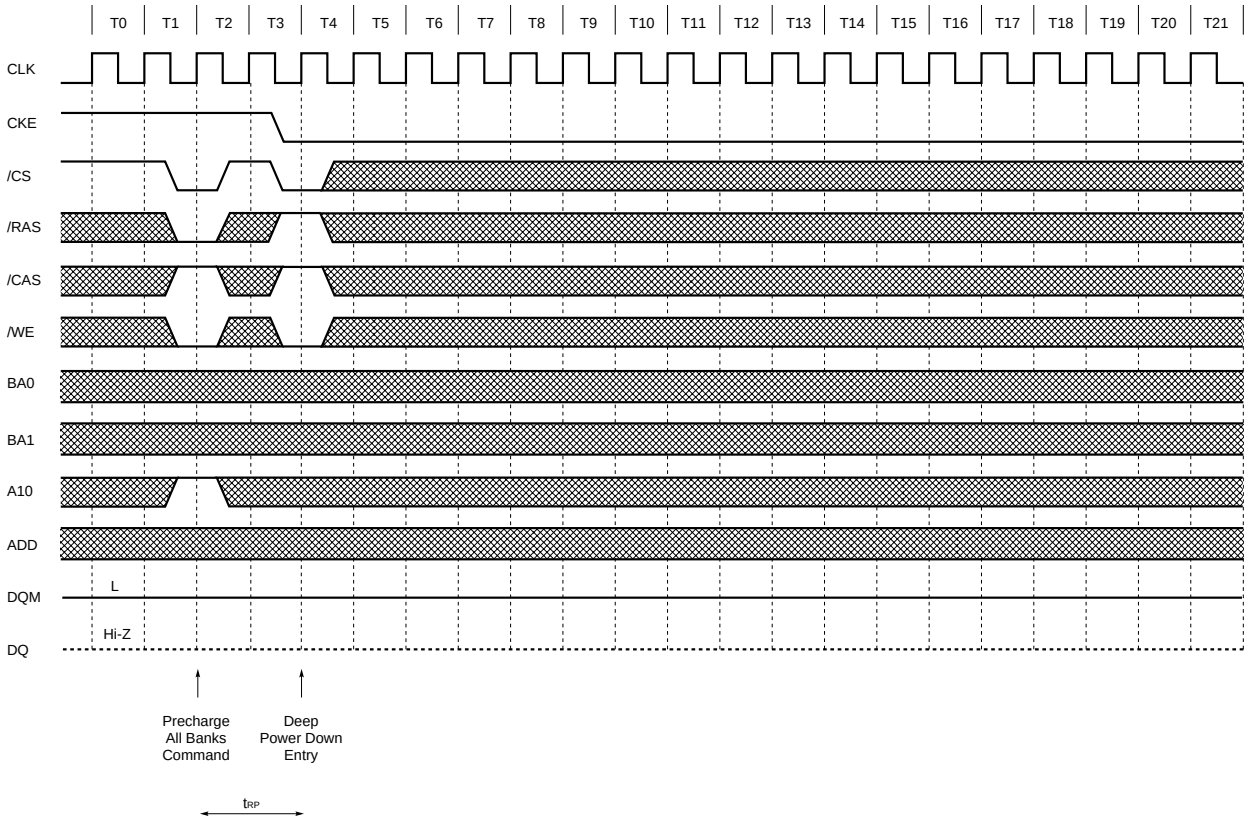
Auto Refresh



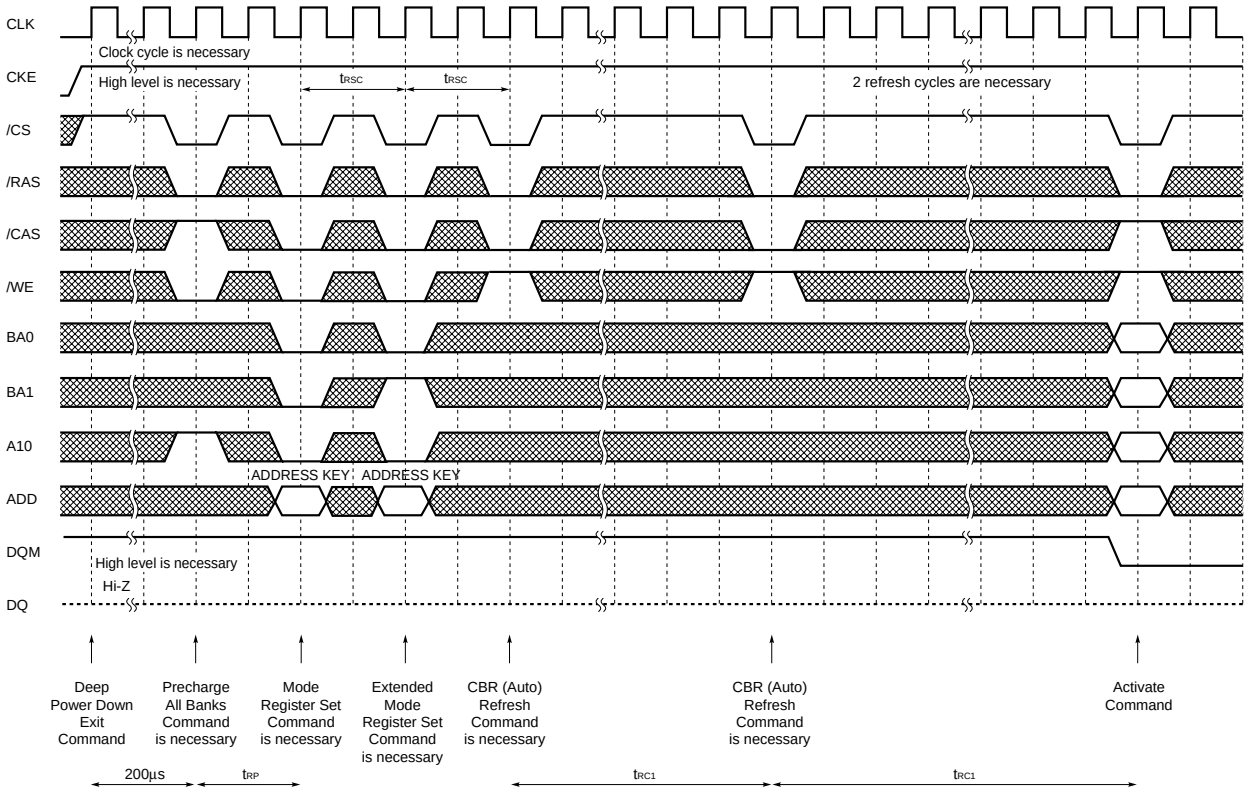
Self Refresh (Entry and Exit)



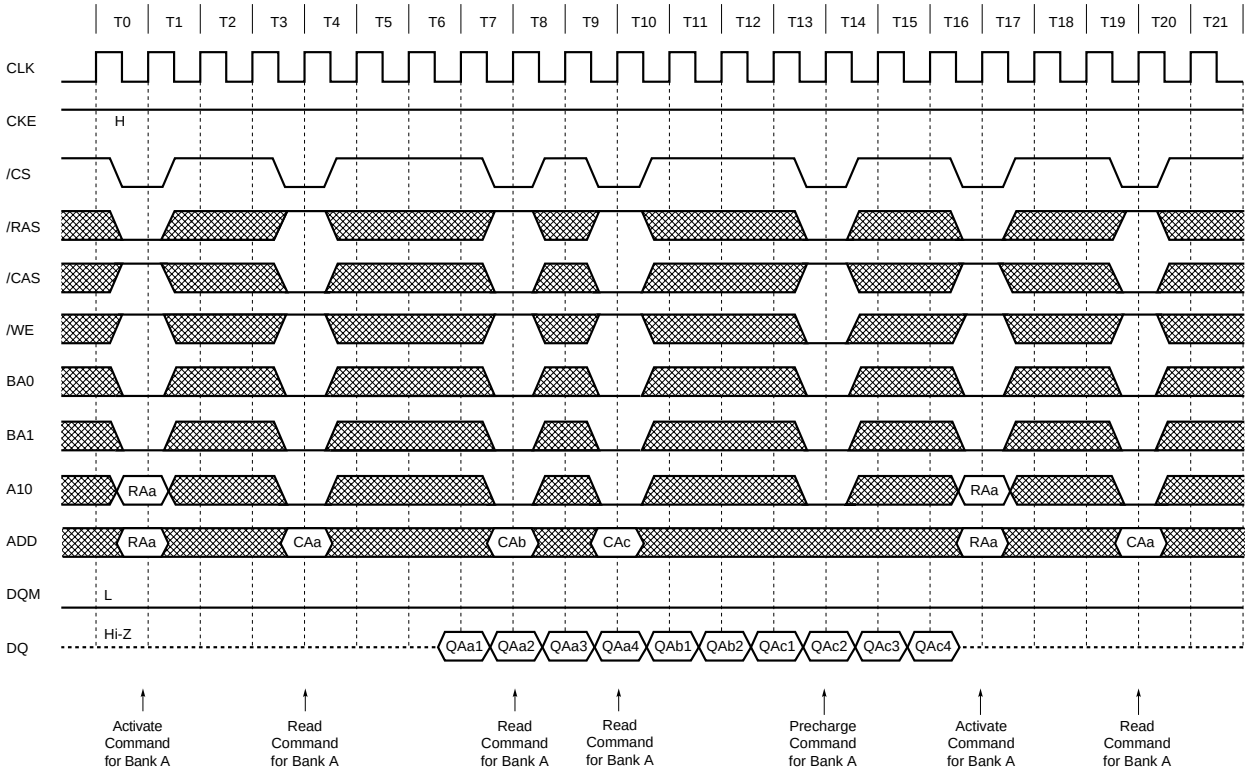
Deep Power Down Entry



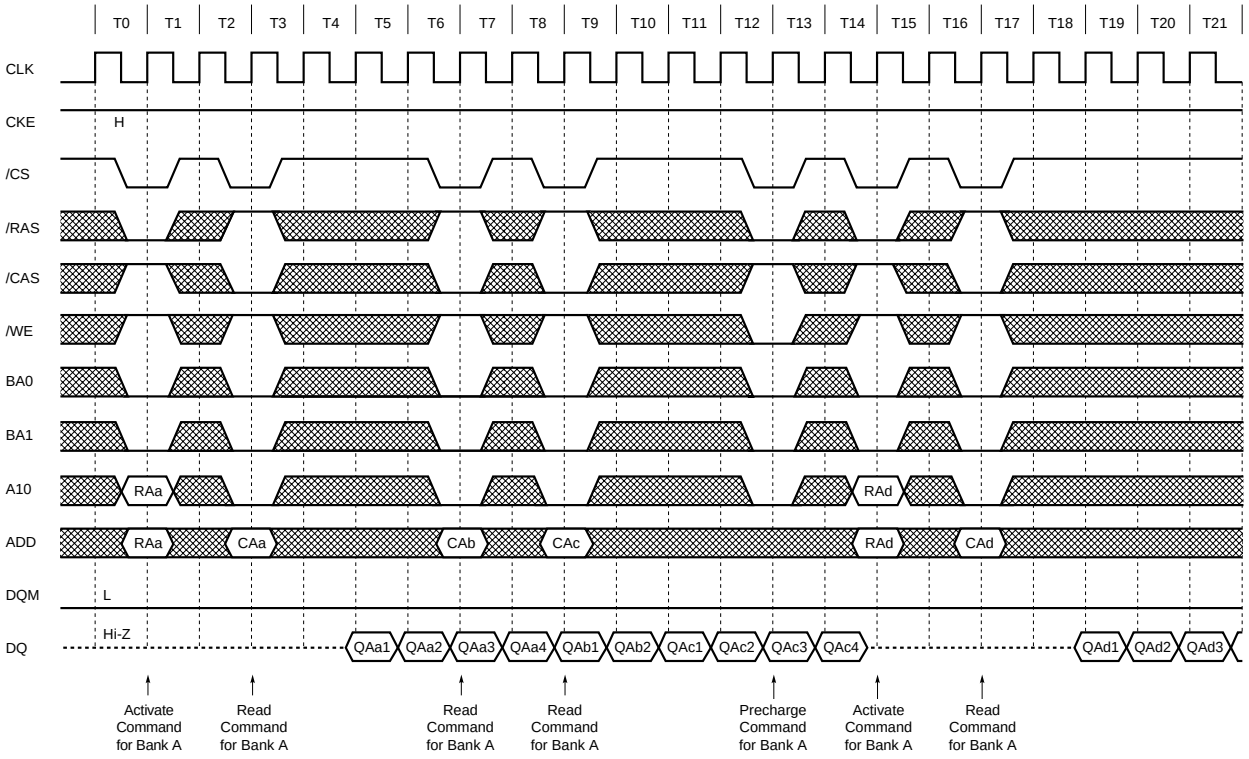
Deep Power Down Exit



Random Column Read

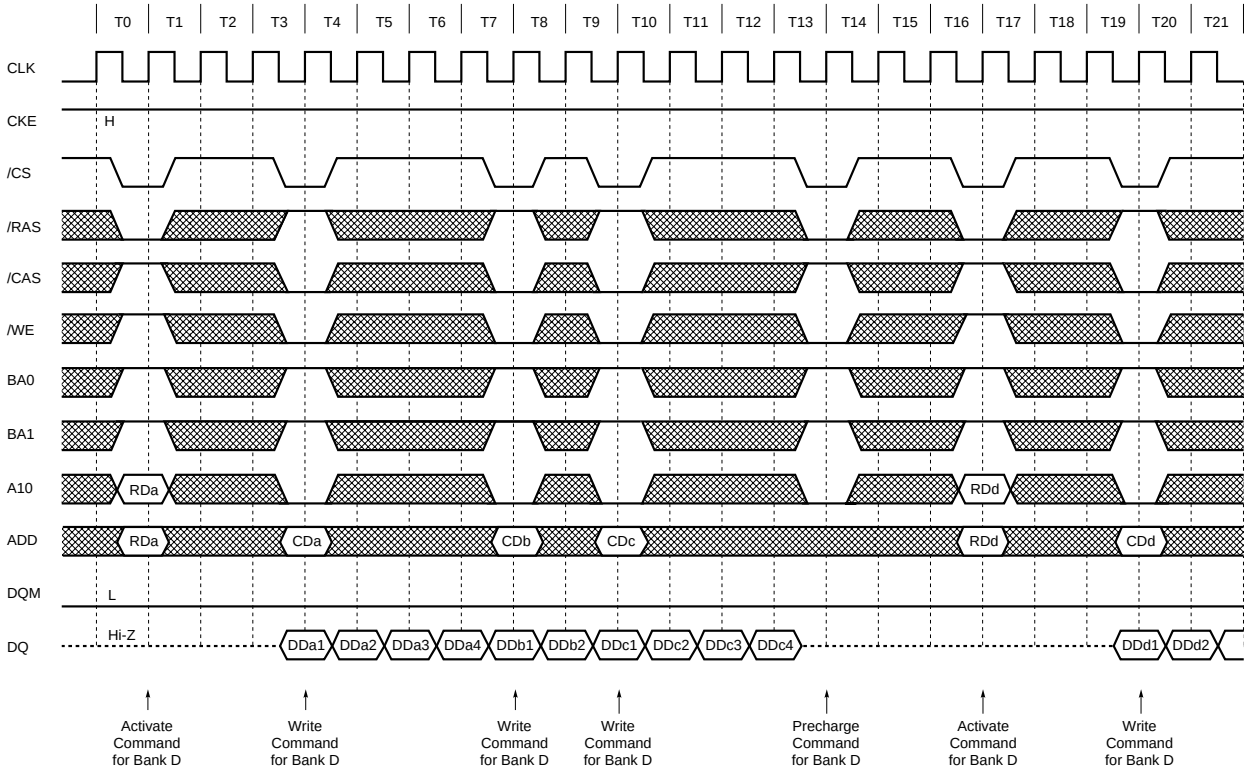


[Burst Length = 4, /CAS Latency = 3]



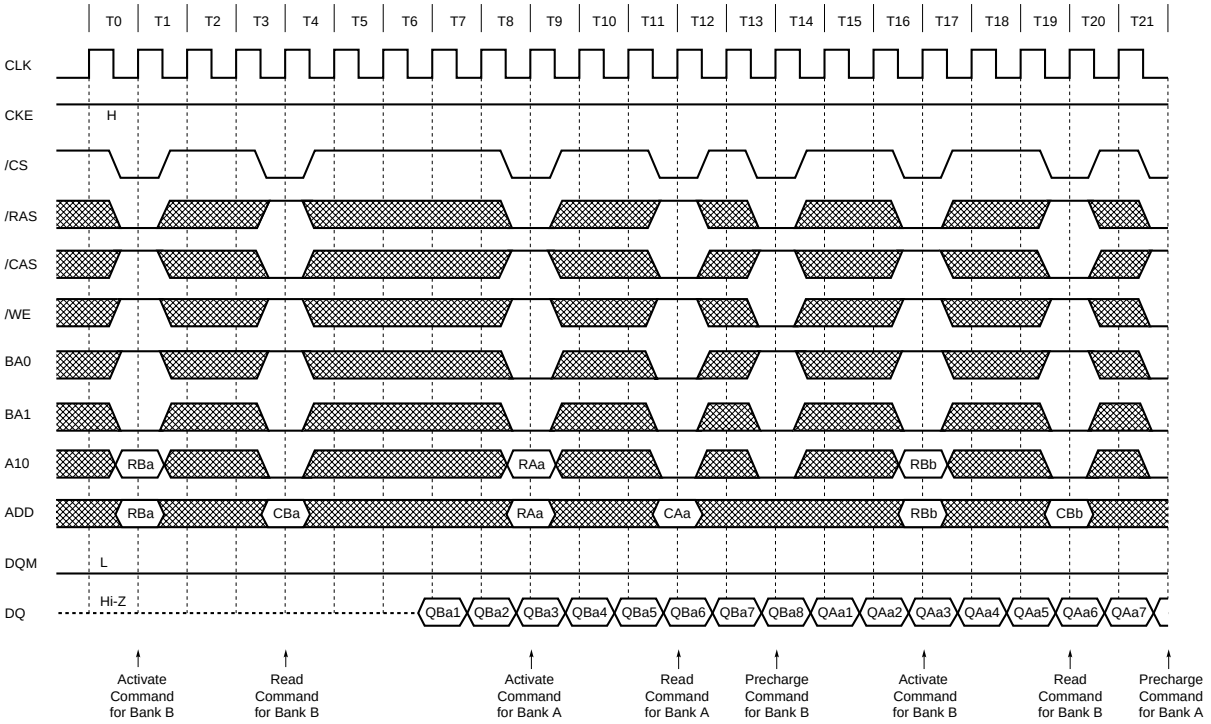
[Burst Length = 4, /CAS Latency = 2]

Random Column Write

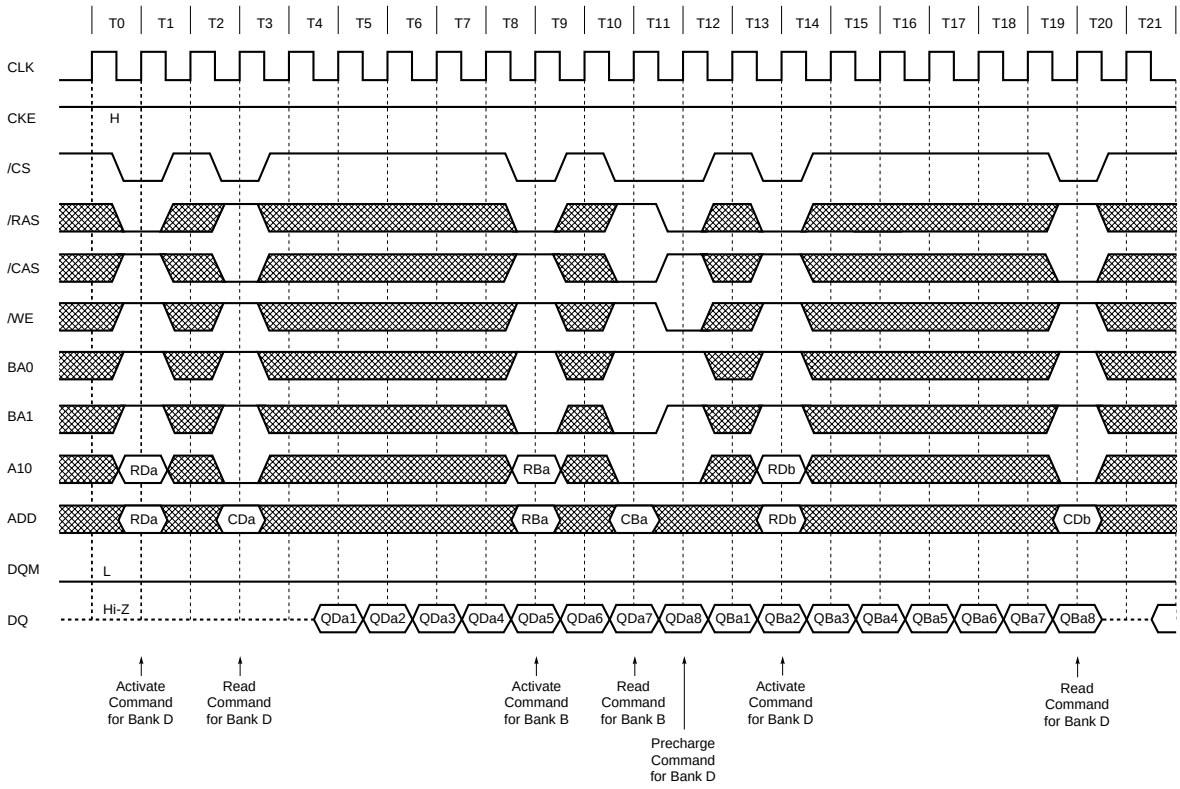


[Burst Length = 4]

Random Row Read

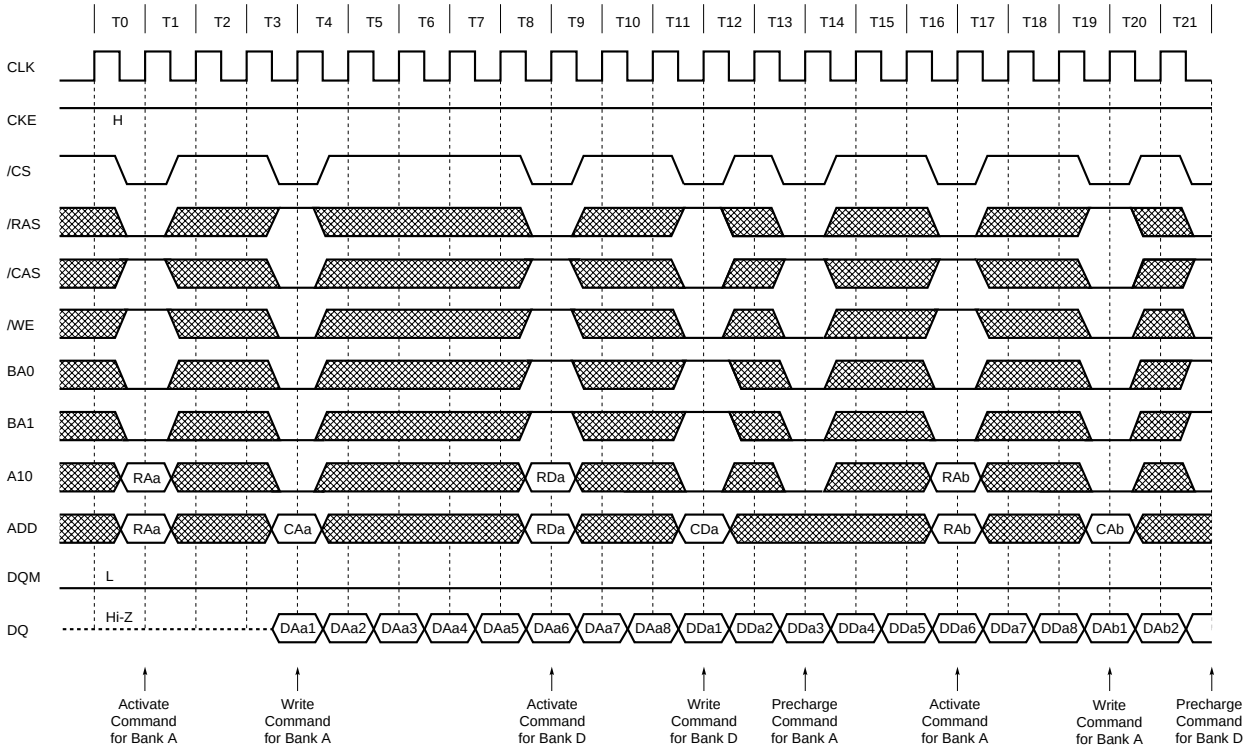


[Burst Length = 8, /CAS Latency = 3]



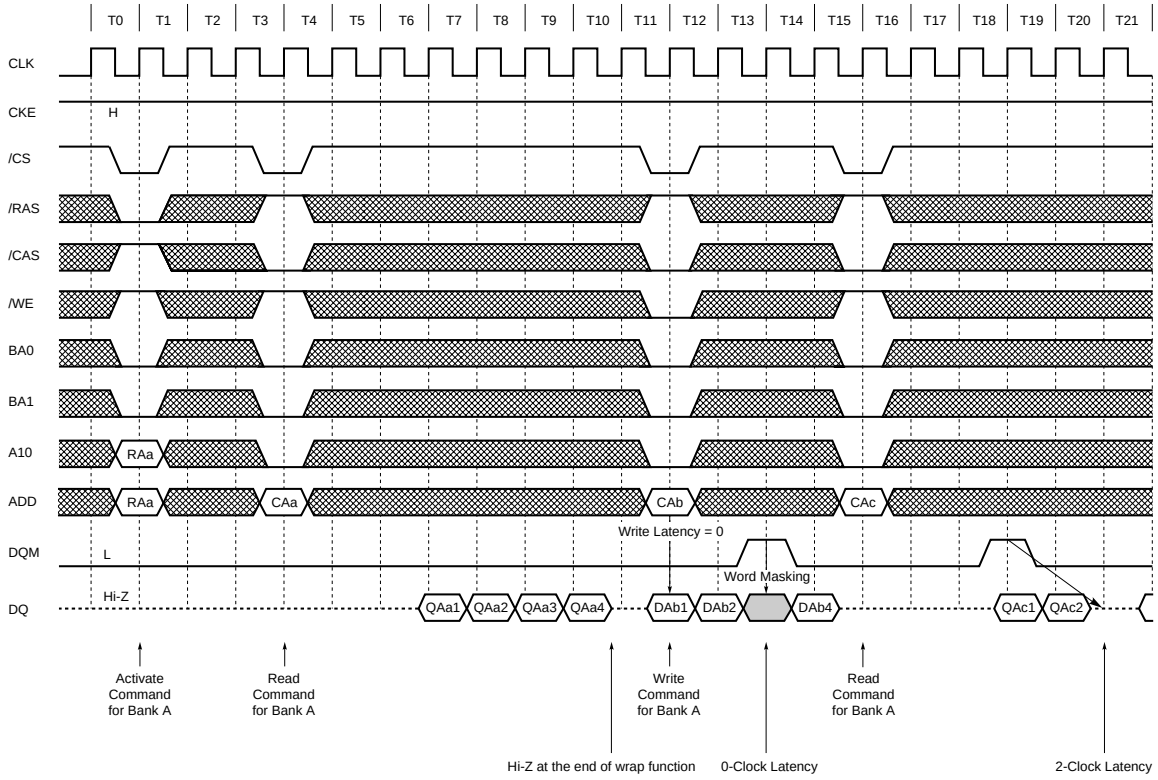
[Burst Length = 8, /CAS Latency = 2]

Random Row Write

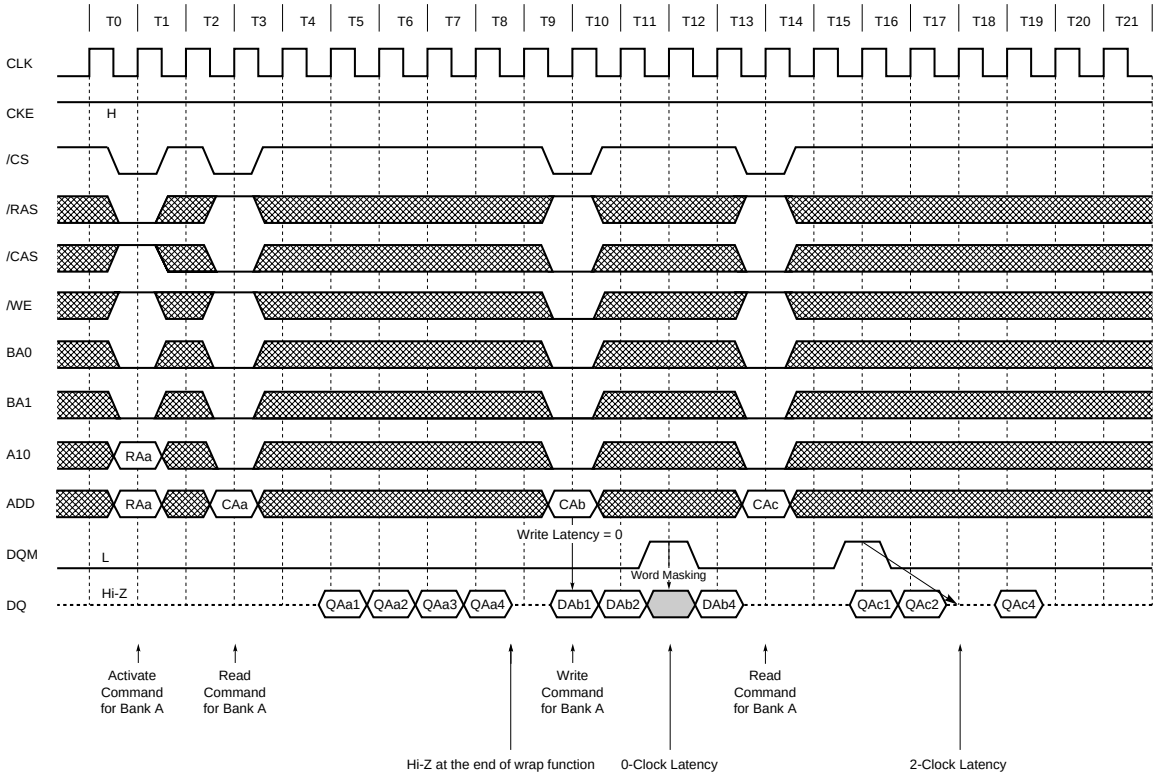


[Burst Length = 8]

Read and Write

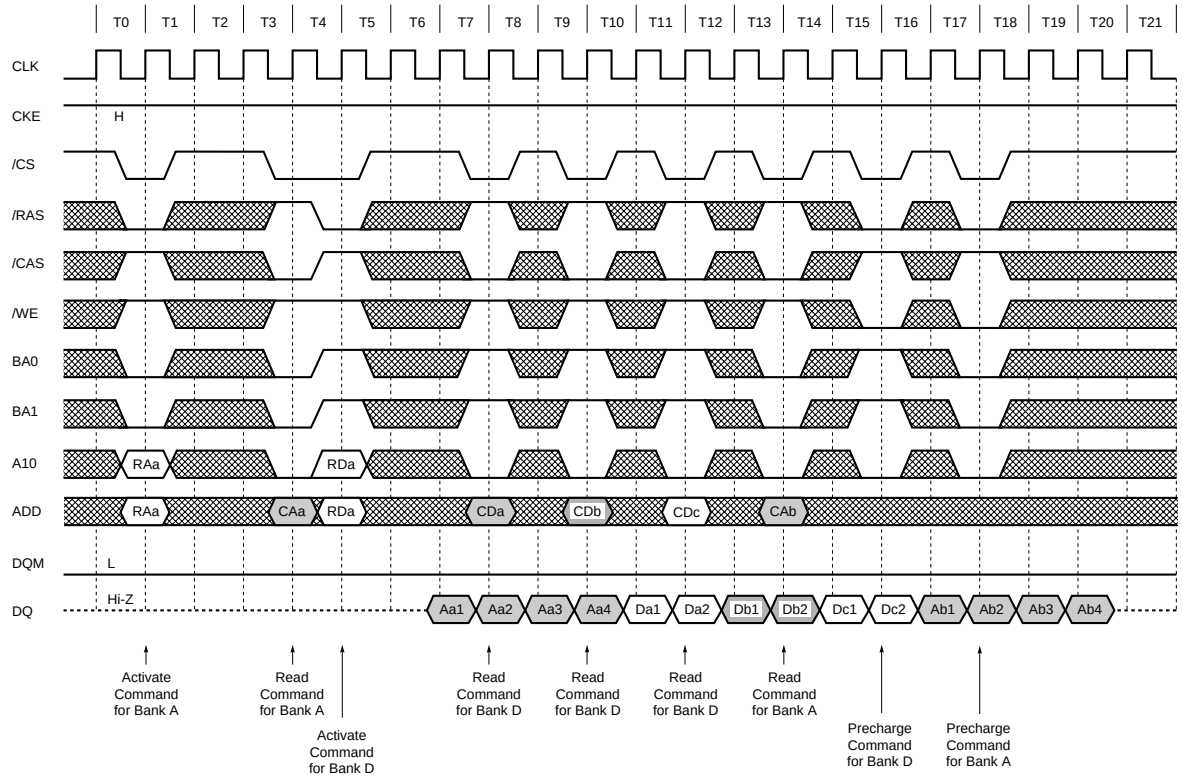


[Burst Length = 4, /CAS Latency = 3]

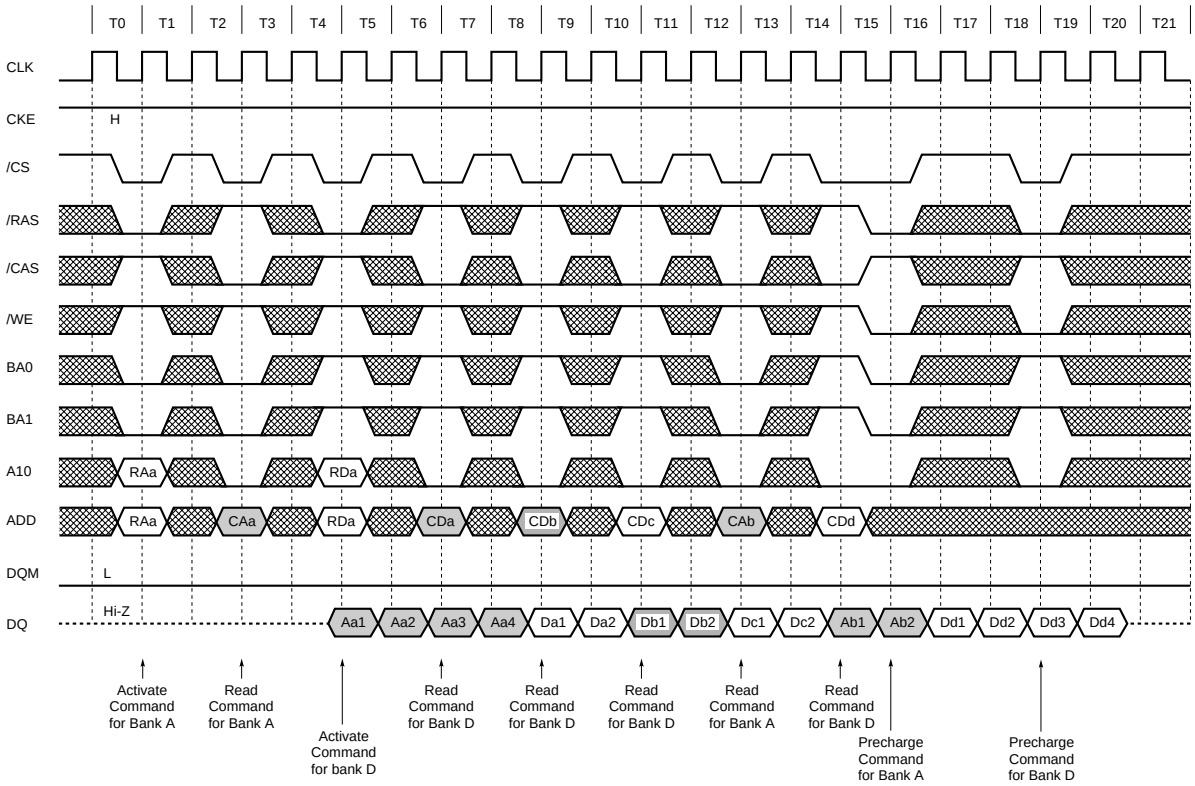


[Burst Length = 4, /CAS Latency = 2]

Interleaved Column Read Cycle

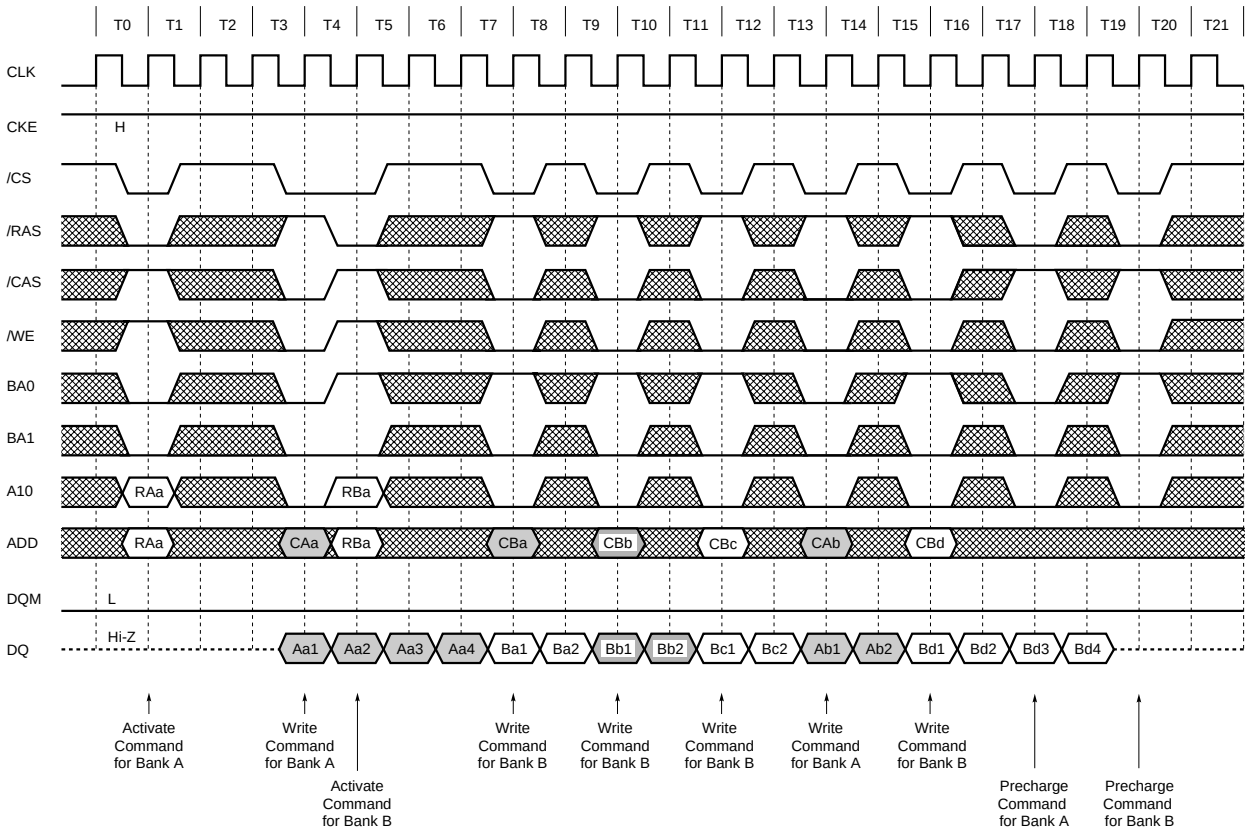


[Burst Length = 4, /CAS Latency = 3]



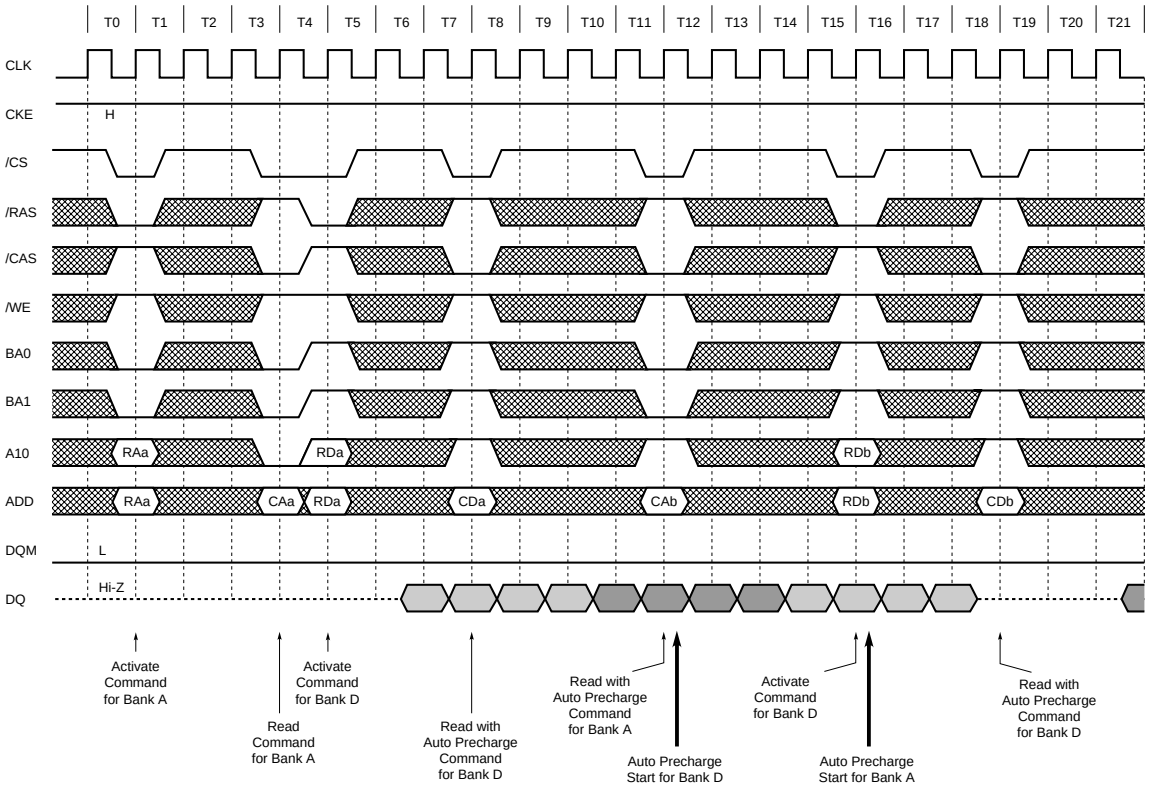
[Burst Length = 4, /CAS Latency = 2]

Interleaved Column Write Cycle

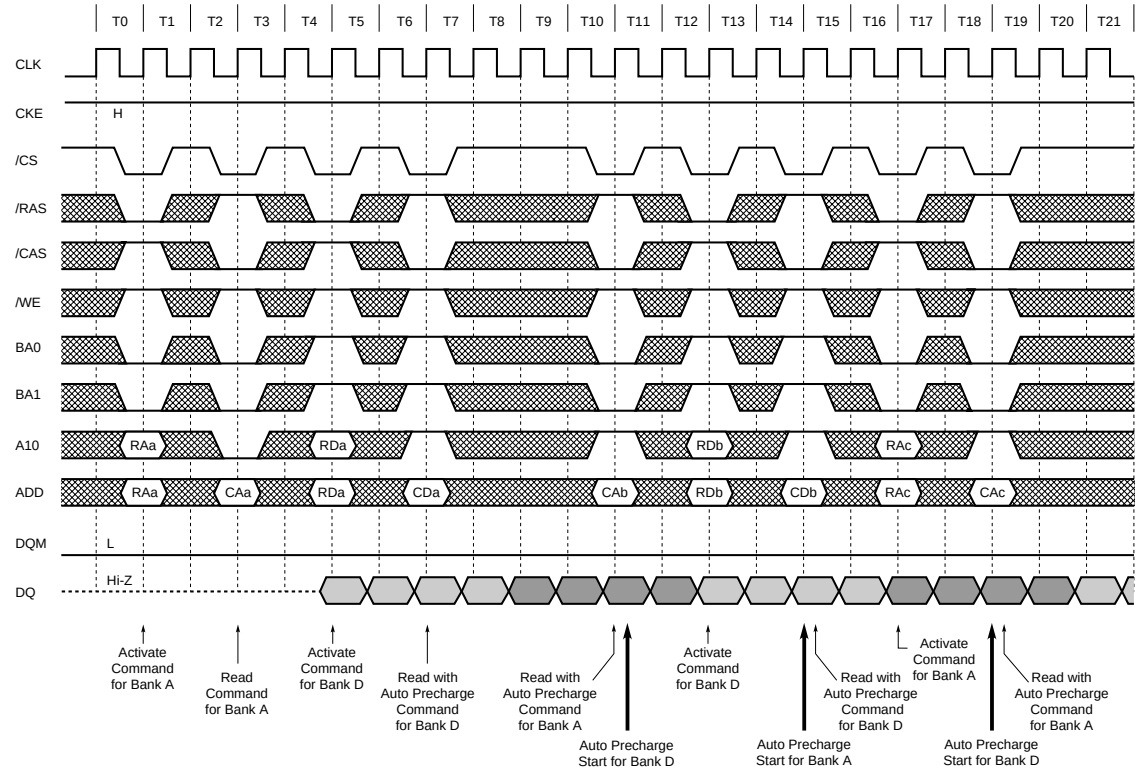


[Burst Length = 4]

Auto Precharge after Read Burst

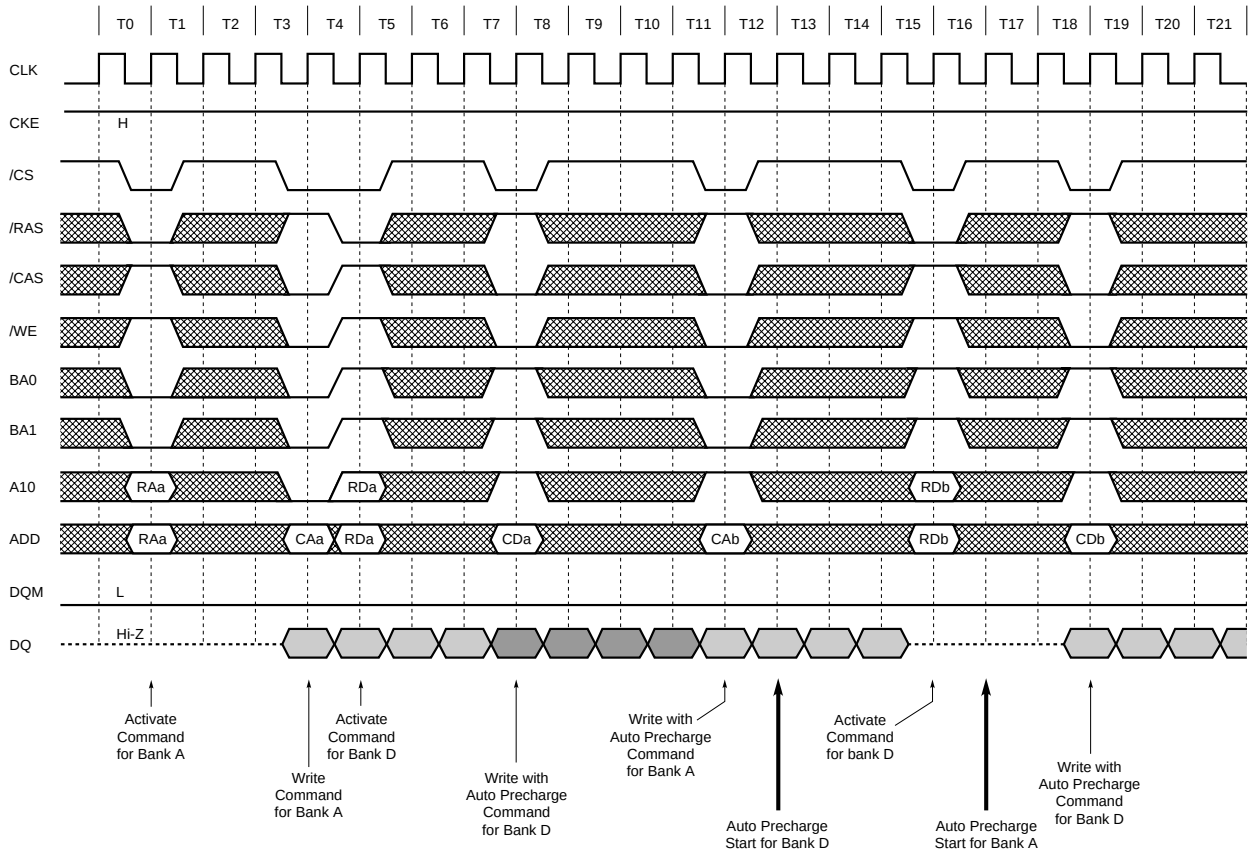


[Burst Length = 4, /CAS Latency = 3]



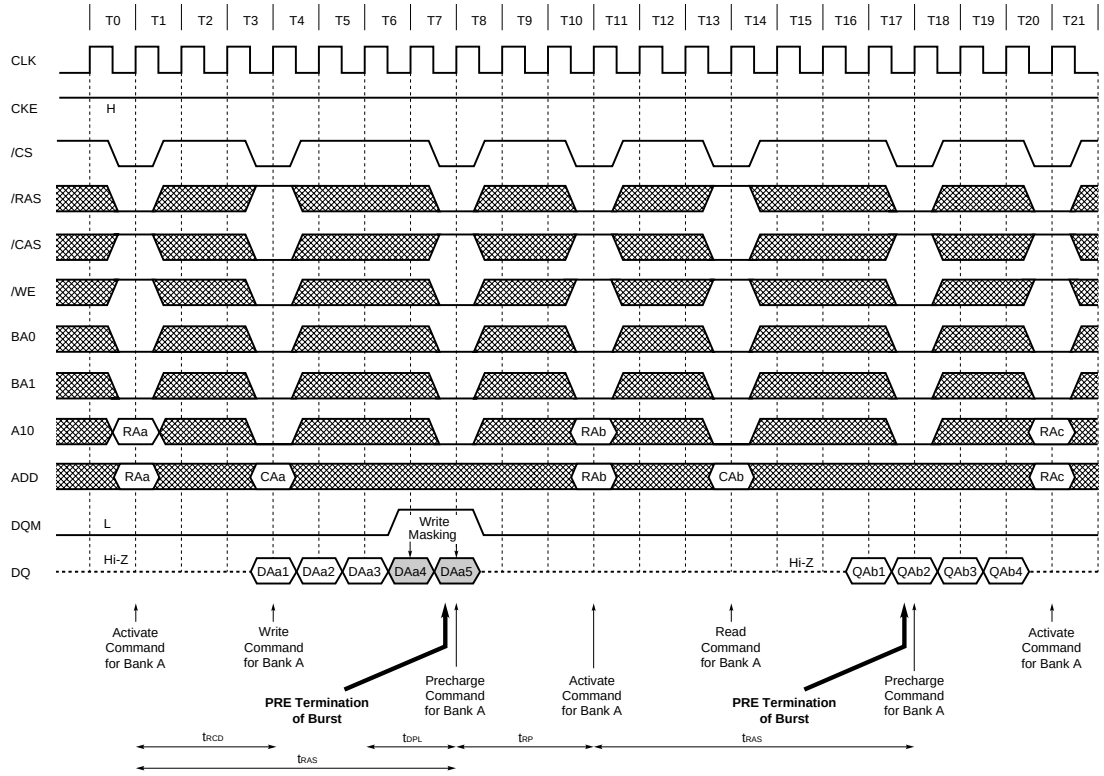
[Burst Length = 4, /CAS Latency = 2]

Auto Precharge after Write Burst

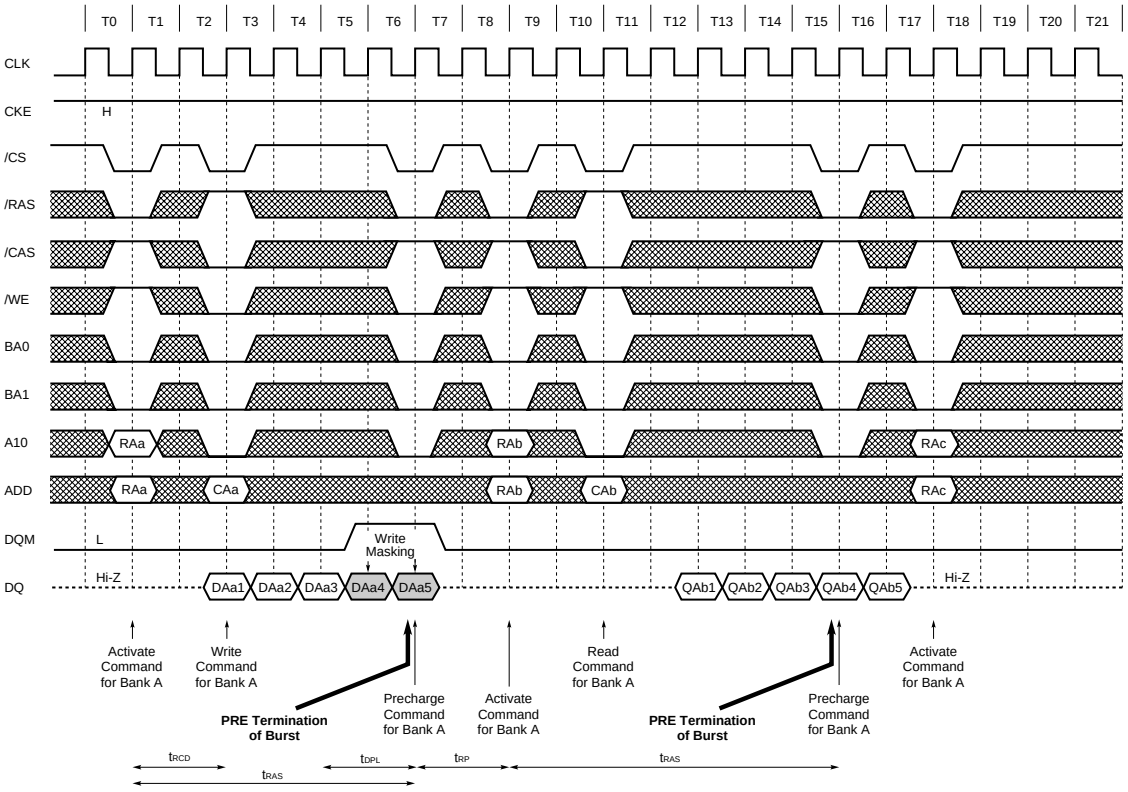


[Burst Length = 4]

Precharge Termination



[Burst Length = 8, /CAS Latency = 3]



[Burst Length = 8, /CAS Latency = 2]

1 Gbit NAND E2PROM

Memory cell 264 × 256K × 16

Register 264 × 16

Page size 264 words

Block size (8K + 256) words

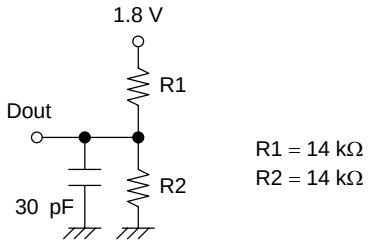
AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(Ta = –30° to 85°C, V_{CC} = 1.70 V to 1.95 V)

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
t_{CLS}	CLE Setup Time	0	—	ns	
t_{CLH}	CLE Hold Time	10	—	ns	
t_{CS}	$\overline{CE}$ Setup Time	0	—	ns	
t_{CH}	$\overline{CE}$ Hold Time	10	—	ns	
t_{WP}	Write Pulse Width	25	—	ns	
t_{ALS}	ALE Setup Time	0	—	ns	
t_{ALH}	ALE Hold Time	10	—	ns	
t_{DS}	Data Setup Time	20	—	ns	
t_{DH}	Data Hold Time	10	—	ns	
t_{WC}	Write Cycle Time	50	—	ns	
t_{WH}	$\overline{WE}$ High Hold Time	15	—	ns	
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Low	100	—	ns	
t_{RR}	Ready to $\overline{RE}$ Falling Edge	20	—	ns	
t_{RP}	Read Pulse Width	35	—	ns	
t_{RC}	Read Cycle Time	50	—	ns	
t_{REA}	$\overline{RE}$ Access Time (Serial Data Access, Status Read, ID Read)	—	35	ns	
t_{CEA}	$\overline{CE}$ Access Time (Serial Data Access, Status Read, ID Read)	—	45	ns	
t_{ALEA}	ALE Access Time (ID Read)	—	45	ns	
t_{OH}	Data Output Hold Time	10	—	ns	
t_{RHZ}	$\overline{RE}$ High to Output High Impedance	—	30	ns	
t_{CHZ}	$\overline{CE}$ High to Output High Impedance	—	20	ns	
t_{REH}	$\overline{RE}$ High Hold Time	15	—	ns	
t_{IR}	Output-High-impedance-to-$\overline{RE}$ Falling Edge	0	—	ns	
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low	30	—	ns	
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low	30	—	ns	
t_{R}	Memory Cell Array to Starting Address	—	25	μs	
t_{RBT}	Boot Block Access	—	150	μs	
t_{WB}	$\overline{WE}$ High to Busy	—	200	ns	
t_{AR2}	ALE Low to $\overline{RE}$ Low (Read Cycle)	50	—	ns	
t_{RST}	Device Reset Time (Ready//Read/Program/Erase)	—	6 / 6 / 10 / 500	μs	

AC TEST CONDITIONS

PARAMETER	CONDITION
Vcc	1.70V to 1.95V
Input level	V_{CC} – 0.2 V, 0.2 V
Input pulse rise and fall time	3 ns
Input comparison level	0.9 V, 0.9 V
Output data comparison level	0.9 V, 0.9 V
Output load	See below Figure



PROGRAMMING AND ERASING CHARACTERISTICS

(Ta = –30° to 85°C, V_{CC} = 1.70 V to 1.95 V)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t_{PROG}	Programming Time	—	200	700	μs	
N	Number of Programming Cycles on Same Page	—	—	3		(1)
t_{BERASE}	Block Erasing Time	—	2	10	ms	

(1): Refer to Application Note (12) toward the end of this document.

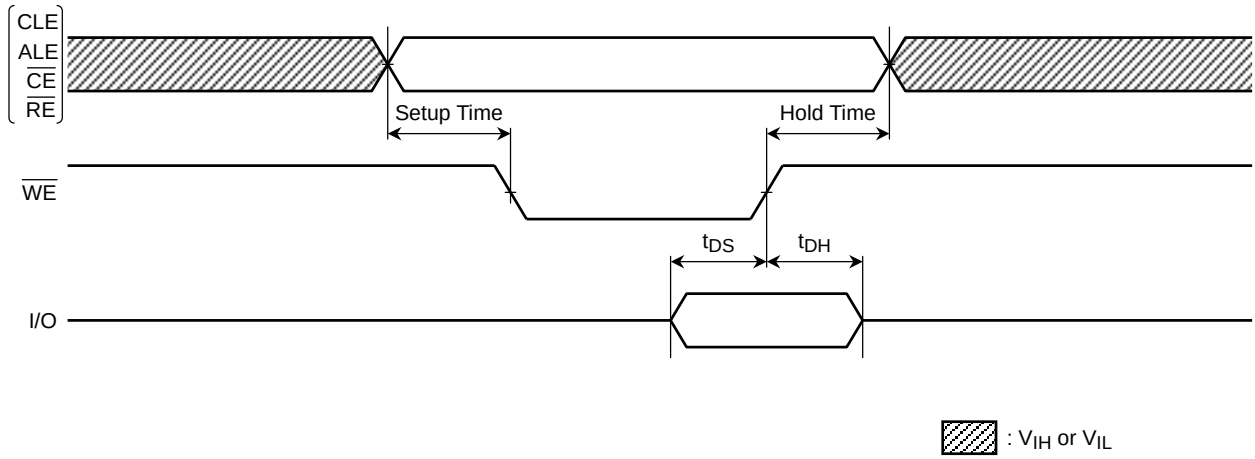
VALID BLOCKS (1)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N_{VB}	Number of Valid Blocks	8032	—	8192	Blocks

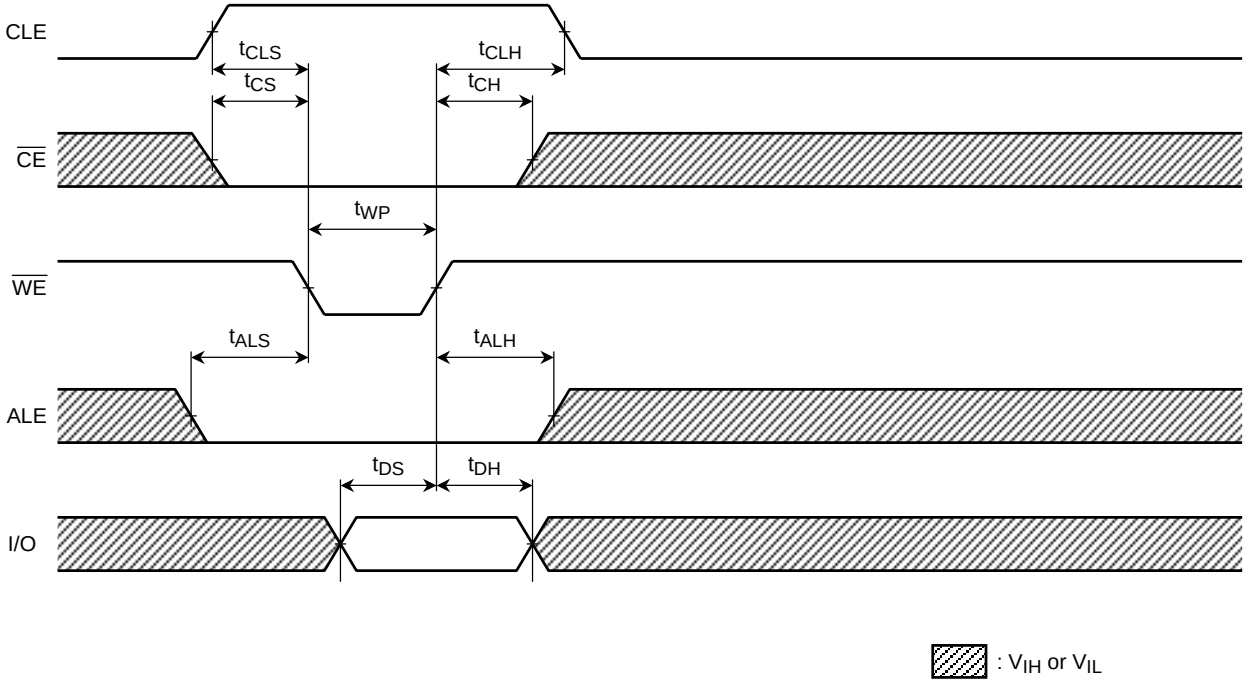
(1) The device occasionally contains unusable blocks. Refer to Application Note (14) toward the end of this document. The 1st block (block address #00) is guaranteed to be a valid block at the time of shipment.

TIMING DIAGRAMS

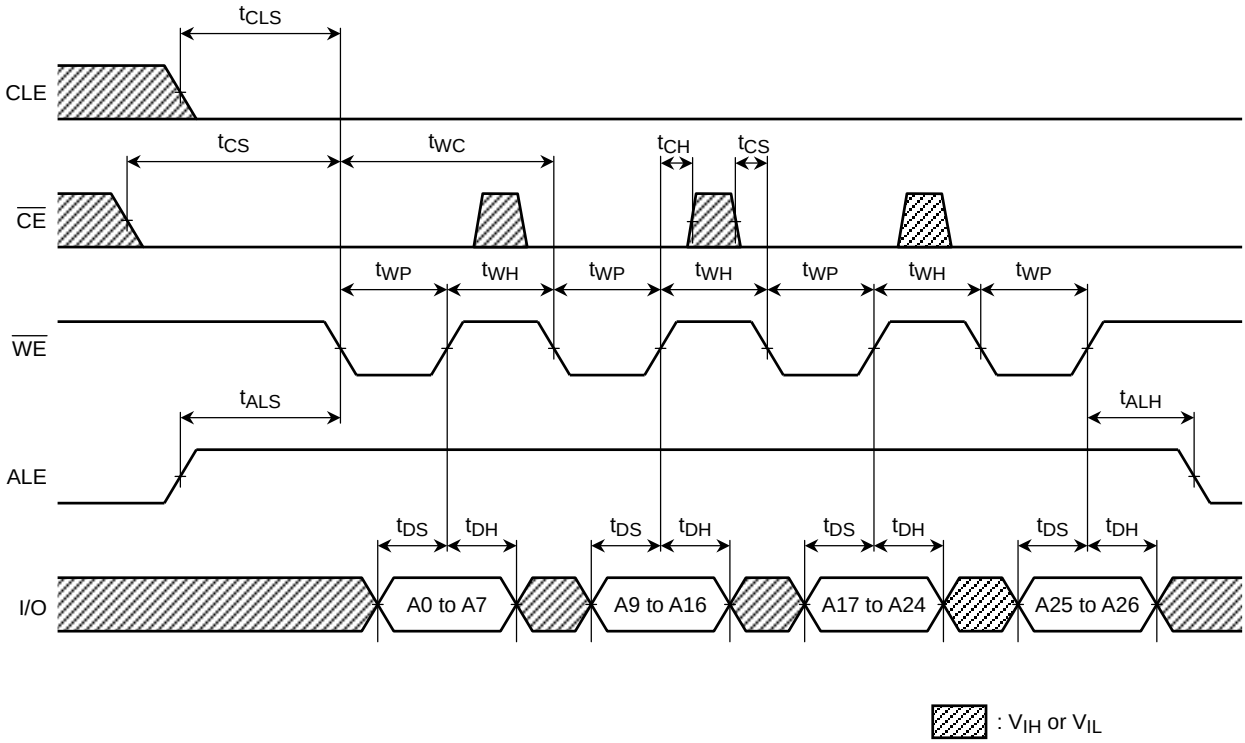
Latch Timing Diagram for Command/Address/Data



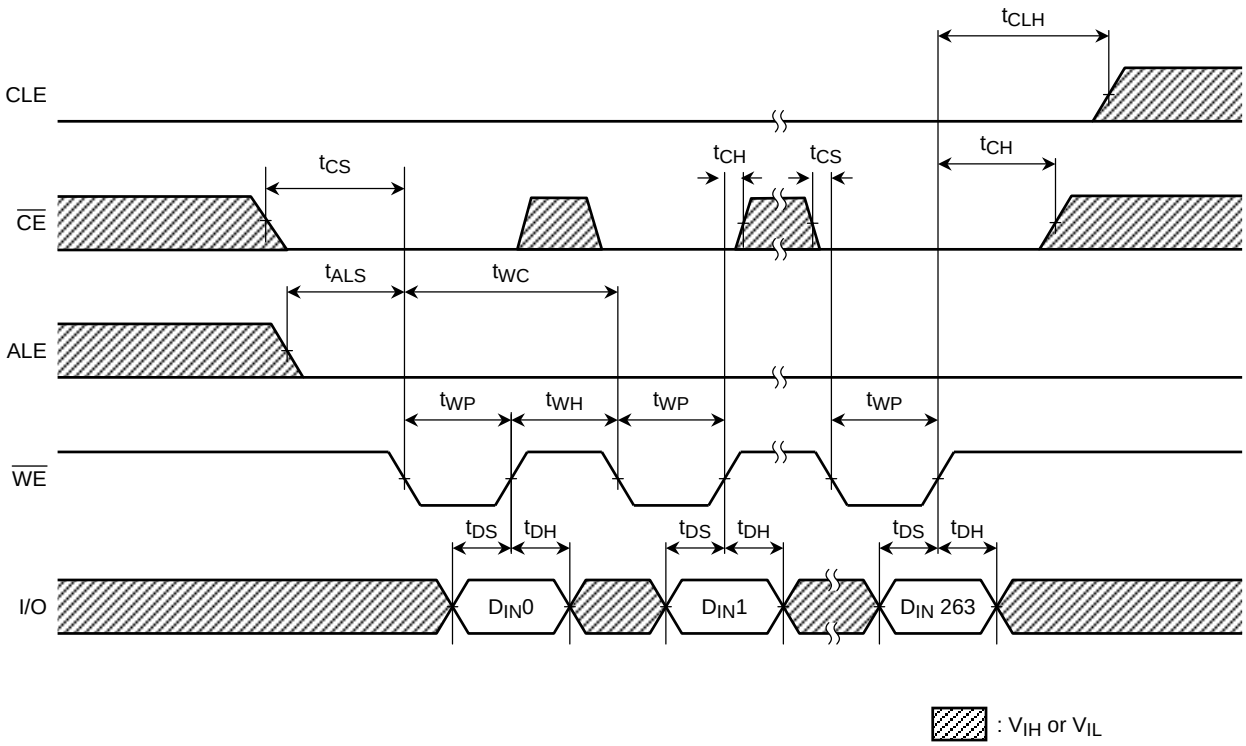
Command Input Cycle Timing Diagram



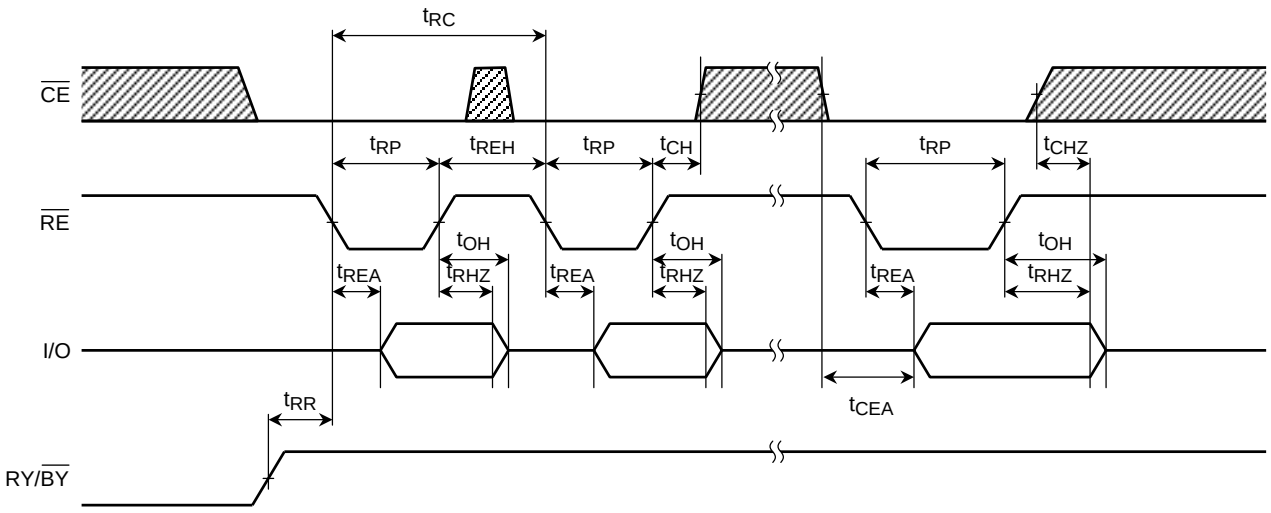
Address Input Cycle Timing Diagram



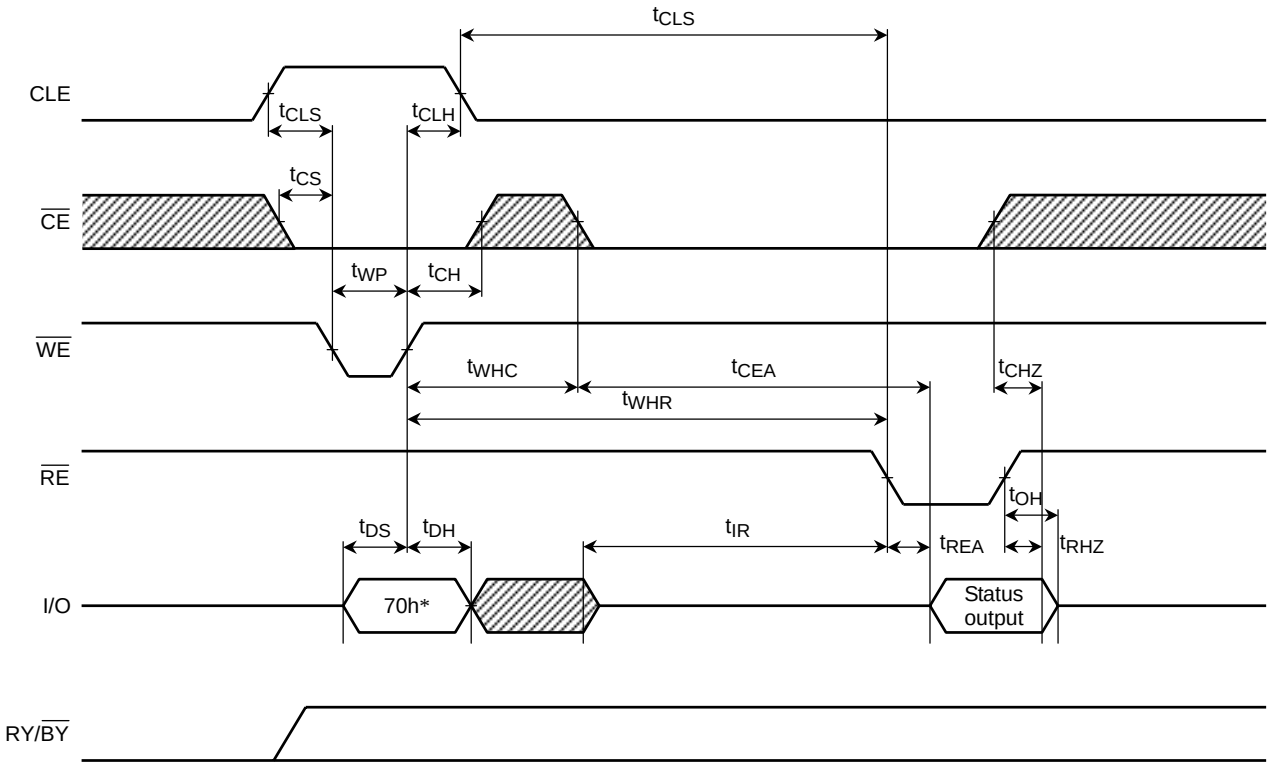
Data Input Cycle Timing Diagram



Serial Read Cycle Timing Diagram



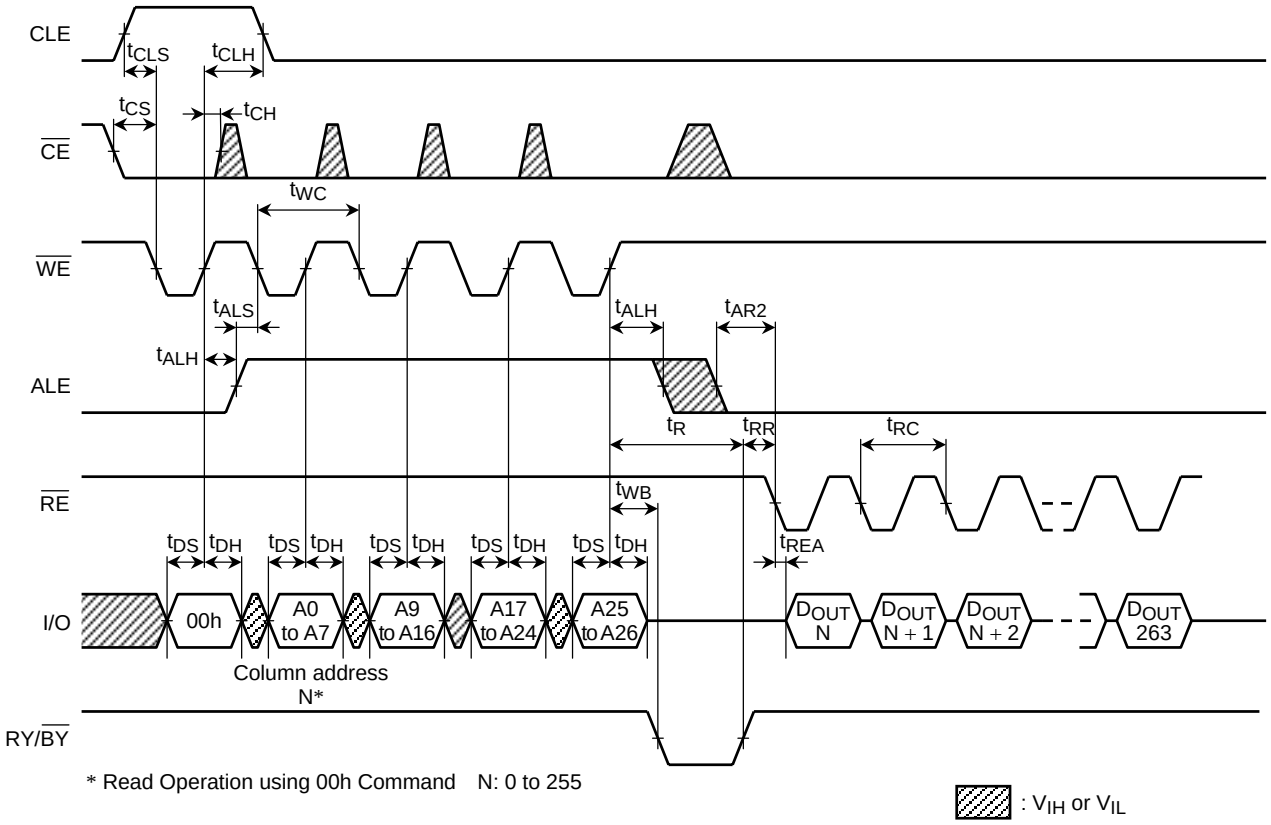
Status Read Cycle Timing Diagram



* 70h represents the hexadecimal number

: V_{IH} or V_{IL}

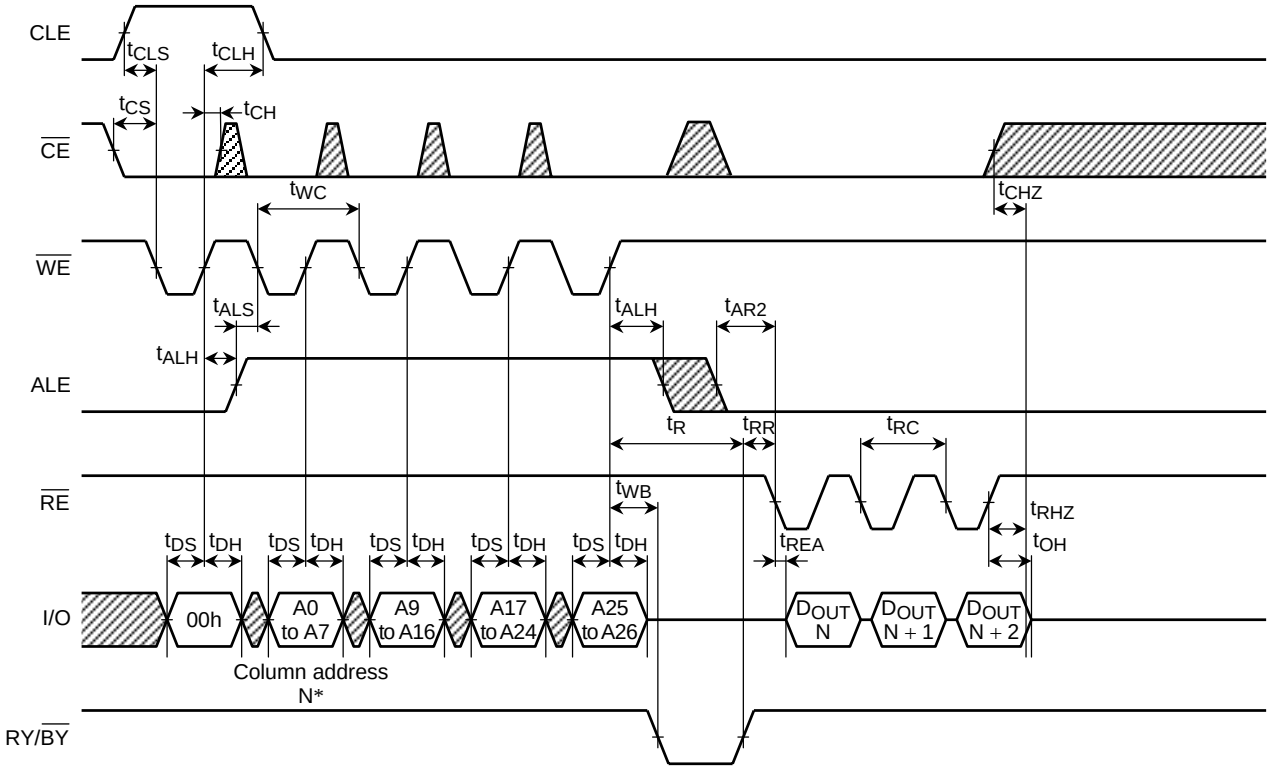
Read Cycle (1) Timing Diagram



* Read Operation using 00h Command N: 0 to 255

: V_{IH} or V_{IL}

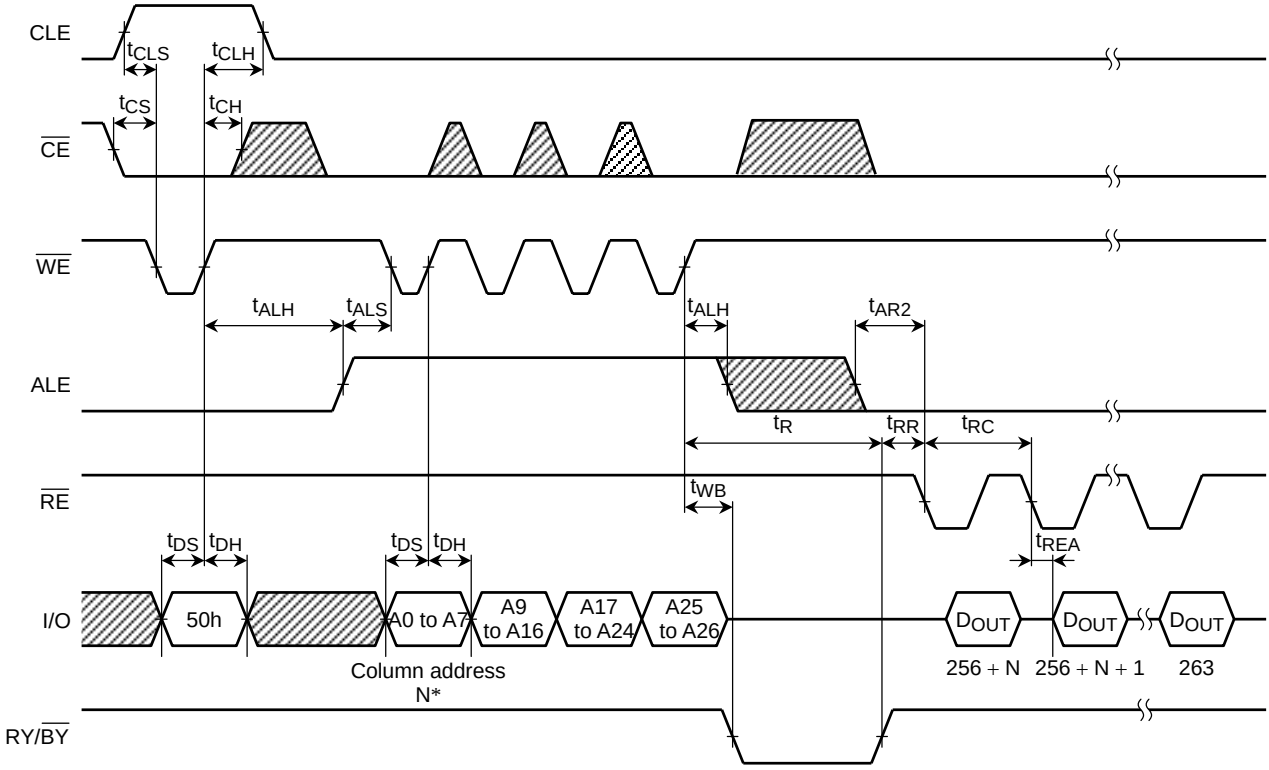
Read Cycle (1) Timing Diagram: When Interrupted by $\overline{CE}$



*: Read operation using 00h command N: 0 to 255

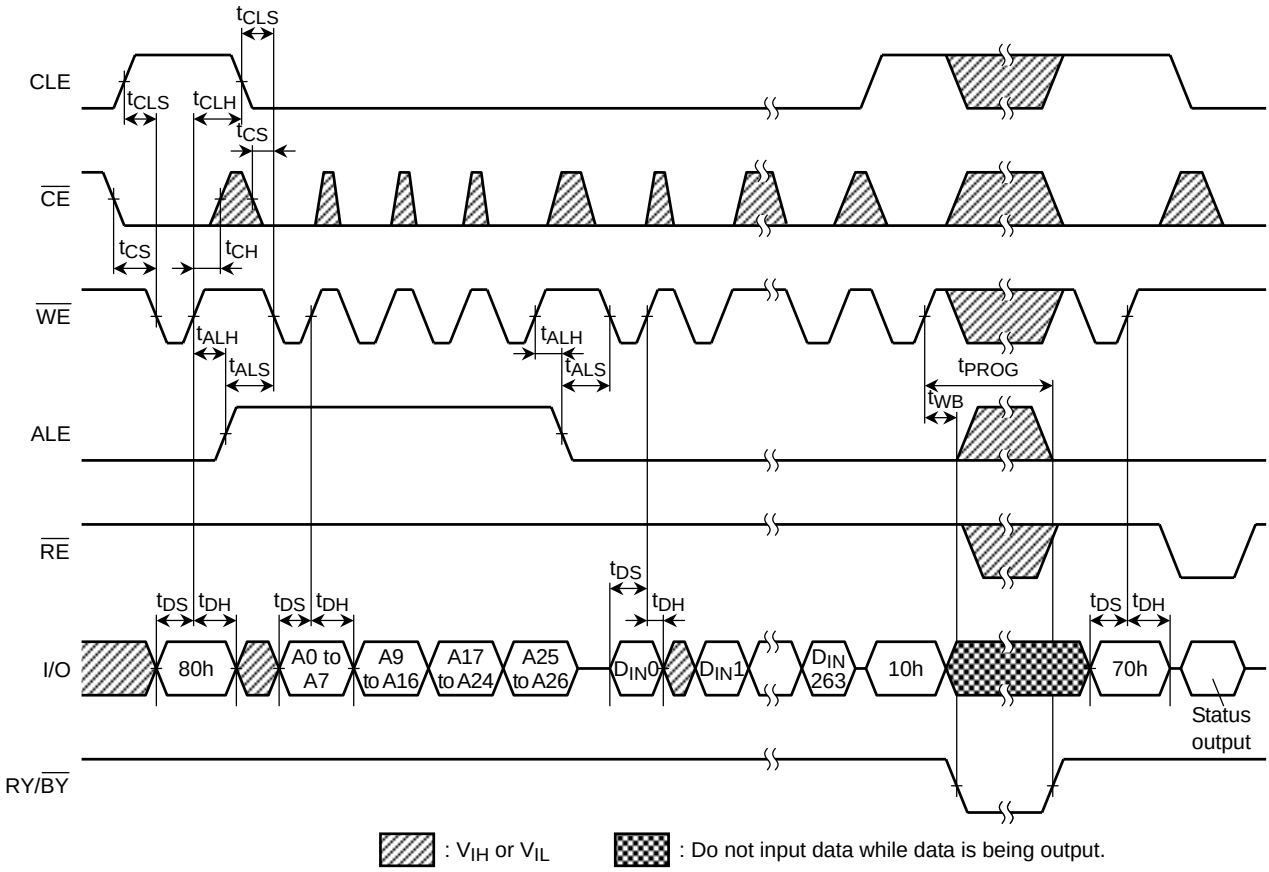
: V_{IH} or V_{IL}

Read Cycle (2) Timing Diagram

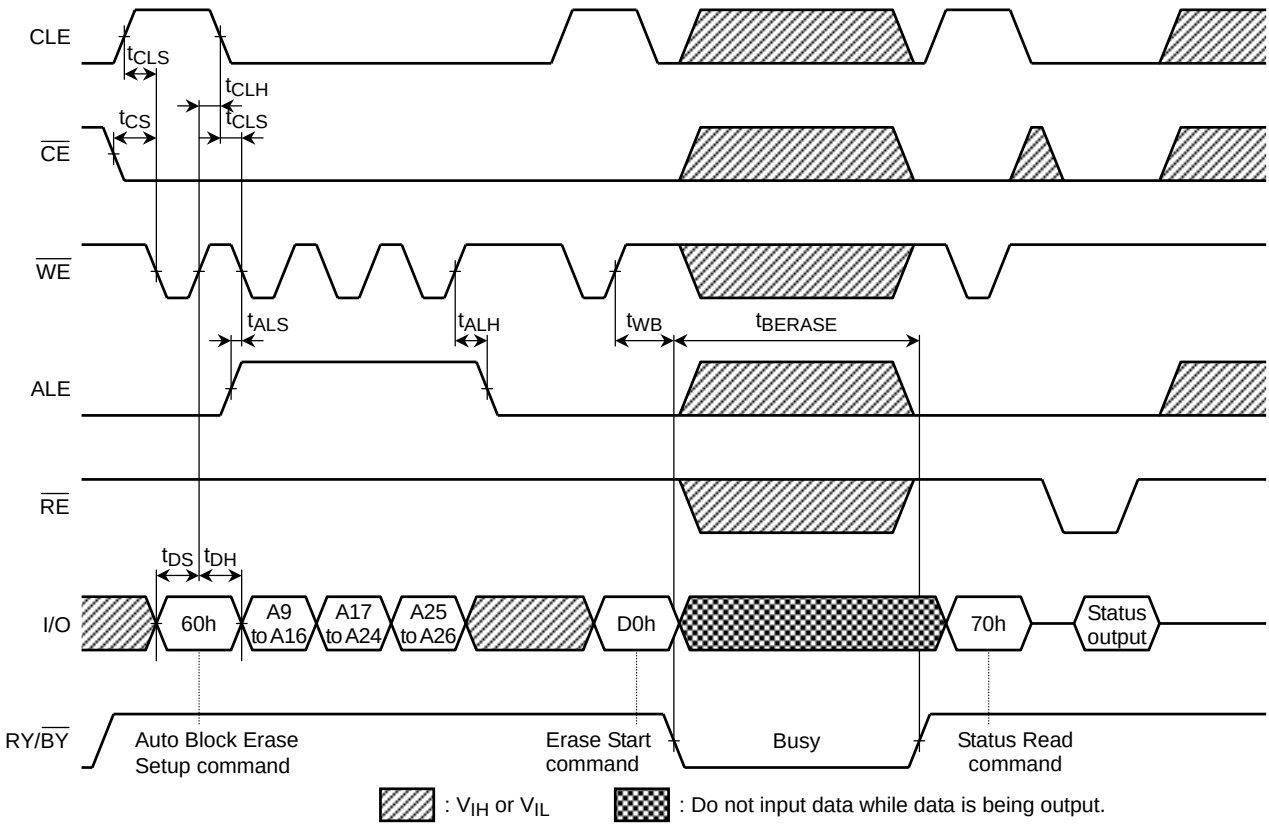


*: Read operation using 50h command N: 0 to 7

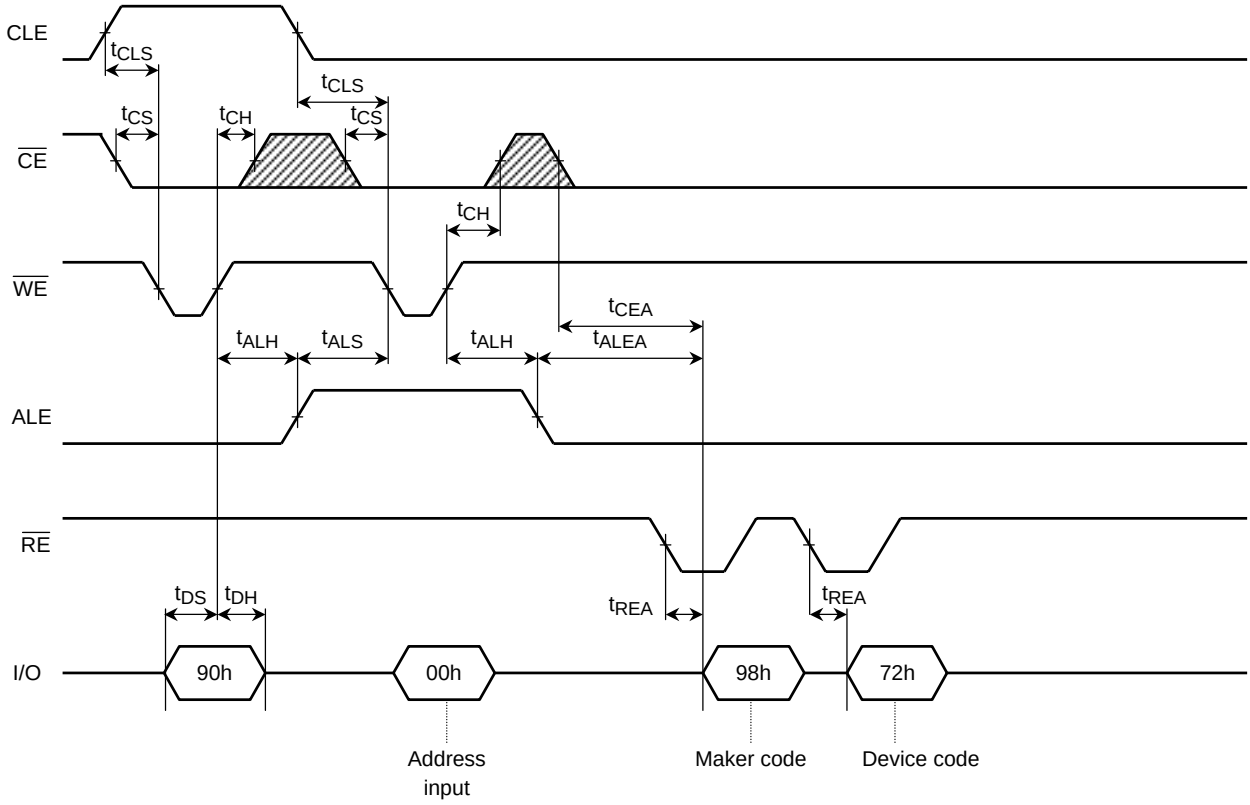
Auto-Program Operation Timing Diagram



Auto Block Erase Timing Diagram

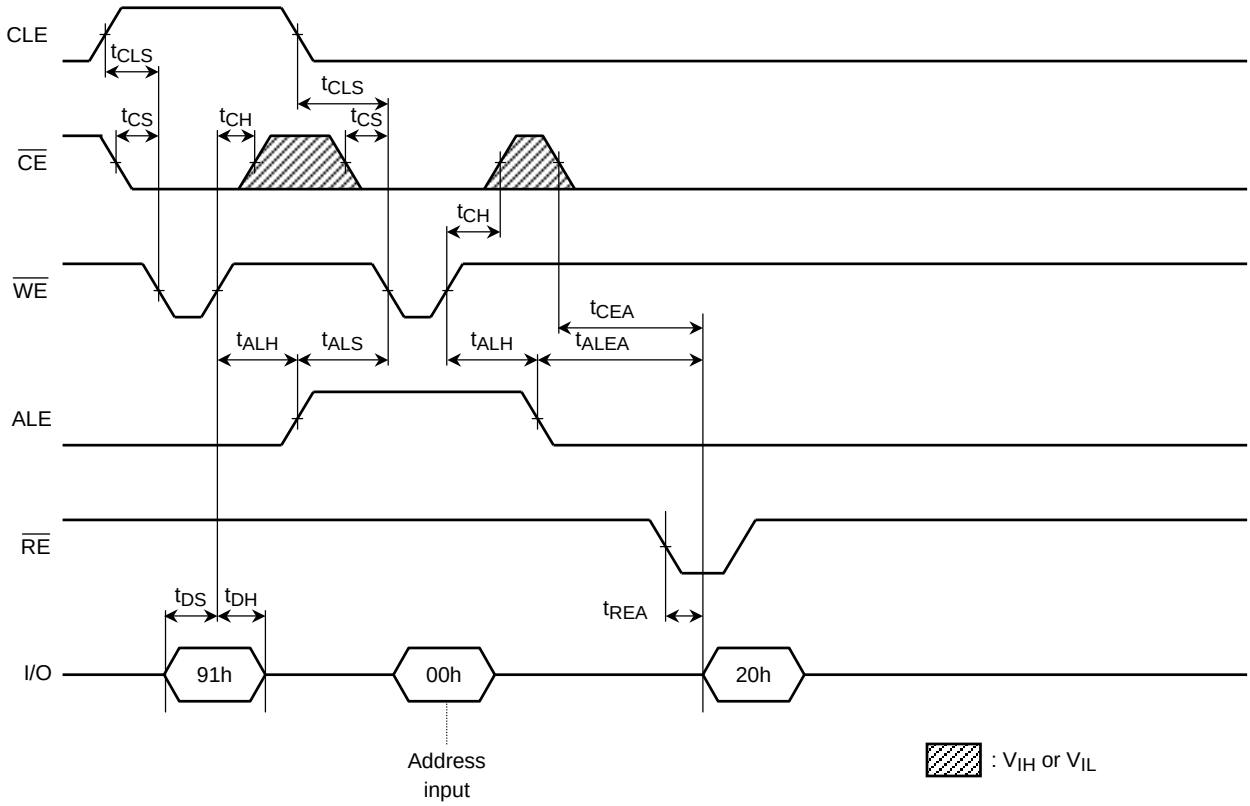


ID Read (1) Operation Timing Diagram



: V_{IH} or V_{IL}

ID Read (2) Operation Timing Diagram



: V_{IH} or V_{IL}

PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information.

Command Latch Enable: CLE

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is High.

Address Latch Enable: ALE

The ALE signal is used to control loading of either address information or input data into the internal address/data register. Address information is latched on the rising edge of $\overline{WE}$ if ALE is High. Input data is latched if ALE is Low.

Chip Enable: $\overline{CE}$

The device goes into a low-power Standby mode when $\overline{CE}$ goes High during a wait state. The $\overline{CE}$ signal is ignored when device is in Busy state (RY/$\overline{BY}$ = L), such as during a Program or Erase or Read operation, and will not enter Standby mode even if the $\overline{CE}$ input goes High.

Write Enable: $\overline{WE}$

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$

The $\overline{RE}$ signal controls serial data output. Data is available t_{REA} after the falling edge of $\overline{RE}$.
The internal column address counter is also incremented (Address = Address + 1) on this falling edge.

I/O Port: I/O1 to 8

The I/O1 to 8 pins are used as a port for transferring address, command and input/output data to and from the device.

I/O Port: I/O9 to 16

The I/O9 to 16 pins are used as a port for input/output data to and from the device. The I/O9 to 16 pins are low level (VIL) when address and command are asserted.

Write Protect: $\overline{WP}$

The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.

Ready/Busy: RY/ $\overline{BY}$

The RY/$\overline{BY}$ output signal is used to indicate the operating condition of the device. The RY/$\overline{BY}$ signal is in Busy state (RY/$\overline{BY}$ = L) during the Program, Erase and Read operations and will return to Ready state (RY/$\overline{BY}$ = H) after completion of the operation. The output buffer for this signal is an open drain.

Schematic Cell Layout and Address Assignment

The Program operation works on page units while the Erase operation works on block units.

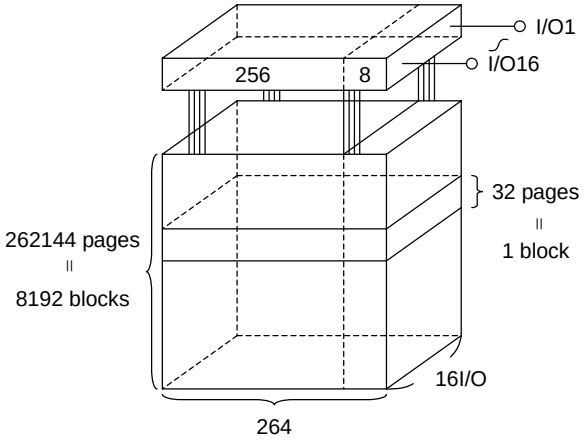


Figure 2. Schematic Cell Layout

A page consists of 264 words in which 256 words are used for main memory storage and 8 words are for redundancy or for other uses.

1 page = 264 words
1 block = 264 words × 32 pages = (8K + 256) words
Capacity = 264 words × 32 pages × 8192 blocks

Table 1. Addressing

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
First cycle	A7	A6	A5	A4	A3	A2	A1	A0
Second cycle	A16	A15	A14	A13	A12	A11	A10	A9
Third cycle	A24	A23	A22	A21	A20	A19	A18	A17
Fourth cycle	*L	*L	*L	*L	*L	*L	A26	A25

A0 to A7: Column address
A9 to A26: Page address
A14 to A26: Block address
A9 to A13: NAND address in block

* : A8 is automatically set to Low or High by a 00h command.
I/O3-8 must be set to Low in the fourth cycle.
I/O9 to I/O16 should be low when address is input.

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by the fifteen different command operations shown in Table 4. Address input, command input and data input/output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$, $\overline{WP}$ and PRE signals, as shown in Table 2.

Table 2. Logic table

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$ *1
Command Input	H	L	L		H	*
Address Input	L	H	L		H	*
Data Input	L	L	L		H	H
Serial Data Output	L	L	L	H		*
During Read (Busy)	*	*	L	H	H	*
	*	*	H	*	*	*
During Programming (Busy)	*	*	*	*	*	H
During Erasing (Busy)	*	*	*	*	*	H
Program, Erase Inhibit	*	*	*	*	*	L
Standby	*	*	H	*	*	0 V/V_{CC}

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

*1: Refer to Application Note (10) toward the end of this document regarding the $\overline{WP}$ signal when Program or Erase Inhibit

*2: The $\overline{CE}$ signal is ignored when device is in Busy state ($R/\overline{B}$ = L), such as during a Program or Erase or Read operation, and will not enter Standby mode even if the $\overline{CE}$ input goes High.

Table 3 shows the operation states for Read mode.

Table 3. Read mode operation states

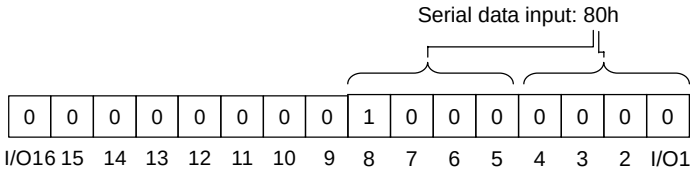
	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O1 to I/O16	Power
Output Select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active

H: V_{IH}, L: V_{IL}

Table 4. Command table (HEX)

	First Cycle	Second Cycle	Acceptable while Busy
Serial Data Input	80	—	
Read Mode (1)	00	—	
Read Mode (2)	50	—	
Reset	FF	—	○
Auto Program	10	—	
Auto Block Erase	60	D0	
Status Read	70	—	○
ID Read (1)	90	—	
ID Read (2)	91	—	

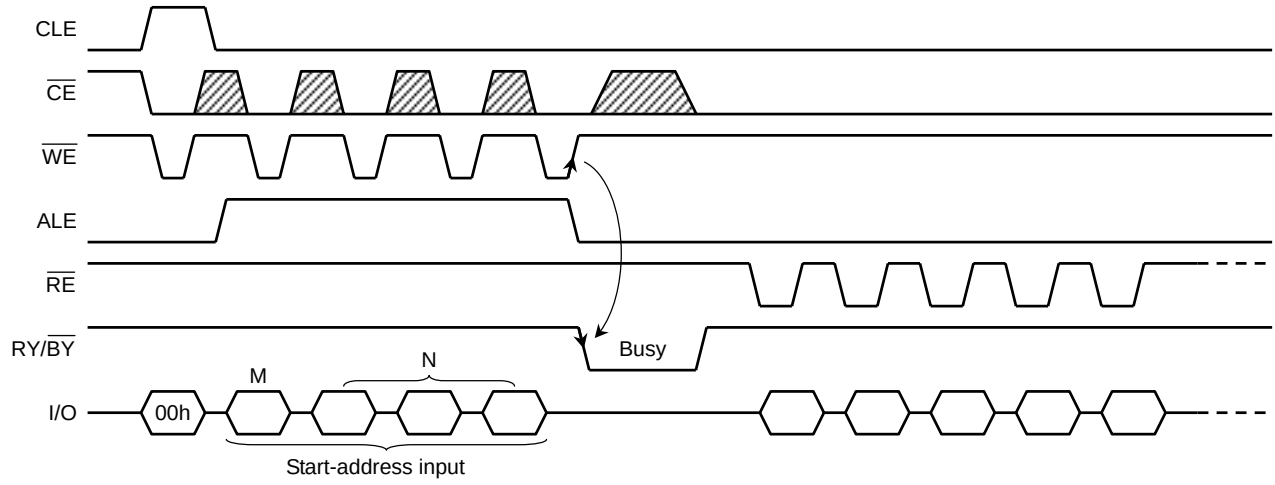
HEX data bit assignment
(Example)



DEVICE OPERATION

Read Mode (1)

Read mode (1) is set when a 00h command is issued to the Command register. Refer to Figure 3 below for timing details and the block diagram.



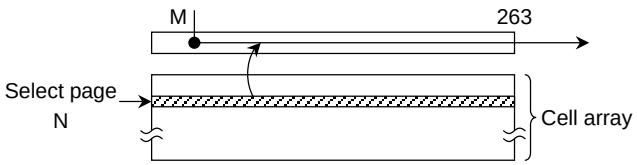


Figure 3. Read mode (1) operation

A data transfer operation from the cell array to the register starts on the rising edge of $\overline{WE}$ in the fourth cycle (after the address information has been latched). The device will be in Busy state during this transfer period.

After the transfer period the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the start pointer designated in the address input cycle.

Read Mode (2)

Read mode (2) has the same timing as Read modes (1) but is used to access information in the extra 8-word redundancy area of the page. The start pointer is therefore set to a value between word 256 and word 263.

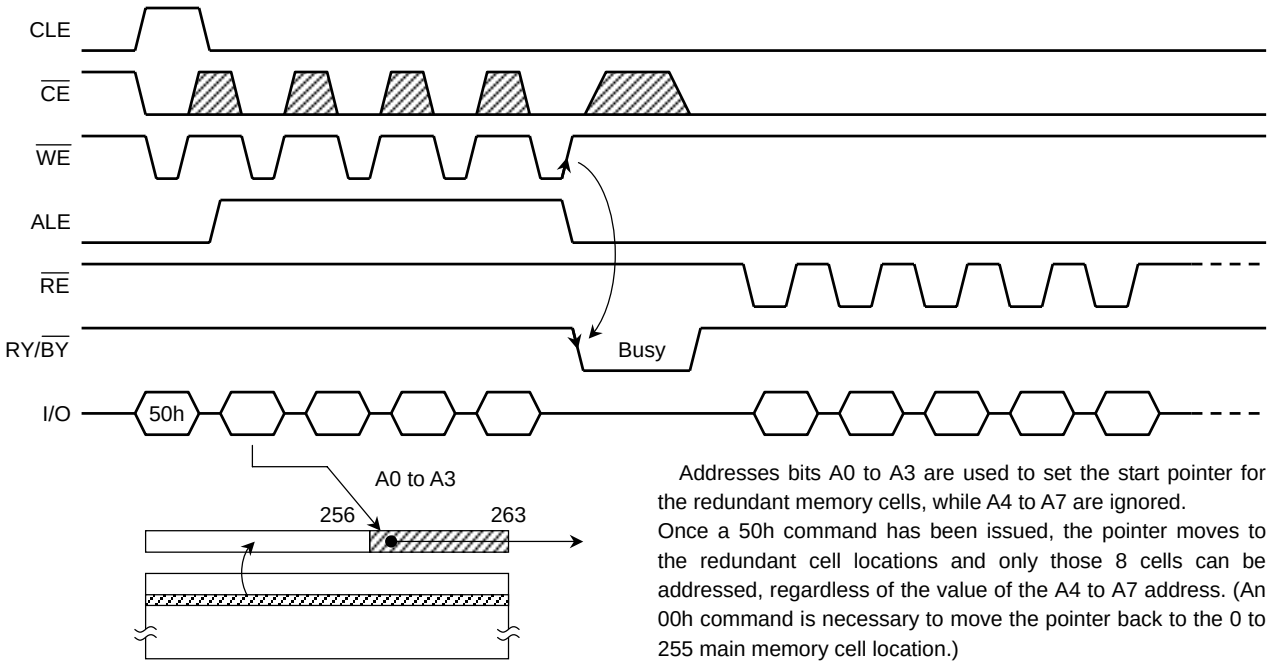


Figure 4. Read mode (2) operation

Addresses bits A0 to A3 are used to set the start pointer for the redundant memory cells, while A4 to A7 are ignored.
Once a 50h command has been issued, the pointer moves to the redundant cell locations and only those 8 cells can be addressed, regardless of the value of the A4 to A7 address. (An 00h command is necessary to move the pointer back to the 0 to 255 main memory cell location.)

Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass/fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port on the $\overline{RE}$ clock after a Status Read command "70h" input. The resulting information is outlined in Table 5.

Table 5. Status output table for Status Read command "70h"

	STATUS	OUTPUT	
I/O1	Pass/Fail	Pass: 0	Fail: 1
I/O2	Not Used	0	
I/O3	Not Used	0	
I/O4	Not Used	0	
I/O5	Not Used	0	
I/O6	Not Used	0	
I/O7	Ready/Busy	Ready: 1	Busy: 0
I/O8	Write Protect	Protect: 0	Not Protected: 1

The Pass/Fail status on I/O1 is only valid when the device is in the Ready state. I/O9 to I/O16 are not used.

An application example with multiple devices is shown in Figure 7.

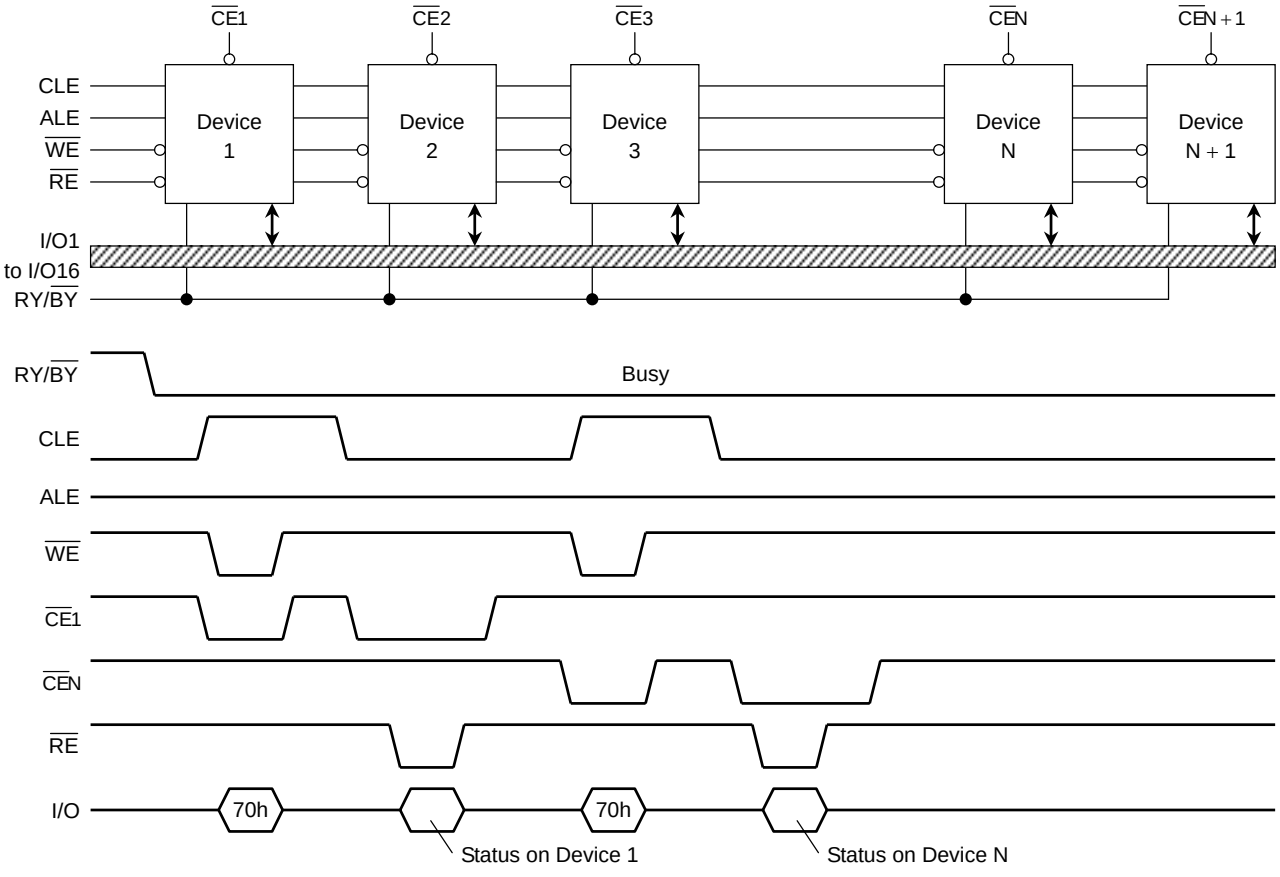


Figure 7. Status Read timing application example

System Design Note: If the $RY/\overline{BY}$ pin signals from multiple devices are wired together as shown in the diagram, the Status Read function can be used to determine the status of each individual device.

Auto Page Program

The device carries out an Automatic Page Program operation when it receives a "10h" Program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detailed timing chart.)

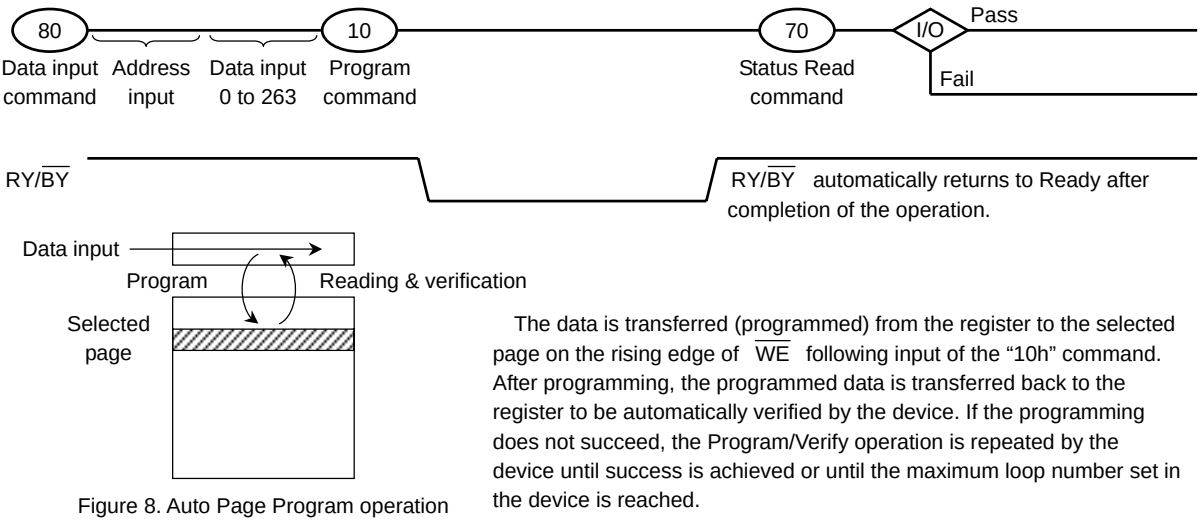
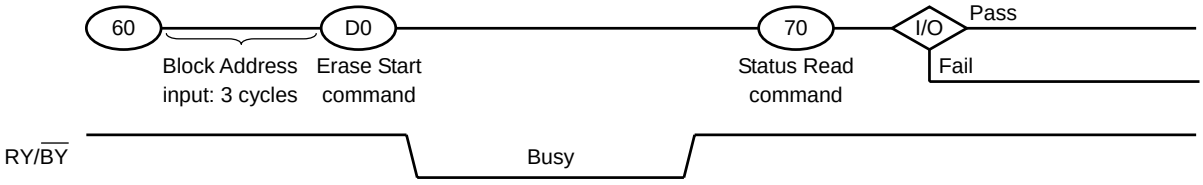


Figure 8. Auto Page Program operation

The data is transferred (programmed) from the register to the selected page on the rising edge of $\overline{WE}$ following input of the "10h" command. After programming, the programmed data is transferred back to the register to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Auto Block Erase

The Auto Block Erase operation starts on the rising edge of $\overline{WE}$ after the Erase Start command "D0h" which follows the Erase Setup command "60h". This two-cycle process for Erase operations acts as an ertra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.



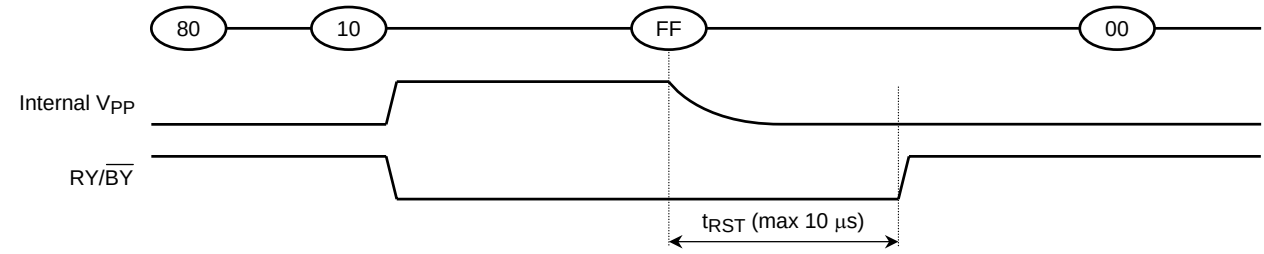
Reset

The Reset mode stops all operations. For example, in the case of a Program or Erase operation the internally generated voltage is discharged to 0 volts and the device enters Wait state.

The response to an "FFh" Reset command input during the various device operations is as follows:

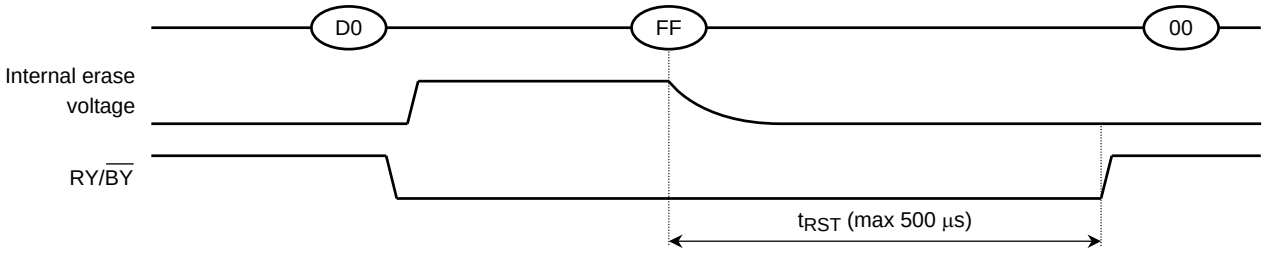
When a Reset (FFh) command is input during programming

Figure 9



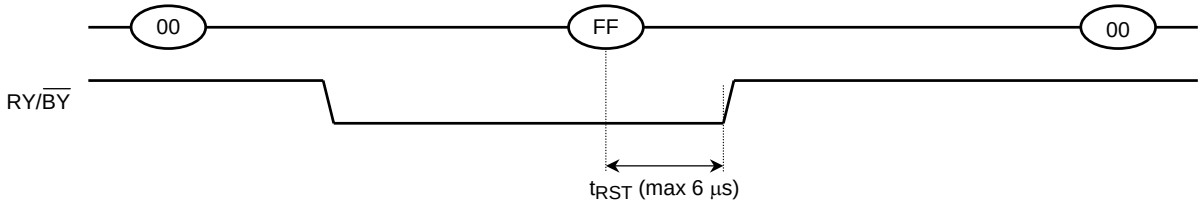
When a Reset (FFh) command is input during erasing

Figure 10.



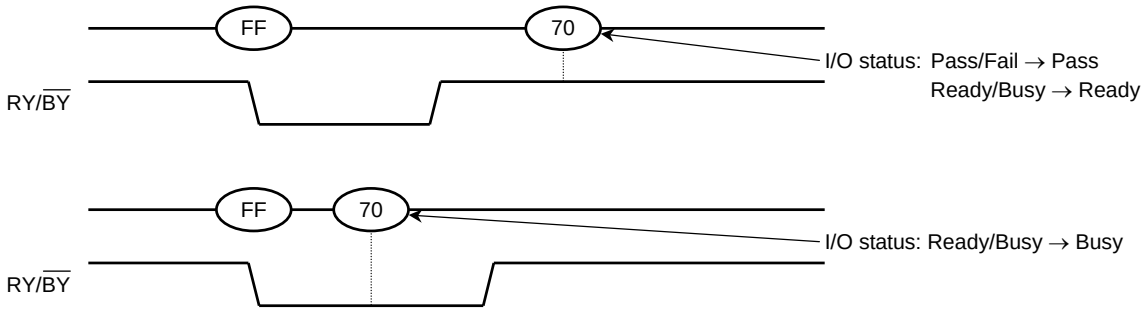
When a Reset (FFh) command is input during Read operation

Figure 11.



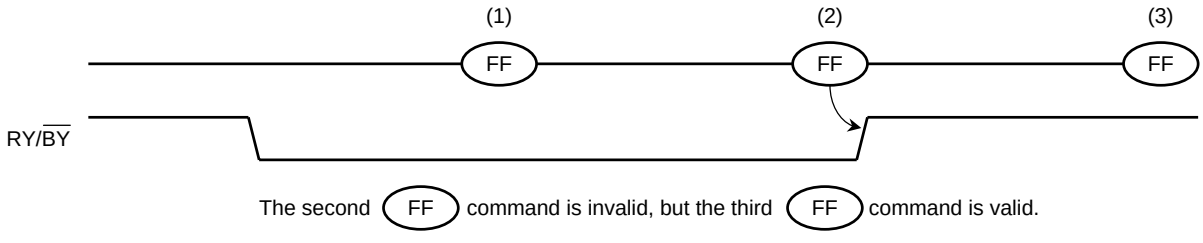
When a Status Read command (70h) is input after a Reset

Figure 12.



When two or more Reset commands are input in succession

Figure 13.



ID Read (1)

The device has 2 types of ID read command, i.e. ID Read (1) command 90h and ID Read (2) command 91h.

ID Read (1) command 90h provides maker code and device code. The ID codes can be read out under the following timing conditions:

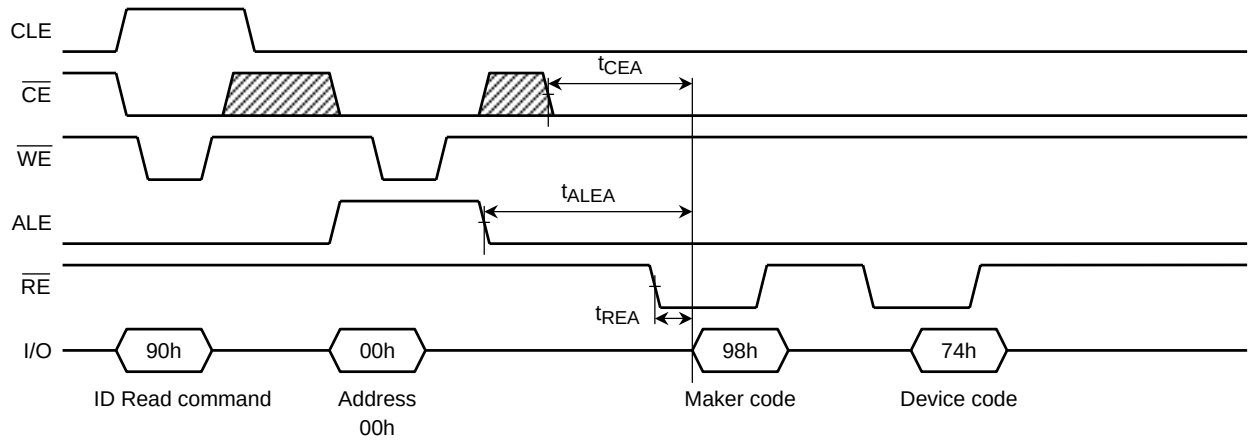


Figure 13. ID Read timing

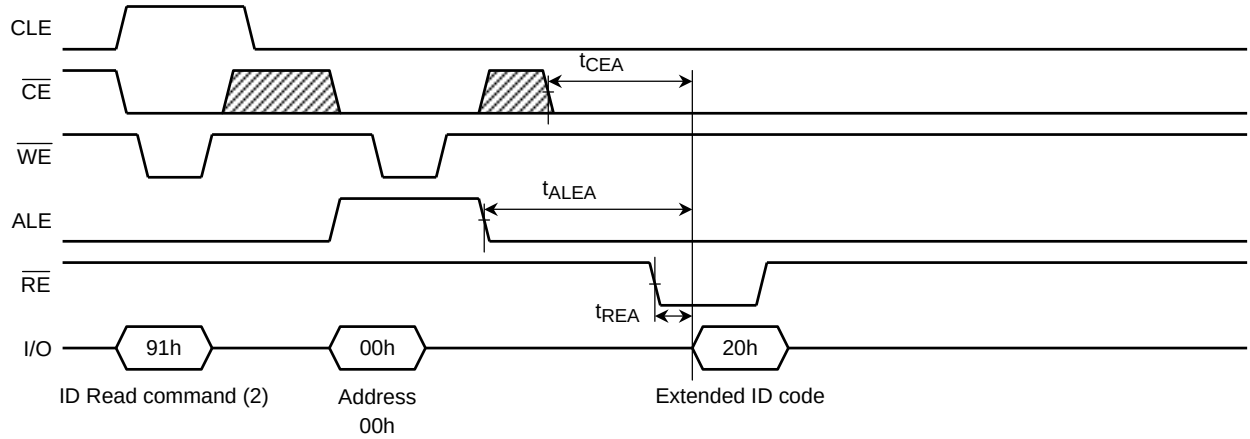
Table 6. ID Codes read out by ID read command 90h

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
Maker code	1	0	0	1	1	0	0	0	98h
Device code	0	1	1	1	0	0	1	0	72h

I/O9 to I/O16 are '0'.

ID Read (2)

ID Read (2) command 91h provides ×4-block mode availability. If ID code read out by 91h is 20h, it indicates the device has ×4-block mode.



For the specifications of the access times t_{REA}, t_{CEA} and t_{ALEA} refer to the AC Characteristics.

Figure 14. ID Read timing

Table 7. ID Codes read out by command 91h

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
Extended ID code	0	0	1	0	0	0	0	0	20h

I/O 9 to I/O 16 are 0

APPLICATION NOTES AND COMMENTS

(1) Power-on/off sequence:

The $\overline{WP}$ signal is useful for protecting against data corruption at power-on/off. The following timing sequence is necessary.

The $\overline{WP}$ signal may be negated any time after the V_{CC} reaches 1.5 V and $\overline{CE}$ signal is kept high in power up sequence.

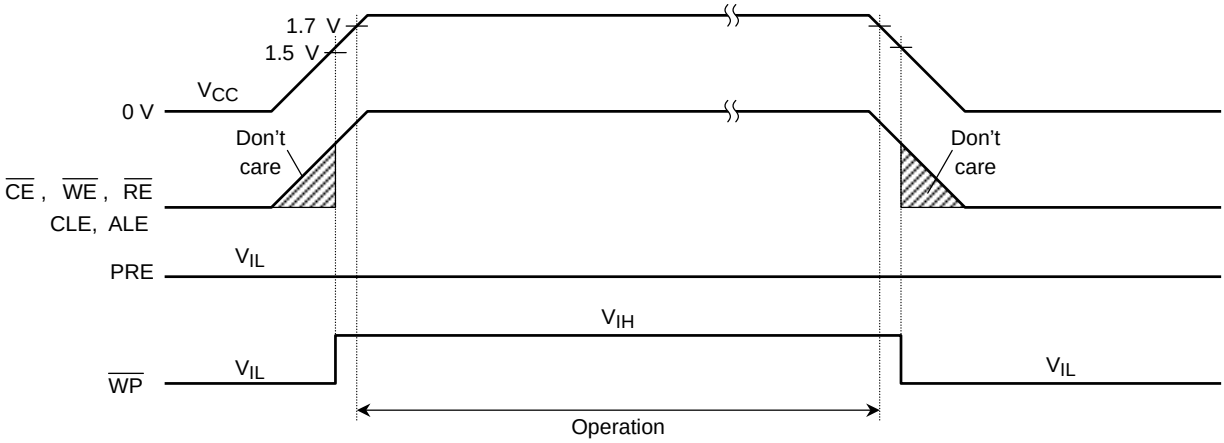


Figure 15. Power-on/off Sequence

In order to operate this device stably, after V_{CC} becomes 1.5V, it should begin access after about 1ms.

(2) Status after power-on

The following sequence is necessary when not using Power-on auto read mode (Boot Block Read).

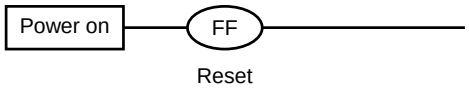


Figure 16.

(3) Prohibition of unspecified commands

The operation commands are listed in Table 4. Input of a command other than those specified in Table 4 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

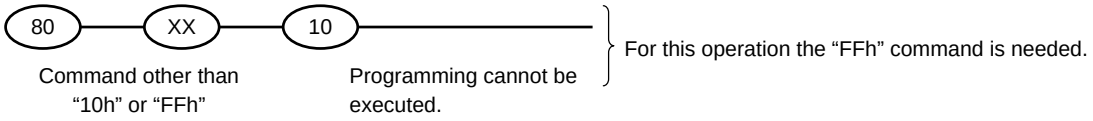
(4) Restriction of command while Busy state

During Busy state, do not input any command except 70h and FFh.

(5) Acceptable commands after Serial Input command "80h"

Once the Serial Input command "80h" has been input, do not input any command other than the Program Execution command "10h" or the Reset command "FFh".

If a command other than "10h" or "FFh" is input, the Program operation is not performed.



(6) Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited.

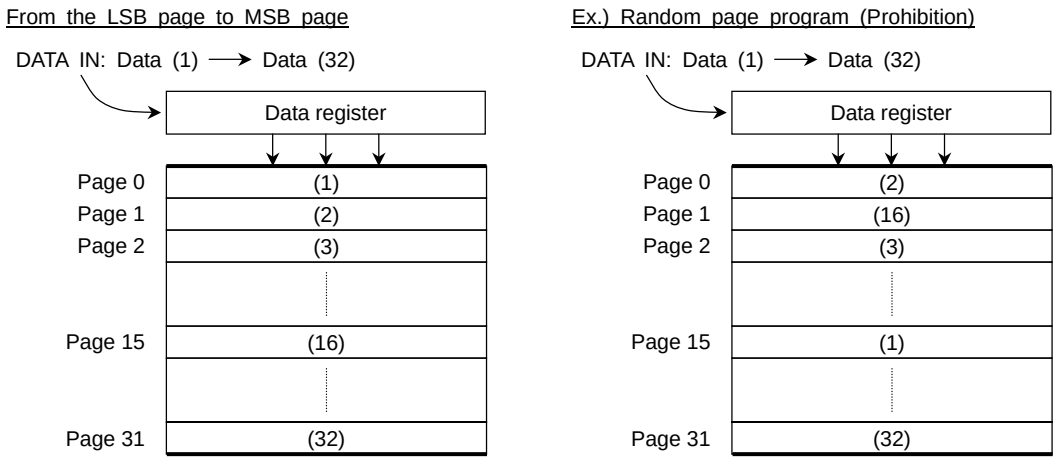


Figure 17. page programming within a block

(7) Status Read during a Read operation

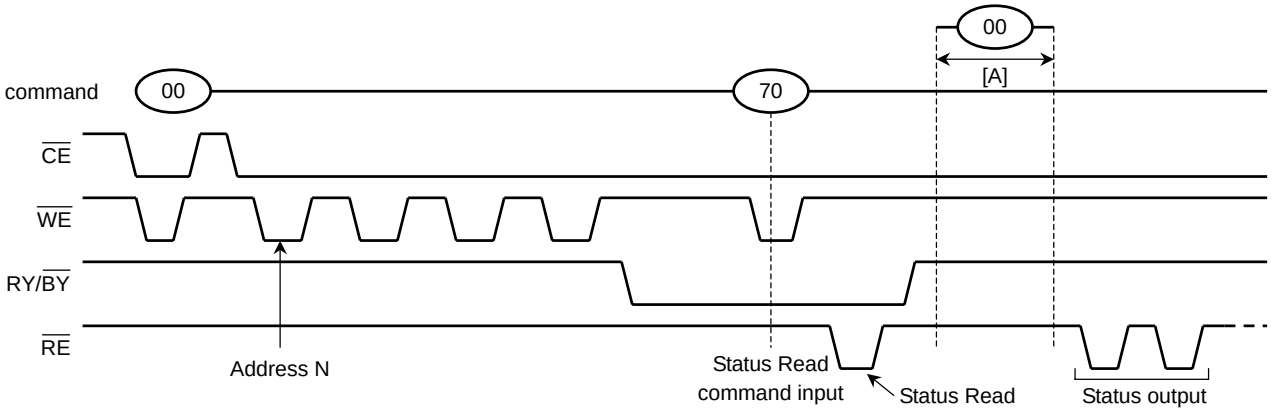


Figure 18.

The device status can be read out by inputting the Status Read command "70h" in Read mode.

Once the device has been set to Status Read mode by a "70h" command, the device will not return to Read mode.

Therefore, a Status Read during a Read operation is prohibited.

However, when the Read command "00h" is input during [A], Status mode is reset and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary

(8) Pointer control for “00h” and “50h”

The device has two Read modes which set the destination of the pointer. Table 7 shows the destination of the pointer, and Figure 19 is a block diagram of their operations.

Table 7. Pointer Destination

Read Mode	Command	Pointer
(1)	00h	0 to 255
(2)	50h	256 to 263

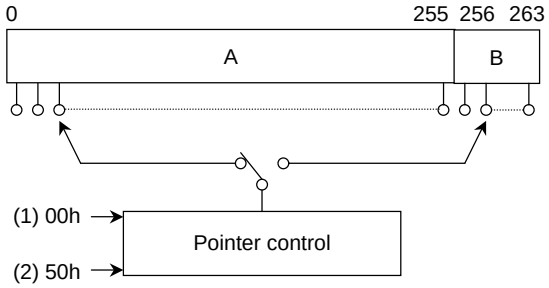
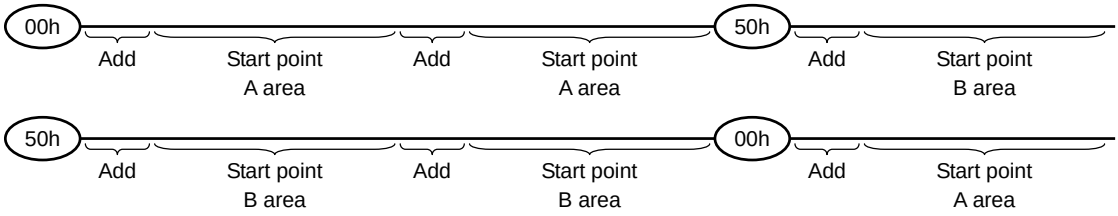


Figure 19 Pointer control

The pointer is set to region A by the “00h” command and to region B by the “50h” command.

(Example)

The “00h” command must be input to set the pointer back to region A when the pointer is pointing to region B.



To program region B only, set the start point to region B using the 50h command.

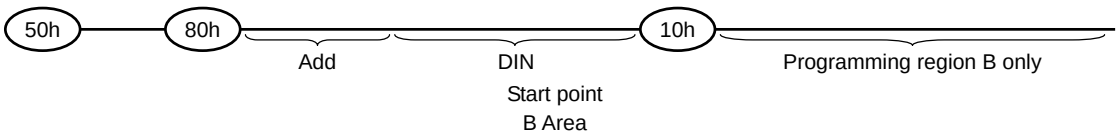


Figure 20. Example of How to Set the Pointer

(9) RY/$\overline{BY}$: termination for the Ready/Busy pin (RY/$\overline{BY}$)

A pull-up resistor needs to be used for termination because the RY/$\overline{BY}$ buffer consists of an open drain circuit.

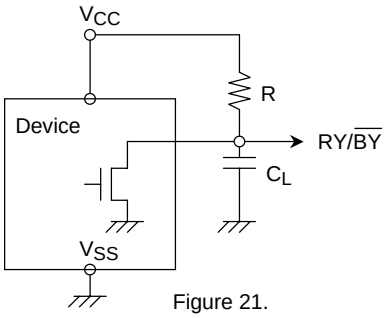
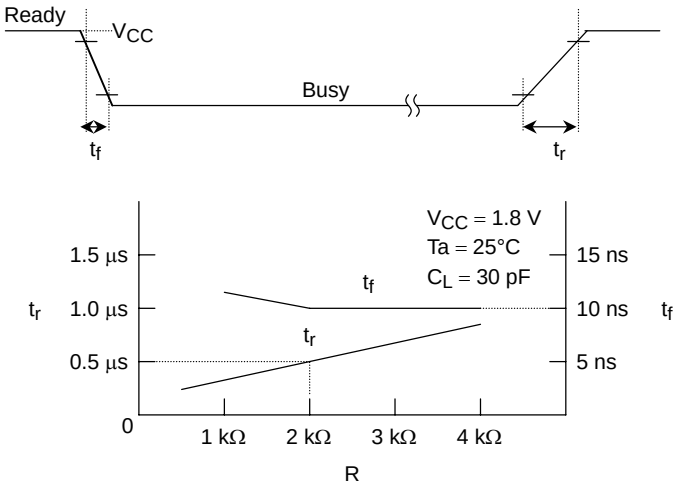


Figure 21.

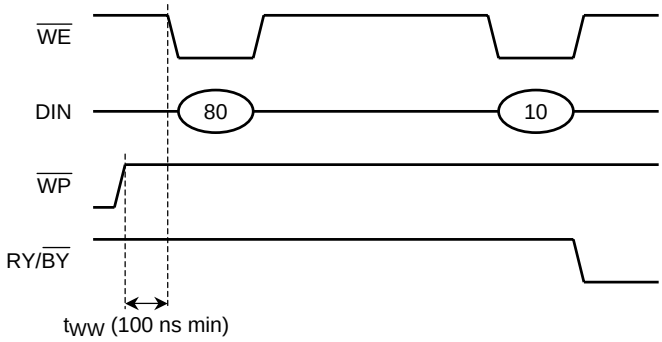


This data may vary from device to device.
We recommend that you use this data as a reference when selecting a resistor value.

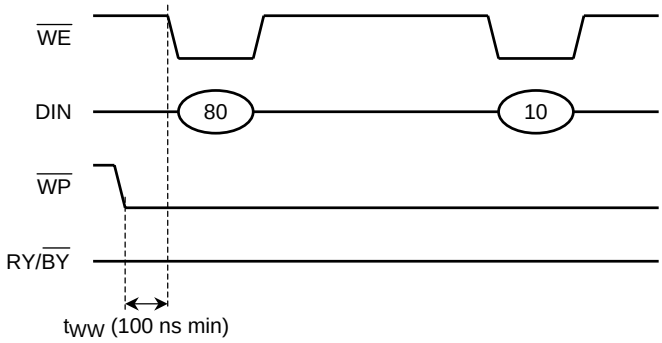
(10) Note regarding the $\overline{WP}$ signal

The Erase and Program operations are automatically reset when $\overline{WP}$ goes Low. The operations are enabled and disabled as follows:

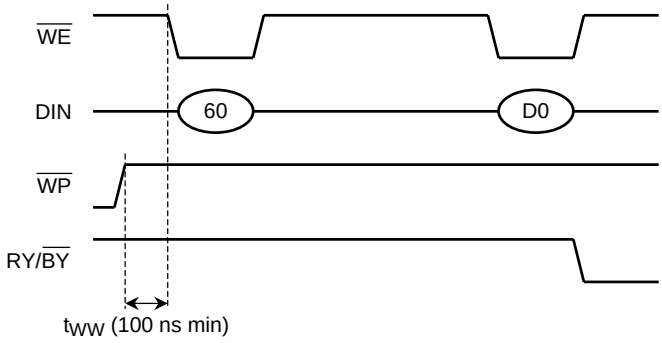
Enable Programming



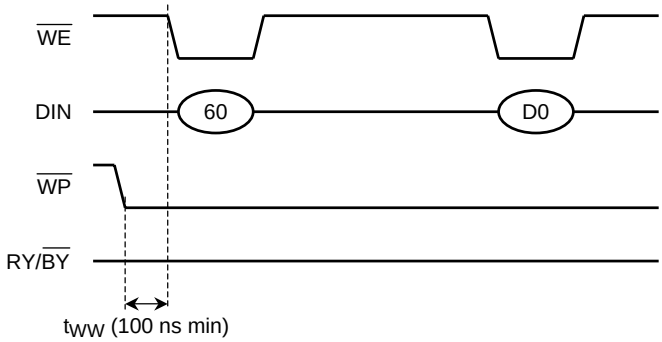
Disable Programming



Enable Erasing



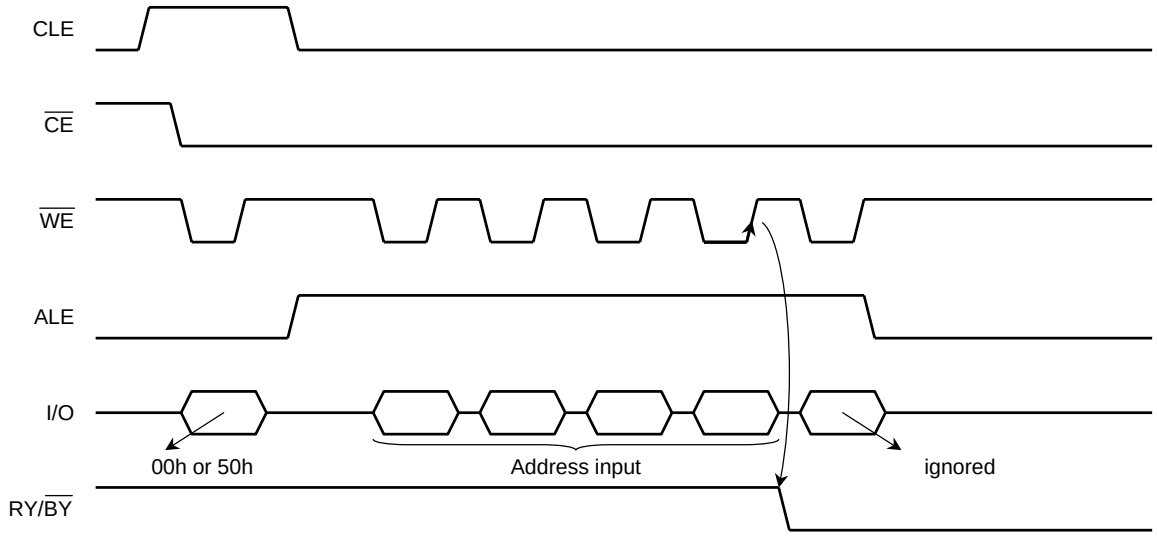
Disable Erasing



(11) When five address cycles are input

Although the device may read in a fifth address, it is ignored inside the chip.

Read operation



Internal read operation starts when $\overline{WE}$ goes High in the fourth cycle.

Figure 22.

Program operation

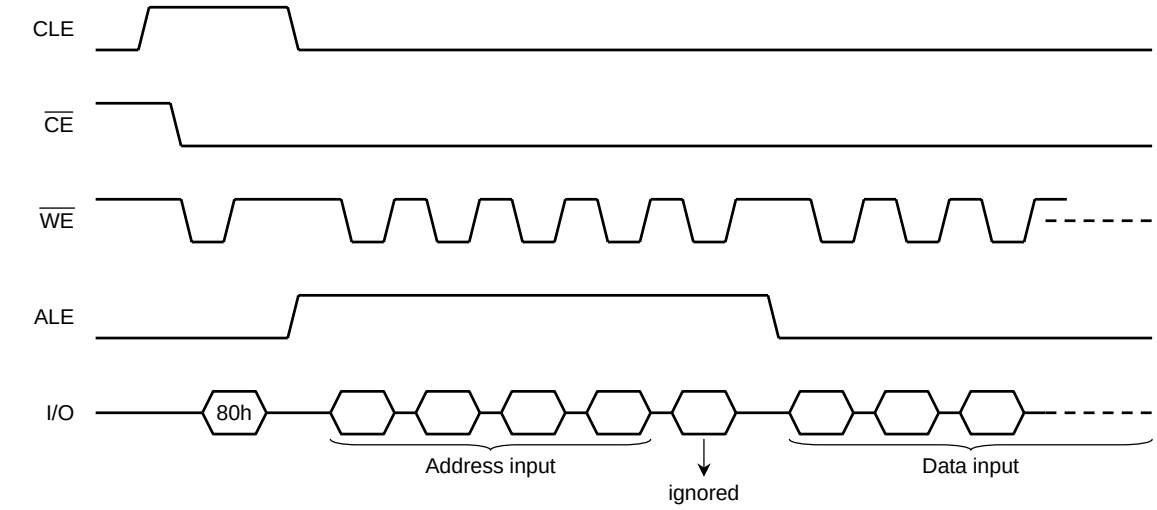


Figure 23.

(12) Several programming cycles on the same page (Partial Page Program)

A page can be divided into up to 3 segments. Each segment can be programmed individually as follows:

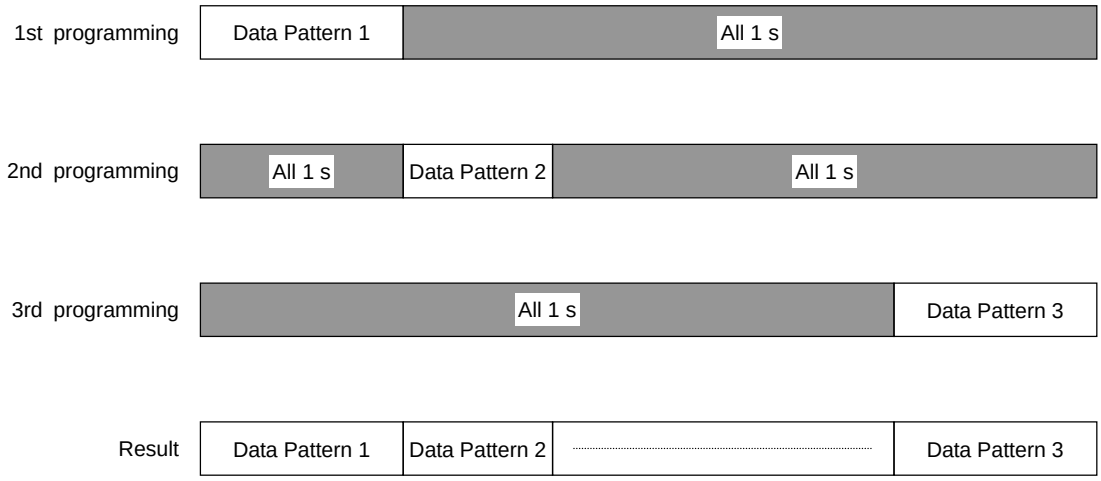


Figure 24.

Note: The input data for unprogrammed or previously programmed page segments must be "1"

(13) Note regarding the $\overline{RE}$ signal

$\overline{RE}$ The internal column address counter is incremented synchronously with the $\overline{RE}$ clock in Read mode. Therefore, once the device has been set to Read mode by a "00h" or "50h" command, the internal column address counter is incremented by the $\overline{RE}$ clock independently of the address input timing, If the $\overline{RE}$ clock input pulses start before the address input, and the pointer reaches the last column address, an internal read operation (array to register) will occur and the device will enter Busy state. (Refer to Figure 25.)

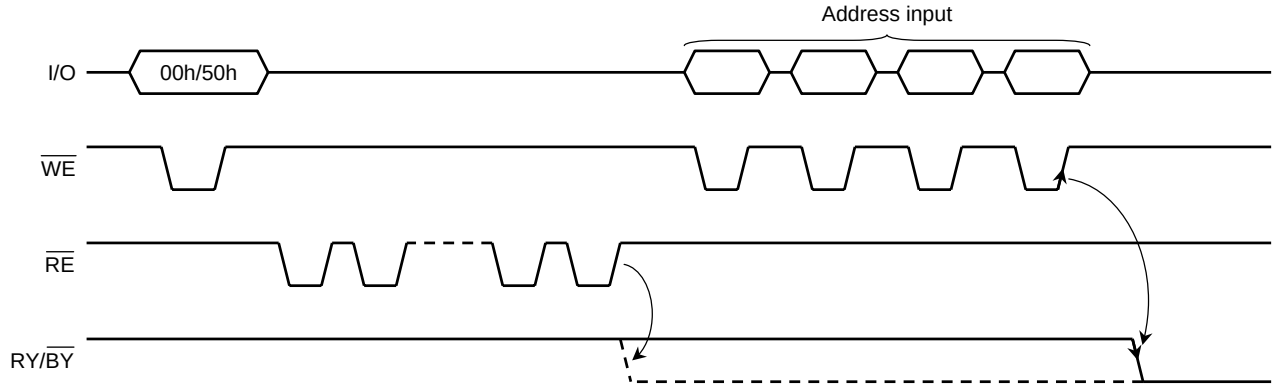


Figure 25.

Hence the $\overline{RE}$ clock input must start after the address input.

(14) Invalid blocks (bad blocks)

The device contains unusable blocks. Therefore, at the time of use, please check whether a block is bad and do not use these bad blocks.

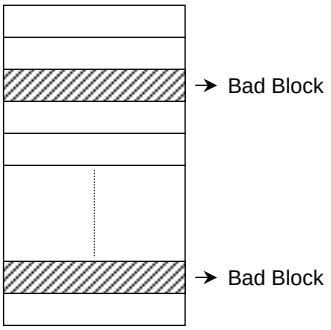


Figure 26.

At the time of shipment, all data words in a Valid Block are FFFFh. For Bad Block, all words are not in the FFFFh state. Please don't perform erase operation to Bad Block.

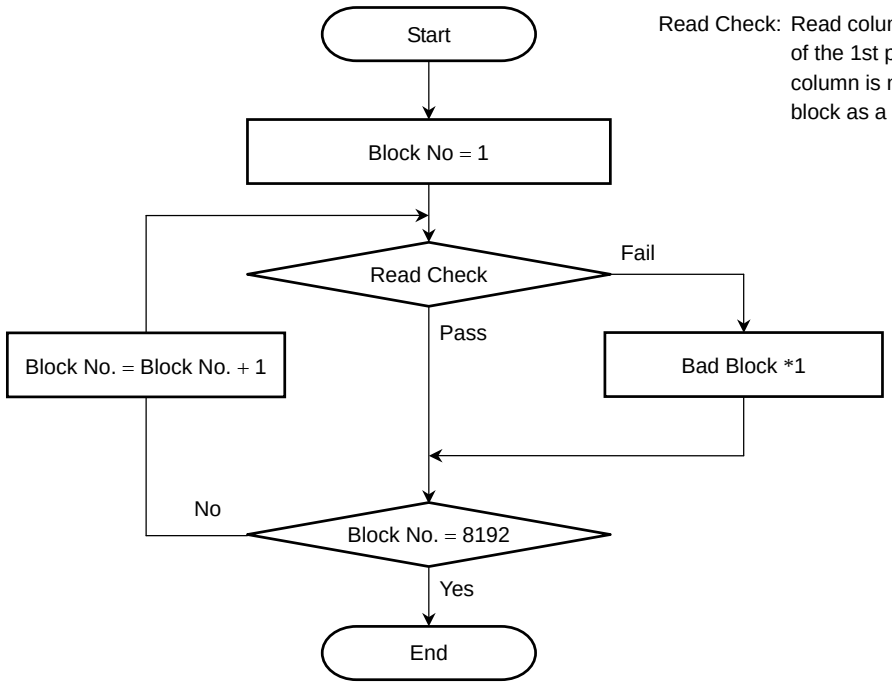
Check if the device has any bad blocks after installation into the system. Figure 27 shows the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.

A bad block does not affect the performance of good blocks because it is isolated from the Bit line by the Select gate

The number of valid blocks at the time of shipment is as follows:

	MIN	TYP.	MAX	UNIT
Valid (Good) Block Number	8032	—	8192	Block

Bad Block Test Flow



Read Check: Read column address 256 or 261 of the 1st page in the block. If the column is not FFFFh, define the block as a bad block.

*1: No erase operation is allowed to detected bad blocks

Figure 27

(15) Failure phenomena for Program and Erase operations

The device may fail during a Program or Erase operation.
The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Single Bit	Programming Failure 1 → 0	ECC

- ECC: Error Correction Code
- Block Replacement

Program

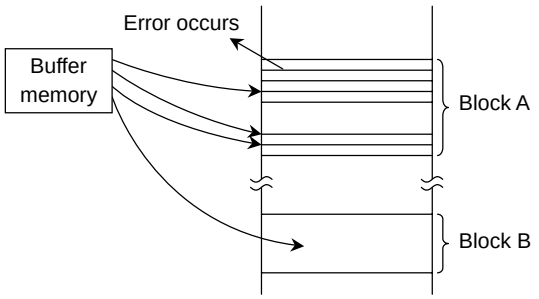


Figure 28.

When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using an another appropriate scheme).

Erase

When an error occurs in an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

(16) Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before write/erase operation is complete will cause loss of data and/or damage to data.

1G Byte GBNAND
THGVS1G3D1CXGI1

Application

This document describes the specifications of the Toshiba GBNAND.
To commence the design of the host system for this device, please confirm the latest information and refer the 7.Host Interface design notes.

1. Product Overview

Toshiba GBNAND is a NAND flash memory device which has NAND memory controller function internally .
Host interface (functional, electrical) is based on SD card. Host can read/write high capacity NAND flash memory easily and efficiently without implementing complex flash memory access procedure.

2. Features

Table 1 : Features

Media Format

Security Functions	SD Security Specification Ver.1.01 Compliant (CPRM Based) *CPRM: Contents Protection for Recording Media Specification
Logical Format	SD File System Specification Ver.1.01 Compliant (DOS-FAT Based formatted)

Electrical

Electrical	Operating Voltage: 2.7V to 3.6 V (Memory Operation) Interfaces: SD Card Interface, (SD: 4 or 1bit) SPI Mode Compatible SD Physical Layer Specification Ver.1.01 Compliant

3. Compatibility

Compliant Specifications

- Host interface
  SD Memory Card Specifications
  - Compliant with PHYSICAL LAYER SPECIFICATION Ver.1.01. (Part1) (Except for Mechanical Specification)
  - Compliant with FILE SYSTEM SPECIFICATION Ver.1.01. (Part2)
  - Compliant with SECURITY SPECIFICATION Ver.1.01. (Part3)

Supplementary Explanation are described in " 6.Others: Limited Conditions, SD Specification Compliance" in this document.

4. Electrical Interface

4.1 Pin Description

Table 2 : Pin Description

SD Mode			SPI Mode				
Name	IO type (1)	Description	Name	IO Type	Description		
CD/ DAT3	I/O /PP	Card Detect/ Data Line [Bit3]	CS	I	Chip Select (Negative True)		
CMD	PP	Command/Response	DI	I	Data In		
CLK	I	Clock	SCLK	I	Clock		
DAT0	I/O /PP	Data Line [Bit0]	DO	O/PP	Data Out		
DAT1	I/O /PP	Data Line [Bit1]	RSV	-	Reserved (2)		
DAT2	I/O /PP	Data Line [Bit2]	RSV	-	Reserved (2)		
$V_{dd}1$	S	Power Supply Voltage 1(3)					
$V_{dd}2$		Power Supply Voltage 2(3)					
$V_{dd}3$		Power Supply Voltage 3(3)					
V_{ss}		Ground					
CKCRI	OSC	CR Clock Oscillator Pins.(4) Connects to the external capacitor and resisters of oscillation.					
CKCRO							
CKCRA							
TST2	T(I)	Test Mode setting.(5)					
TST0	T(I)						
TESTOUT1	T(O)	Test Clock Output (5)					

(1) S: Power Supply, I: Input, O: Output, I/O: Bi-directionally, 'PP' - IO using push-pull drivers
T(I): Test Pin (Input), T(O): Test Pin (Output), OSC: CR Oscillator

(2) These signals should be pulled up by host side with 10-100k ohm resistance in the SPI Mode.

(3) All $V_{dd}1$, $V_{dd}2$, and $V_{dd}3$ have to be connected to the common power supply source (2.7V – 3.6V) externally.

(4) Typical frequency is 896KHz. (See 4.2.1)

(5) For normal operation mode, TST2 and TST0 have to be open or 0V.
TST2 and TST0 are pull-downed to V_{ss} internally.
For clock oscillation test mode, set TST2 and TST0 to "High" level.
In this case, x784/32 clock (typically 22MHz) of CR oscillation is outputted from TESTOUT1.

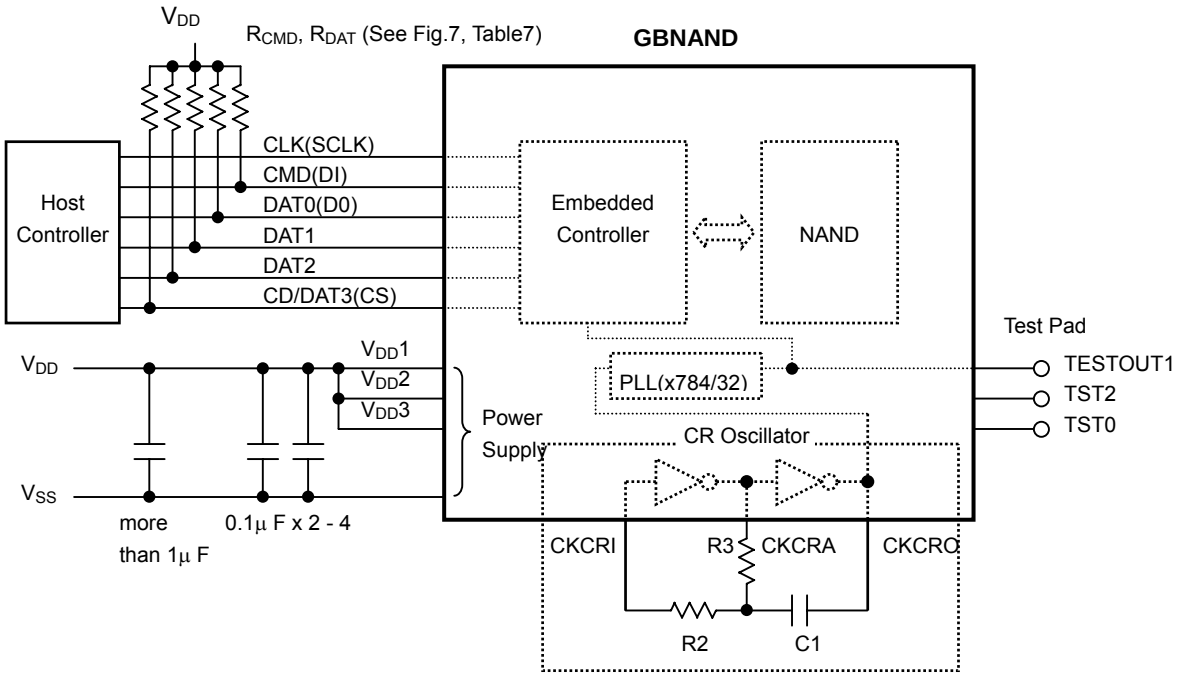


Fig.1-1: Pin connection

4.2 External connections and external parts

Fig.1-1 shows the external connections and external parts for this device
The following external parts are necessary.

For CR oscillation: One capacitance(C1) and two resisters(R2, R3)
Decoupling capacitance for power supply line
Pull-Up registers for SD bus lines (same as SD memory card)

4.2.1 External connections and external parts

This device works by CR oscillation clock.
C1, R2 and R3 decides the CR oscillation frequency.
CR oscillation frequency has to be 896 KHz + 8%, -10% (Ta=25 degree, VDD=3.3V), +14%, -16% (all Ta range and all VDD range) for this device.
Recommended values of C1, R2, R3 are :

C1: 100pF +-5%
R2: 24KOhm ±0.5% or ±1%
R3: 2.2KOhm ±0.5% or ±1%
(*)Each C, R should be low temperature coefficient type.
(Notice)

- CR oscillation frequency and the stability may be influenced by printed circuit board layout, printed circuit board materials, temperature, power supply voltage .
  Please evaluate the CR oscillation with customer's actual printed circuit board and check the frequency and the stability.
  If the recommended C and R values above are not seems suitable, please contact Toshiba.
- Pattern layout between CKCRI , CRCRA, CKCRO, C1, R2, R3 should be as short and wide as possible, and the patters should be connected without through-holes for stable oscillation.
  Fig.1-2 and Fig.1-3 show the recommended pattern layout around the oscillation pins.
- When TST2-pin and TST0-pin are set into "High" level, x784/32 clock of CR oscillator is outputted from TESTOUT1 pin. (Typically 22MHz. It is multiplied by an internal PLL circuit.)
  (Please supply VDD only and don't assert SD commands to the device when measuring PLL output frequency with TESTOUT1, TST0, TST2 pins.)
  This test mode can be used for frequency evaluation and test.
  It is recommended to prepare test-pads for TST2, TST0 and TESTOUT1 on the printed circuit board to use this test mode.
  Make sure that TST2 and TST0 must be open or "Low" level and TESTOUT1 must be open in the normal operation mode.

4.2.2 Power Supply

All Vdd1, Vdd2, and Vdd3 have to be connected to the common power supply source (2.7V – 3.6V) externally.
More than 1μF capacitance and two – four 0.1μF ceramic capacitances should be implemented for power supply decoupling.
Printed circuit board pattern for power supply and decoupling capacitances should be wide and short.
(Notice)

Suitable decoupling capacitance value may depend on power supply characteristics and power supply control method.
Please evaluate the suitable decoupling capacitance value with your actual product.

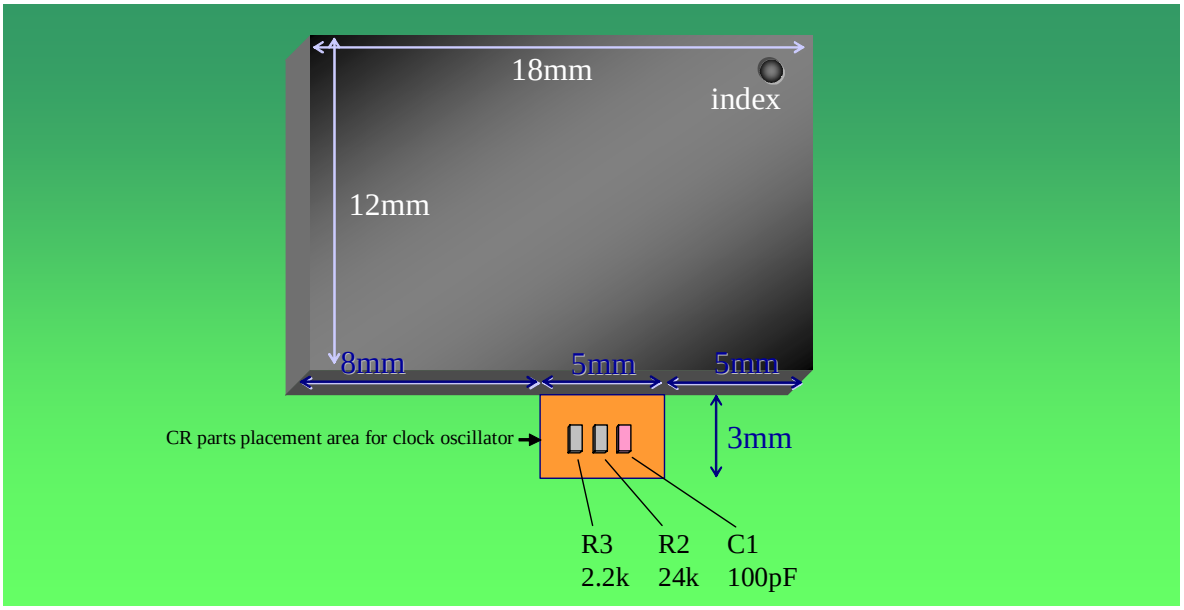


Fig.1-2: External Parts Layout (Recommendation)

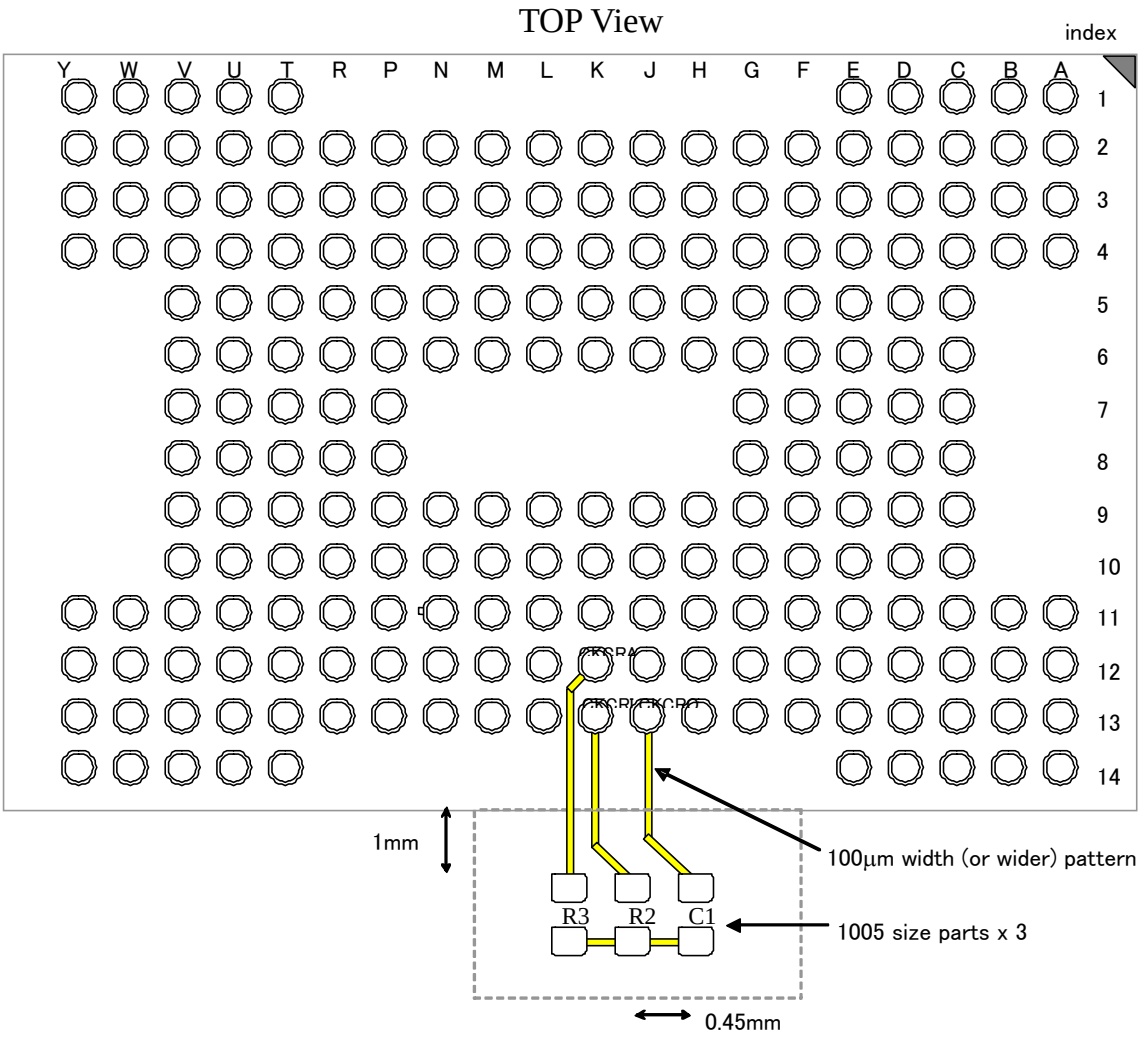


Fig.1-3: PWB Pattern Layout (Recommendation)

4.3 Bus Topology

The device supports two alternative communication protocols: SD and SPI Bus Mode. It is as same as standard SD memory card.
Host System can choose either one of modes. Same Data of the device can read and write by both modes.
SD Mode allows the 4-bit high performance data transfer. SPI Mode allows easy and common interface for SPI channel.
The disadvantage of this mode is loss of performance, relatively to the SD mode.

4.3.1 SD Bus Mode Protocol

The SD bus allows the dynamic configuration of the number of data line from 1 to 4 Bi-directional data signal.
After power up by default, the Device will use only DAT0. After initialization, host can change the bus width.
Multiplied SD cards connections are available to the host. Common V_{dd}, V_{ss} and CLK signal connections are available in the multiple connections. However, Command, Respond and Data lined (DAT0-DAT3) shall be divided for each card from host.
This feature allows easy trade off between hardware cost and system performance. Communication over the SD bus is based on command and data bit stream initiated by a start bit and terminated by stop bit.

Command:
Commands are transferred serially on the CMD line. A command is a token to starts an operation from host to the card. Commands are sent to an addressed single card (addressed Command) or to all connected cards (Broad cast command).

Response:
Responses are transferred serially on the CMD line.
A response is a token to answer to a previous received command. Responses are sent from an addressed single card or from all connected cards.

Data:
Data can be transfer from the card to the host or vice versa.
Data is transferred via the data lines.

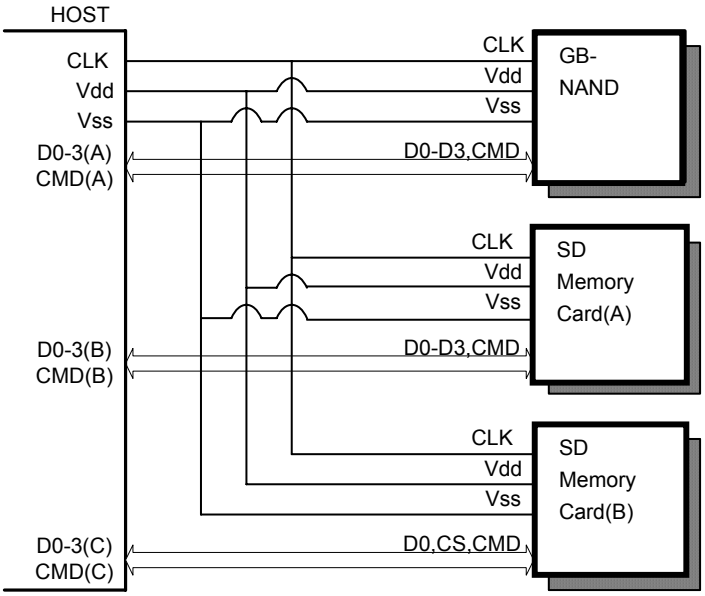


Fig 4: Bus connection Diagram (SD Mode)

CLK:	Host card Clock signal
CMD:	Bi-directional Command/ Response Signal
DAT0 - DAT3:	4 Bi-directional data signal
V_{dd}:	Power supply
V_{ss}:	GND

Table 3: SD Mode Command Set
(+: Implemented, -: Not Implemented)

CMD Index	Abbreviation	Implementation	Note
CMD0	GO_IDLE_STATE	+	
CMD2	ALL_SEND_CID	+	
CMD3	SEND_RELATIVE_ADDR	+	
CMD4	SET_DSR	-	DSR Register is not implemented.
CMD7	SELECT/DESELECT_CARD	+	
CMD9	SEND_CSD	+	
CMD10	SEND_CID	+	
CMD12	STOP_TRANSMISSION	+	
CMD13	SEND_STATUS	+	
CMD15	GO_INACTIVE_STATE	+	
CMD16	SET_BLOCKLEN	+	
CMD17	READ_SINGLE_BLOCK	+	
CMD18	READ_MULTIPLE_BLOCK	+	
CMD24	WRITE_BLOCK	+	
CMD25	WRITE_MULTIPLE_BLOCK	+	
CMD27	PROGRAM_CSD	+	
CMD28	SET_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD29	CLR_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD30	SEND_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD32	ERASE_WR_BLK_START	+	
CMD33	ERASE_WR_BLK_END	+	
CMD38	ERASE	+	
CMD42	LOCK_UNLOCK	+	
CMD55	APP_CMD	+	
CMD56	GEN_CMD	-	This command is not specified.
ACMD6	SET_BUS_WIDTH	+	
ACMD13	SD_STATUS	+	
ACMD22	SEND_NUM_WR_BLOCKS	+	
ACMD23	SET_WR_BLK_ERASE_COUNT	+	
ACMD41	SD_APP_OP_COND	+	
ACMD42	SET_CLR_CARD_DETECT	+	
ACMD51	SEND_SCR	+	
ACMD18	SECURE_READ_MULTI_BLOCK	+	
ACMD25	SECURE_WRITE_MULTI_BLOCK	+	
ACMD26	SECURE_WRITE_MKB	+	
ACMD38	SECURE_ERASE	+	
ACMD43	GET_MKB	+	
ACMD44	GET_MID	+	
ACMD45	SET_CER_RN1	+	
ACMD46	SET_CER_RN2	+	
ACMD47	SET_CER_RES2	+	
ACMD48	SET_CER_RES1	+	
ACMD49	CHANGE_SECURE_AREA	+	

- CMD28, 29,30 and CMD42 are Optional Commands.
- CMD4 is not implemented because DSR register (Optional Register) is not implemented.
- CMD56 is for vender specific command. Which is not defined in the standard card.

4.3.2 SPI Bus Mode protocol

The SPI bus allows 1 bit Data line by 2-chanel (Data In and Out).
The SPI compatible mode allows the MMC Host systems to use SD card with little change.
The SPI bus mode protocol is byte transfers.

All the data token are multiples of the bytes (8-bit) and always byte aligned to the CS signal.

The advantage of the SPI mode is reducing the host design in effort.
Especially, MMC host can be modified with little change.
The disadvantage of the SPI mode is the loss of performance versus SD mode.

Caution: Please use SD Card Specification. DO NOT use MMC Specification.

For example, initialization is achieved by ACMD41, and be careful to Register. Register definition is different, especially CSD Register.

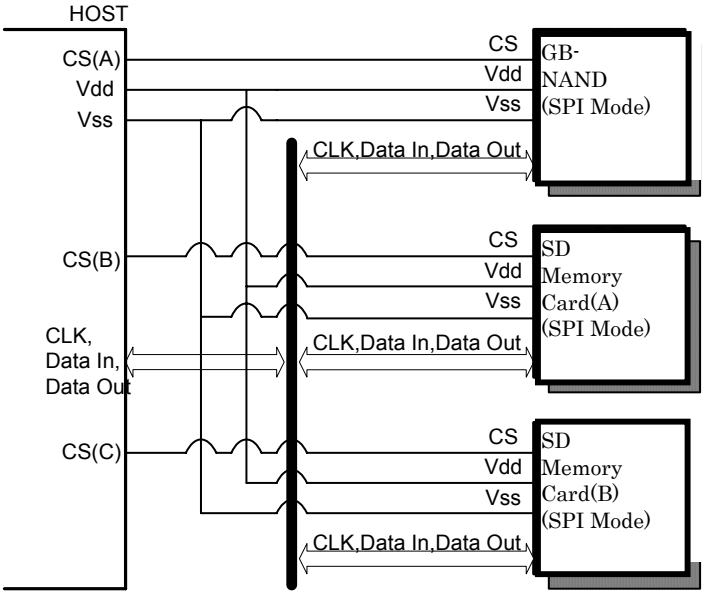


Fig 5: Bus connection Diagram (SPI Mode)

CS:	Card Select Signal
CLK:	Host card Clock signal
Data In:	Host to card data line
Data Out:	Card to host data line
V_{dd}:	Power supply
V_{ss}:	GND

Table.4: SPI Mode Command set
(+: Implemented, -: Not Implemented)

CMD ndex	Abbreviation	Implementation	Note
CMD0	GO_IDLE_STATE	+	
CMD1	SEND_OP_CND	+	NOTICE: DO NOT USE (See Fig.6 and 9.2)
CMD9	SEND_CSD	+	
CMD10	SEND_CID	+	
CMD12	STOP_TRANSMISSION	+	
CMD13	SEND_STATUS	+	
CMD16	SET_BLOCKLEN	+	
CMD17	READ_SINGLE_BLOCK	+	
CMD18	READ_MULTIPLE_BLOCK	+	
CMD24	WRITE_BLOCK	+	
CMD25	WRITE_MULTIPLE_BLOCK	+	
CMD27	PROGRAM_CSD	+	
CMD28	SET_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD29	CLR_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD30	SEND_WRITE_PROT	-	Internal Write Protection is not implemented.
CMD32	ERASE_WR_BLK_START_ADDR	+	
CMD33	ERASE_WR_BLK_END_ADDR	+	
CMD38	ERASE	+	
CMD42	LOCK_UNLOCK	+	
CMD55	APP_CMD	+	
CMD56	GEN_CMD	-	This command is not specified.
CMD58	READ_OCR	+	
CMD59	CRC_ON_OFF	+	
ACMD6	SET_BUS_WIDTH	+	
ACMD13	SD_STATUS	+	
ACMD22	SEND_NUM_WR_BLOCKS	+	
ACMD23	SET_WR_BLK_ERASE_COUNT	+	
ACMD41	SD_APP_OP_COND	+	
ACMD42	SET_CLR_CARD_DETECT	+	
ACMD51	SEND_SCR	+	
ACMD18	SECURE_READ_MULTI_BLOCK	+	
ACMD25	SECURE_WRITE_MULTI_BLOCK	+	
ACMD26	SECURE_WRITE_MKB	+	
ACMD38	SECURE_ERASE	+	
ACMD43	GET_MKB	+	
ACMD44	GET_MID	+	
ACMD45	SET_CER_RN1	+	
ACMD46	SET_CER_RN2	+	
ACMD47	SET_CER_RES2	+	
ACMD48	SET_CER_RES1	+	
ACMD49	CHANGE_SECURE_AREA	+	

- CMD28, 29,30 and CMD42 are Optional Commends.
- CMD56 is for vender specific command. Which is not defined in the standard card.

4.4 Initialization

Initialization procedure for this device is as same as for standard SD card.
To initialize the device, follow the following procedure is recommended example.

1) Supply Voltage for initialization.
   Host System can apply the Operating Voltage from initialization to the card.
   Apply more than 74 cycles of Dummy-clock to the device.
2) Select operation mode (SD mode or SPI mode)
   In case of SPI mode operation, host should drive CD/DAT3 of SD Card I/F to “Low” level. Then, issue CMD0.
   In case of SD mode operation, host should drive or detect CD/DAT3 of SD Card I/F (Pull up register of 1 pin is pull up to “High” normally).
   Card maintain selected operation mode except re-issue of CMD0 or power on below is SD mode initialization procedure.
3) Send the ACMD41 with Arg = 0 and identify the operating voltage range of the Card.
4) Apply the indicated operating voltage to the card.
   Reissue ACMD41 with apply voltage storing and repeat ACMD41 until the busy bit is cleared.
   (Bit 31 Busy = 1) If response time out occurred, host can recognize not SD Card compatible device.
   Note:
      In MMC-SPI Mode, CMD1 can use in this state.
      However, do not use CMD1 in case of SD Mode.
5) Issue the CMD2 and get the Card ID (CID).
   Issue the CMD3 and get the RCA. (RCA value is randomly changed by access, not equal zero)
6) Issue the CMD7 and move to the transfer state.
   If necessary, Host may issue the ACMD42 and disabled the pull up resistor for Card detect.
7) Issue the ACMD13 and poll the Card status as SD Memory Card. Check SD_CARD_TYPE value.
   If significant 8 bits are “all zero”, that means SD Card compatible device. If it is not, stop initialization.
8) Issue CMD7 and move to standby state.
   Issue CMD9 and get CSD.
   Issue CMD10 and get CID.
9) Back to the Transfer state with CMD7.
   Issue ACMD6 and choose the appropriate bus-width.

   Then the Host can access the Data between this device as a storage device.

Recommended Example of SD card Initialize Procedure

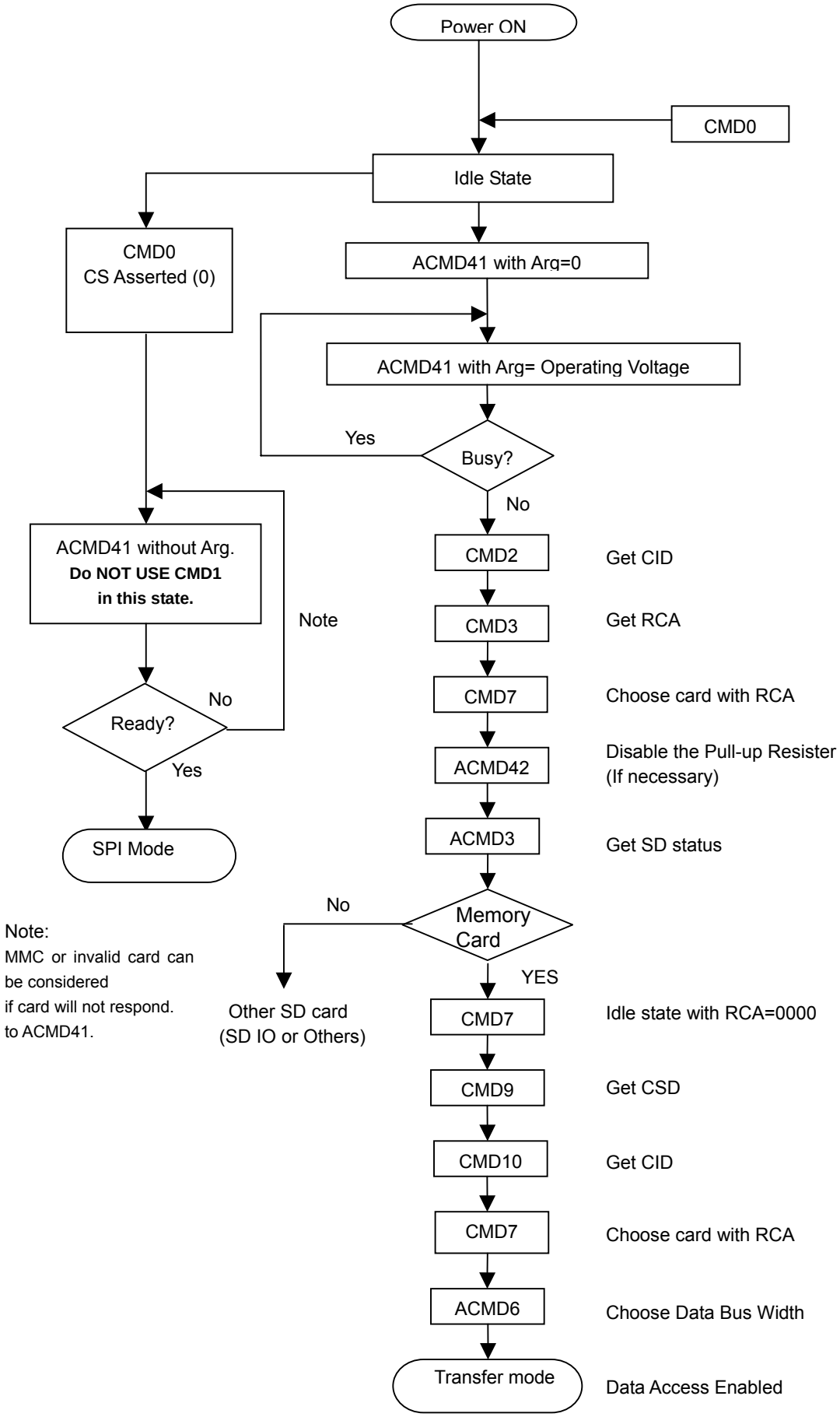


Fig 6. Initialize Procedure

4.5 Electrical Characteristics

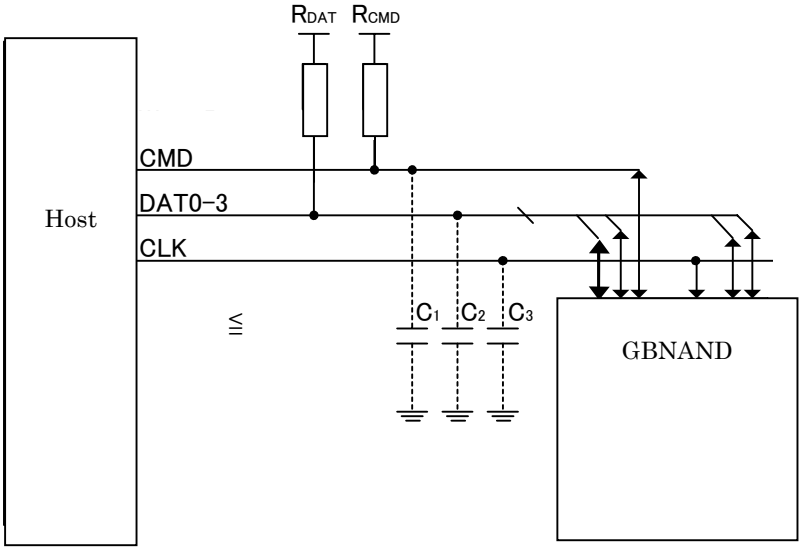


Fig7: Connection diagram

4.5.1 DC Characteristics

Table 6: DC Characteristics

Item		Symbol	Condition	MIN.	Typ.	MAX.	Unit	Note
Supply Voltage 1		V_{DD} (=V_{DD1} =V_{DD2} =V_{DD3})	-	2.0	-	3.6	V	For CMD0, 15,55, ACMD41 Only
Supply Voltage 2			-	2.7	-	3.6	V	For All commands
Input Voltage	High Level	V_{IH}	-	V_{DD} x 0.625	-	-	V	
	Low Level	V_{IL}	-	-	-	V_{DD} x 0.25	V	
Output Voltage	High Level	V_{OH}	V_{DD} = 2V I_{OH} = -100μA	V_{DD} x 0.75	-	-	V	
	Low Level	V_{OL}	V_{DD} = 2V I_{OL} = 100μA	-	-	V_{DD} x 0.125	V	
Standby Current		I_{CC1}(1)	3.6V Clock 25MHz	-	-	30	mA	
			3.0V Clock Stop	-	-	0.25		at 25 °C
Operation Voltage		I_{CC2}(1)	3.6V/25MHz	-	-	80	mA	Write
			3.6V/25MHz	-	-	80		Read
Input Voltage Setup Time		Vrs	-	-	-	250	ms	

(1) V_{DD1} Current + V_{DD2} Current + V_{DD3} Current

Table 7: Signal Capacitance

Item	Symbol	Min.	Max.	Unit	Note
Pull up Resistance	R_{CMD} , R_{DAT}	10	100	K Ohm	
Bus Signal Line Capacitance	C_L	-	250	pF	F_{PP}<5MHz (21Cards)
Bus Signal Line Capacitance	C_L	-	100	pF	F_{PP}<20MHz (7Cards)
Single Card Capacitance	C_{CARD}	-	10	pF	
Pull up Resistance inside card(DAT3)	R_{DAT3}	10	90	K Ohm	

4.5.2 AC Characteristics

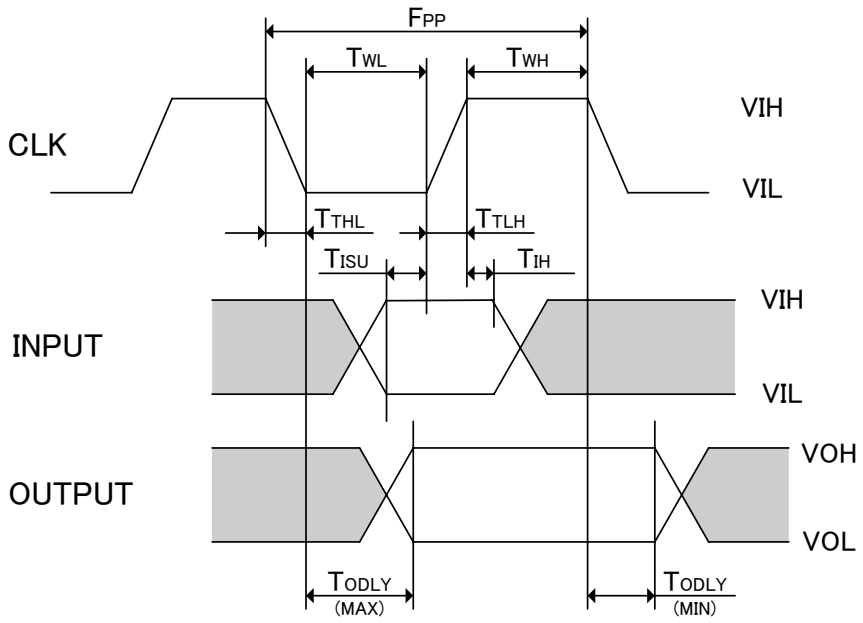


Fig 8: AC Timing Diagram

Table 8: AC Characteristics

Item	Symbol	Min.	Max.	Unit	Note
Clock Frequency (In any Sates)	Fsty	0	25	MHz	CL<100pF (7Cards)
Clock Frequency (Data transfer Mode)	F_{PP}	0.1	25	MHz	CL<100pF (7Cards)
Clock Frequency (Card identification Mode)	F_{OD}	100	400	kHz	CL<250pF (21Cards)
Clock Low Time	T_{WL}	10	-	ns	CL<100pF (7Cards)
Clock High Time	T_{WH}	10	-	ns	
Clock Rise Time	T_{TLH}	-	10	ns	
Clock Fall Time	T_{THL}	-	10	ns	
Clock Low Time	T_{WL}	50	-	ns	CL < 250pF (21Cards)
Clock High Time	T_{WH}	50	-	ns	
Clock Rise Time	T_{TLH}	-	50	ns	
Clock Fall Time	T_{THL}	-	50	ns	
Input Setup Time	T_{ISU}	5	-	ns	CL < 25pF (1Cards)
Input Hold Time	T_{IH}	5	-	ns	
Output Delay Time	T_{ODLY}	0	14	ns	

5. Card Internal Information

5.1 Security Information

MKB (Media Key Block) and Media ID are Toshiba Standard Information. These information are compliance with the CPRM.

Note: The security information is NOT Development information for evaluation.
Host System shall be compliance with the CPRM to use the security function.
This information is kept as confidential because of security reasons.

5.2 SD Card Registers

The SD card has six registers and SD Status information: OCR, CID, CSD, RCA, DSR, SCR and SD Status. DSR IS NOT SUPPORTED in this card.

There are two types of register groups.
MMC compatible registers: OCR, CID, CSD, RCA, DSR, and SCR
SD card Specific: SD Status

Table.9: SD card Registers

Resister Name	Bit Width	Description
OCR	32	Operation Conditions (VDU Voltage Profile and Busy Status Information)
CID	128	Card Identification information
CSD	128	Card specific information
RCA	16	Relative Card Address
DSR	16	Not Implemented (Programmable Card Driver): Driver Stage Register
SCR	64	SD Memory Card's special features
SD Status	512	Status bits and Card features

5.2.1 OCR Register

This 32-bit register describes operating voltage range and status bit in the power supply.
(Refer Appendix 2. for the detail)

Table.10: OCR register definition

OCR bit position	VDD voltage window	Initial value
		1GB
31	Card power up status bit (busy)	"0" = busy "1" = ready
30-24	reserved	All '0'
23	3.6 – 3.5	1
22	3.5 – 3.4	1
21	3.4 – 3.3	1
20	3.3 – 3.2	1
19	3.2 – 3.1	1
18	3.1 – 3.0	1
17	3.0 – 2.9	1
16	2.9 – 2.8	1
15	2.8 – 2.7	1
14	2.7 – 2.6	0
13	2.6 – 2.5	0
12	2.5 – 2.4	0
11	2.4 – 2.3	0
10	2.3 – 2.2	0
9	2.2 – 2.1	0
8	2.1 – 2.0	0
7	2.0 – 1.9	0
6	1.9 – 1.8	0
5	1.8 – 1.7	0
4	1.7 – 1.6	0
3-0	Reserved	All '0'

bit 23-4: Describes the SD Card Voltage
bit 31 indicates the card power up status. Value "1" is set after power up and initialization procedure has been completed.

5.2.2 CID Register

The CID (Card Identification) register is 128-bit width. It contains the card identification information.
(Refer Appendix 3. for the detail) The Value of CID Register is vender specific.

Tabel.11: CID Register

Field	Width	CID-slice	Initial Value
			1GB
MID	8	[127:120]	02 h
OID	16	[119:104]	"TM" (544D h)
PNM	40	[103:64]	" SD01G "
PRV	8	[63:56]	(a) Product revision
PSN	32	[55:24]	(a) Product serial number
-	4	[23:20]	All '0'
MDT	12	[19:8]	(b) Manufacture date
CRC	7	[7:1]	(c) CRC
-	1	[0:0]	1

(a), (b): Depends on the individual device. Controlled by Production Lot.
(c) : Depends on the CID Register

• MID

8 bit binary number, Indicates the Manufacture ID allocated by the SDA.

→ 02 -h (Indicates Toshiba) (Unit: -h means Hex-decimal value, here after)

• OID

16 bit binary number, Indicates the Manufacture ID allocated by the SDA.

→ 544D -h = "TM" in ASCII String (Indicates Toshiba)

• PNM

5 ASCII Characters long (40 bit), Toshiba Product Code.

→ Toshiba Standard SD card indicates as below by capacity.
1GB : "SD01G" (0x5344303147)

• PRV

Product Revision of the card.

→ This number may be changed without any notice by TOSHIBA.

• PSN

32 bit serial number of unsigned integer.

→ Uniquely assigned integer

• MDT

The manufacturing date composed of two-hexadecimal digits.

→ CID-Slice [11:8] Month Field (Exp. 1h = January)
CID-Slice [19:12] Year Field (Exp. 0h = 2000)

• CRC

Checksum of CID contents.

→ CRC 7 Checksum (See Chapter 7. of the SD PHYSICAL SPECIFICATION)

5.2.3 CSD Register

CSD is Card-Specific Data register provides information on 128bit width.
Some field of this register can writable by PROGRAM_CSD (CMD27).

Table.12: CSD Register

Field	Width	Cell Type(1)	CSD slice	Initial Value
				1GMB
CSD_STRUCTURE	2	R	[127:126]	00
-	6	R	[125:120]	All '0'
TAAC	8	R	[119:112]	0_0101_101(200μs)
NSAC	8	R	[111:104]	00000000
TRAN_SPEED	8	R	[103:96]	0_0110_010(25Mbps)
CCC	12	R	[95:84]	0_0_0_1_1_0_1_1_0_1_0_1
READ_BL_LEN	4	R	[83:80]	1001(512Bytes)
READ_BL_PARTIAL	1	R	[79:79]	1
WRITE_BLK_MISALIGN	1	R	[78:78]	0
READ_BLK_MISALIGN	1	R	[77:77]	0
DSR_IMP	1	R	[76:76]	0
-	2	R	[75:74]	All '0'
C_SIZE	12	R	[73:62]	0xF59
VDD_R_CURR_MIN	3	R	[61:59]	111(100mA)
VDD_R_CURR_MAX	3	R	[58:56]	110(80mA)
VDD_W_CURR_MIN	3	R	[55:53]	111(100mA)
VDD_W_CURR_MAX	3	R	[52:50]	110(80mA)
C_SIZE_MULT	3	R	[49:47]	111
ERASE_BLK_EN (Note)	1	R	[46:46]	1
SECTOR_SIZE	7	R	[45:39]	1111111
WP_GRP_SIZE	7	R	[38:32]	0000000
WP_GRP_ENABLE	1	R	[31:31]	0
-	2	R	[30:29]	All '0'
R2W_FACTOR	3	R	[28:26]	101
WRITE_BL_LEN	4	R	[25:22]	1001
WRITE_BL_PARTIAL	1	R	[21:21]	0
-	5	R	[20:16]	All '0'
FILE_FORMAT_GRP	1	R/W(1)	[15:15]	0
COPY	1	R/W(1)	[14:14]	0
PERM_WRITE_PROTECT	1	R/W(1)	[13:13]	0
TMP_WRITE_PROTECT	1	R/W	[12:12]	0
FILE_FORMAT	2	R/W(1)	[11:10]	00
-	2	R/W	[9:8]	All '0'
CRC	7	R/W	[7:1]	(CRC)
-	1	-	[0:0]	1

Cell Types: R: Read Only, R/W: Writable and Readable, R/W(1): One-time Writable / Readable

Note: Erase of one data block is not allowed in this card. This information is indicated by "ERASE_BLK_EN". Host System should refer this value before one data block size erase.

• CSD_STRUCTURE

Version number of the related CSD structure.

Table 12-1:CSD_STRUCTURE

CSD_STRUCTURE	CSD STRUCTURE VERSION	Valid for SD PHYSICAL LAYER SPECIFICATION Version
0	CSD Version 1.0	Version 1.0
1-3	Reserved	

→ Version 1.0 Compliant

• TAAC

Defines the asynchronous part of the data access time.

Table 12-2: TAAC Access Time Definition

TAAC bit	Code
2:0	Time Unit 0 = 1ns,1 = 10ns,2 = 100ns,3 = 1μS,4 = 10μs,5 = 100μs, 6 = 1ms,y = 10ms
6:3	Time Value 0 = Reserved,1 = 1.0,2 = 1.2,3 = 1.3,4 = 1.5,5 = 2.0, 6 = 2.5, 7 = 3.0,8 = 3.5,9 = 4.0,A = 4.5,B = 5.0,C = 5.5,D = 6.0, E = 7.0,F = 8.0
7	Reserved

→ 200 μs

• NSAC

Defines the worst case for the clock dependent factor of the data access time.
Unit is 100 clock cycle.
Total access time equal TAAC plus NSAC, calculation with actual clock frequency.
This is average delay by the first clock out put for data block.

→ 0 clock Cycle

• TRAN_SPEED

The following table defines the maximum data transfer rate per one data line.

Table 12-3: Maximum Data Transfer Rate Definition

TRAN_SPEED bit	Code
2:0	Transfer Rate Unit 0 = 100kbit/s,1 = 1Mbit/s,2 = 10Mbit/s,3 = 100Mbit/s, 4-7 = Reserved
6:3	Time Value 0 = Reserved,1 = 1.0,2 = 1.2,3 = 1.3,4 = 1.5,5 = 2.0,6 = 2.5, 7 = 3.0,8 = 3.5,9 = 4.0,A = 4.5,B = 5.0,C = 5.5,D = 6.0, E = 7.0,F = 8.0
7	Reserved

→ Trans Rate is 25Mbps

• CCC

The Card Class Command Register (CCC) defines which command classes are supported by this card.

Table12-4: Supported Card Command Classes

CCC bit	Supported Card command Class
0	Class 0
1	Class 1
...	
11	Class 11

→ Class 0,2,4,5,7,8, are supported

• READ_BL_LEN

The Maximum read data block length for reading is computed as $2^{READ\_BL\_LEN}$.
READ_BL_LEN is always equal to WRITE_BL_LEN.

Table12-5:DATA Block Length

READ_BL_LEN	Block Length
0-8	Reserved
9	2^9 = 512Bytes
• • •	
11	2^{11} = 2048Bytes
12-15	Reserved

→ 1GB = 512 Bytes

• READ_BL_PARTIAL (Always = 1)

This is always data “1” in SD Memory Card so it can be read by Byte unit for Block data.

→ ”1”:This card can partially readable by Byte unit.

• WRITE_BLK_MISALIGN

Define whether the data block to be written by one command can be spread over more than one physical block of the Flash Memory Device.

Table 12-6:WRITE_BLK_MISALIGN

WRITE_BLK_MISALIGN	Across Block Boundaries Write
0	Not Allowed
1	Allowed

→ ”0”: Not allowed on this card

• READ_BLK_MISALIGN

Define whether the data block to be read by one command can be spread over more than one physical block of the Flash Memory Device.

Table 12-7: READ_BLK_MISALIGN

READ_BLK_MISALIGN	Across Block Boundaries Read
0	Not Allowed
1	Allowed

→ "0": Invalid on this card

• DSR_IMP

If set, a driver stage register (DSR) is implemented (supported).

Table 12-8: DSR_IMP

DSR_IMP	DSR Type
0	DSR NOT Implemented
1	DSR Implemented

→ "0": DSR NOT implemented

• C_SIZE

This parameter is used to compute the user's data card capacity(Not include the security area) as below.

Memory Capacity = BLOCKNR x **BLOCK_LEN**

BLOCKNR = (C_SIZE + 1) x **MULT**

MULT = $2^{C\_SIZ\_MULT+2}$ (C_SIZE_MULT < 8)

BLOCK_LEN = $2^{READ\_BL\_LEN}$ (READ_BL_LEN < 12)

Therefore the maximum capacity of the 64MB card is:

3784x32x512/1024/1024 = 59.125MB

→ The user's data card capacity is as below.

1GB : 982.5MB

• VDD_R_CURR_MIN,VDD_W_CURR_MIN

The maximum values for Read/Write currents at VDD: MINIMUM.

Tab 12-9: VDD_R_CURR_MIN, VDD_W_CURR_MIN

VDD_R_CURR_MIN VDD_W_CURR_MIN	Code for current consumption @ VDU
2:0	0 = 0.5mA, 1 = 1mA, 2 = 5mA, 3 = 10mA, 4 = 25mA, 5 = 35mA, 6 = 60mA, 7 = 100mA

→ 100mA@V_{DD} = 2.7 V (Minimum)

• READ_BLK_MISALIGN

The maximum values for Read/Write currents at VDD : MAXIMUM.

Table 12-10: VDD_R_CURR_MAX, VDD_W_CURR_MAX

VDD_R_CURR_MAX VDD_W_CURR_MAX	R/W current Maximum
2:0	0 = 0.5mA, 1 = 5mA, 2 = 10mA, 3 = 25mA, 4 = 35mA, 5 = 45mA, 6 = 80mA, 7 = 200mA

→ 80mA @VDU = 3.6 V (Maximum) on this card

• C_SIZE_MULT

This parameter is used to compute the user's data card capacity not include the security protected are refer to C_SIZE.

Table 12-11: Multiply Factor for the Device Size

C_SIZE_MULT	MULT
0	$2^2 = 4$
1	$2^3 = 8$
2	$2^4 = 16$
3	$2^5 = 32$
4	$2^6 = 64$
5	$2^7 = 128$
6	$2^8 = 256$
7	$2^9 = 512$

→ 1GB : $2^9 = 512$

• ERASE_BLK_EN

Caution!: This is different from MMC. Please be careful.)
WRITE_BL_LEN defines whether erase of one write block(see WRITE_BL_LEN) is allowed.

Table12-12: ERASE_BLK_EN

ERASE_BLK_EN	Description
0	Host cannot erase by WRITE_BL_LEN
1	Host can erase by WRITE_BL_LEN

→ "1" : Can erase by WRITE_BL_LEN unit
So should be check this value, and recognize how to erase.

• R SECTOR_SIZE

Sector defines the minimum erasable size. SECTOR_SIZE indicates the minimum erasable size as the number of write blocks.

→ 1 Sector-size = 128 Write Blocks on this card

• WP_GRP_SIZE

WP_GRP_SIZE defines the minimum number of sectors that can be set for the write protect group (WP_Group).
A value of '0' means 1WP-Group = 1 erase sector,'127 means1WP-Group = 128 sectors.

→ "1": 1WP-Group is one sector on this card

• WP_GRP_ENABLE

A value of "0" means not implemented (supported) the WP-Group functions.

Table12-13: WP_GRP_ENABLE

WP_GRP_ENABLE	Description
0	NOT Implemented
1	Implemented

→ "0": WP Group is not Implemented on this card

• R2W_FACTOR

That is calculated R2W_FACTOR defines a multiple number for typical write time as a multiple of the read access time.

Table12-14: R2W_FACTOR

R2W_FACTOR	Multiples of read Access Time
0	1
1	2(Write half as fast as read)
2	4
3	8
4	16
5	32
6,7	Reserved

→ "5": Typical write time = Read Access timex32 on this card

• WRITE_BL_LEN

The maximum write block length is calculated as $2^{WRITE\_BL\_LEN}$.

Table12-15: DATA Block Length

WRITE_BL_LEN	Block Length
0-8	Reserved
9	2^9 = 512Bytes
・・・	
11	2^{11} = 2048Bytes
12-15	Reserved

→ 1GB=”9”: 512Bytes

• WRITE_BL_PARTIAL

WRITE_BL_LEN defines whether partial block write is available.

Table12-16: Write Data size

WRITE_BL_PARTIAL	Block Oriented write Data size
0	Only the WRITE_BL_LEN size or 512Bytes are available
1	Partial size (Minimum 1Byte) write available

→ ”0”: Partial size write is not available on this card

• FILE_FORMAT_GRP/FILE_FORMAT

Indicates the selected group of file format group and file format.

Table12-17: File Format

FILE_FORMAT_GRP	FILE_FORMAT	Kinds
0	0	Hard disk-like File system with partition table
0	1	DOS FAT(floppy-like) with boot sector only (No partition table)
0	2	Universal File Format
0	3	Others/Unknown
1	0,1,2,3	Reserved

Further information is given in SD Memory Card FILE SYSTEM SPECIFICATION.

→ [0.0]: Hard disk-like file system with partition table on this card

• COPY

Defines the contents of this card is original (=0) or duplicated (1).
This bit is one time programmable.

Table12-18: COPY

COPY	Description
0	Original
1	Copy

→ ”0”: Original on this card

• PERM_WRITE_PROTECT

Permanently protects the whole card content against write or erase.
This bit is one time programmable.

Table12-19: PERM_WRITE_PROTECT

PERM_WRITE_PROTECT	Description
0	Not protected/Writable
1	Permanently Write protected

→ ”0”: Not Protected/Writable on this card

• TMP_WRITE_PROTECT

Temporarily protects the whole card content against write or erase.

Table12-20: TMP_WRITE_PROTECT

TMP_WRITE_PROTECT	Description
0	Not protected/Writable
1	Temporarily Write Erase protected

→ ”0”: Not Protected/Writable on this card

• CRC

Calculated CRC for default data is set here.
Host System is responsible to re-calculate this CRC if any CSD contents are changed.

5.2.4 RCA Register

The writable 16bit relative card address register carries the card address in SD Card mode.

5.2.5 DSR Register

This register is not implemented on this card.

5.2.6 SCR Register

SCR (SD Card Configuration Register) provides information on SD Memory Card's special features.
The size of SCR Register is 64 bit.

Table13: SCR Register

Field	Width	Cell Type	SCR Slice	Value
SCR_STRUCTURE	4	R	[63:60]	0000
SD_SPEC	4	R	[59:56]	0000
DATA_STAT_AFTER_ERASE	1	R	[55:55]	1
SD_SECURITY	3	R	[54:52]	010
SD_BUS_WIDTHS	4	R	[51:48]	0101
-	16	R	[47:32]	All '0'
-	32	R	[31:0]	Reserved for manufacturer usage

• SCR_STRUCTURE

Version number of the related structure in the SD Card PHYSICAL LAYER SPECIFICATION.

Table13-1: SCR_STRUCTURE

SCR_STRUCTURE	SCR STRUCTURE VERSION	Valid for SD PHYSICAL LAYER SPECIFICATION
0	SCR Version 1.0	Version 1.0
1-15	Reserved	

→ "0": Version 1.0 Compliant on this card

• SD_SPEC

Describes the SD PHYSICAL LAYER SPECIFICATION version supported by this card.

Table13-2: SD_SPEC

SD_SPEC	SD PHYSICAL LAYER SPECIFICATION Version
0	Version 1.0
1-15	Reserved

→ "0" = Version1.0 Compliant on this card

• DATA_STAT_AFTER_ERASE

This indicates the block “0” or “1” after erase operation.

→ ”1” on this card

• SD_SECURITY

Describe the security algorithm supported by the Card.

Table13-3: Supported Security Algorithm

SD_SECURITY	Supported algorithm
0	No Security
1	Security Protocol 1.0
2	Security Protocol 2.0
3-7	Reserved

Security protocol 1.0: n Bus encryption

→ ”2”: Security Protocol 2.0 on this card

• SD_BUS_WIDTHS

Indicates the DAT bus width that a supported by this card.

Table 13-4:Supported Bus Widths

SD_BUS_WIDTHS	Supported BUS width
0 bit position	1 bit(DAT0)
1st bit position	Reserved
2nd bit position	4 bit(DAT0-3)
3rd bit position	Reserved

→ ” 0101”: 1 and 4 bit supported.

5.2.7 SD Status

Table14: SD Status

Identifier	Width	Type	SD Status Slice	Value
DAT_BUS_WIDTH	2	SR	[511:510]	00
SECURED_MODE	1	SR	[509]	0
-	13	-	[508:496]	All '0'
SD_CARD_TYPE	16	SR	[495:480]	0x0000
SIZE_OF_PROTECTED_AREA	32	SR	[479:448]	0x28
-	136	-	[447:312]	All '0'
-	312	-	[311:0]	All '0'

S: Status bit
R: Set based on Command Response

• DAT_BUS_WIDTH

Indicate the currently defined data bus width that was defined by SET_BUS_WIDTH command.

Table14-1:DAT_BUS_WIDTH

DAT_BUS_WIDTH	Bus Width
'00'	1 bit(default)
'01'	Reserved
'10'	4 bit width
'11'	Reserved

• SECURED_MODE

Indicates whether card is in secure mode operation.

Table14-2:SECURED_MODE

SECURED_MODE	Secured Mode Status
'0'	NOT Secured Mode
'1'	Secured Mode

• SD_CARD_TYPE

SD Card type described here. (Various SD types to be defined in the future.)

Table14-3:SD_CARD_TYPE

SD_CARD_TYPE	SD Card Type
'0000'h	SD Memory Card

• SD_CARD_TYPE

Show the size of protected area.
The actual area = (SIZE_OF_PROTECTED_AREA) x MULT x BLOCK_LEN

→ Protected Area depends on the Memory Types as below.
1GB: 10240KB

5.3 Logical Format

The device is formatted before shipping compliant to the SD Card FILE SYSTEM SPECIFICATION.
Following parameters may be changed if the host system is not compliant with the SD Card Format Specification.
The logical format parameters are described in the Table 15, 16, 17, 18.
The data of the logical format is described in Appendix 3.

5.3.1 SD card Capacities

This register is not implemented on this card.

Table 15: SD Card capacities

Item	Card Capacities	
	Sector	KB
Whole Capacity	2,032,640	1,016,320
User Data Area Size	2,012,160	1,006,080
Protected Area Size	20,480	10,240

5.3.2 SD card System information

Table.16: SD card System information

Item		Card Capacities
User Data Area	Data Boundary unit size (KB)	64
	Cluster Size(KB)	16
Protected Area	Data Boundary unit size (KB)	16
	Cluster Size(KB)	16

5.3.3 MBR, Boot Sector parameters

Table. 17: Master Boot Record a Partition Table

BP	Data Length	Field Name	Contents
0	446	Master Boot Record	All 0x00
446	16	Partition Table(partition1)	Refer Table 18
462	16	Partition Table(partition2)	All 0x00
478	16	Partition Table(partition3)	All 0x00
494	16	Partition Table(partition4)	All 0x00
510	2	Signature Word	0x55(BP510),0xAA(BP511)

Table 18: Partition Table

BP	Data Length	Field Name	Contents
0	1	Boot Indicator	0x00
1	1	Starting Head	3
2	2	Starting Sector/Starting Cylinder	55/0
4	1	System ID	0x06
5	1	Ending Head	3
6	2	Ending Sector/Ending Cylinder	32/998
8	4	Relative Sector	243
12	4	Total Sector	2,011,917

Table.19: Extended FDC Descriptor

BP	Data Length	Field Name	Contents
0	3	Jump Command	0xEB(BP0),0x00(BP1),0x90(BP2)
3	8	Creating System Identifier	(Card Specific 8Byte-Data)
11	2	Sector Size	512
13	1	Sectors per Cluster	64
14	2	Reserved Sector Count	1
16	1	Number of FATs	2
17	2	Number of Root-directory Entries	512
19	2	Total Sectors	0
21	1	Medium Identifier	0xF8
22	2	Sectors per FAT	246
24	2	Sectors per Track	63
26	2	Number of Sides	32
28	4	Number of Hidden Sectors	243
32	4	Total Sectors	2,011,917
36	1	Physical Disk Number	0x80
37	1	Reserved	0x00
38	1	Extended Boot Record Signature	0x29
39	4	Volume ID Number	(Card Specific 4Byte Data)
43	11	Volume Label	“NO NAME “
54	8	File System Type	“FAT16 “
62	448	(Reserved for system use)	All 0x00
510	2	Signature Word	0x55(BP510), 0xAA(BP511)

5.3.4 FAT

FAT1 and FAT2 are consisted with the same data.
1GB: FAT16 .

Table.20: FAT

BP	FAT16
0	0xF8
1	0xFF
2	0xFF
3	0xFF
4	0x00
5	0x00
….	0x00
End	0x00

5.3.5 Root Directory Entries

Initial values are All “0x00”.

5.3.5 User Data Area

Initial values are All “0xFF”.

6. Others: Limited Conditions, SD Specification Compliance

• 1) Non Supported Registers:

DSR Register (Optional register: PHISYCAL LAYER SPECIFICATION 5.6)

• 2) Non Supported Functions:

Programmable Card Output Driver (Optional in PHYSICAL LAYER SPECIFICATION 6.5)
Card ‘s Internal Write Protect (Optional in PHYSICAL LAYER SPECIFICATION 4.3.5.)

• 3) Non Specified Command:

CMD4 SET_DSR
CMD56 GEN_CMD

7. Host System Design Guidelines

The purpose of this guideline is a reference to help the design of the device interface of the Host system.
The description here does not make any warranty fitness for particular host.
The implementations of the host systems are different in each system.
Please design the SD Memory Card Host systems considering the each condition.

Mandate: Mandate requirement to the Host implementation
Recommendation: Recommended Implementation, Just General Example

7.1 Error handling (Recommendation)

This section shows a reference of host's error handling for errors generated in accessing the SD card.

7.1.1 Basic processing for error handling

7.1.1.1 Definition of error handling

(1) Retry process
Retry process refers to re-issuing a command. For example if SD card fails to receive a command due to noise, the command is issued again.

(2) Recovery process
Recovery process refers to the process taken by the host when SD card normally receives a command and, during the processing the command, it detects a General Error.

(3) Host's exception handling
The exception handling refers to the process taken by the host when the SD memory card normally receives a command, and during the command processing, it detects an error other than ERROR which is defined in SD card specification. This problem can be resolved by neither retry process nor recovery process.

7.1.1.2 Common error handling

7.1.1.2.1 Error against command response

(1) Time-out
Run the retry process. To avoid the infinite loop, implement a retry counter in the host so that, if the retry counter expires, the exception handling starts in the host.

(2) ERROR
Following the procedure per command, run the recovery process.

(3) Other errors
If the unit and size of address fail to conform to the SD memory card specification, no such errors can be resolved with command retry, requiring the exception handling by the host.

7.1.1.2.2 Process by data response

(1) Time-out
For the multiple command, send a CMD12. Response to CMD12 shall follow the procedures defined in 7.1.1.2.1.

(2) Error detection
Follow the same procedure as in (1) Time-out.

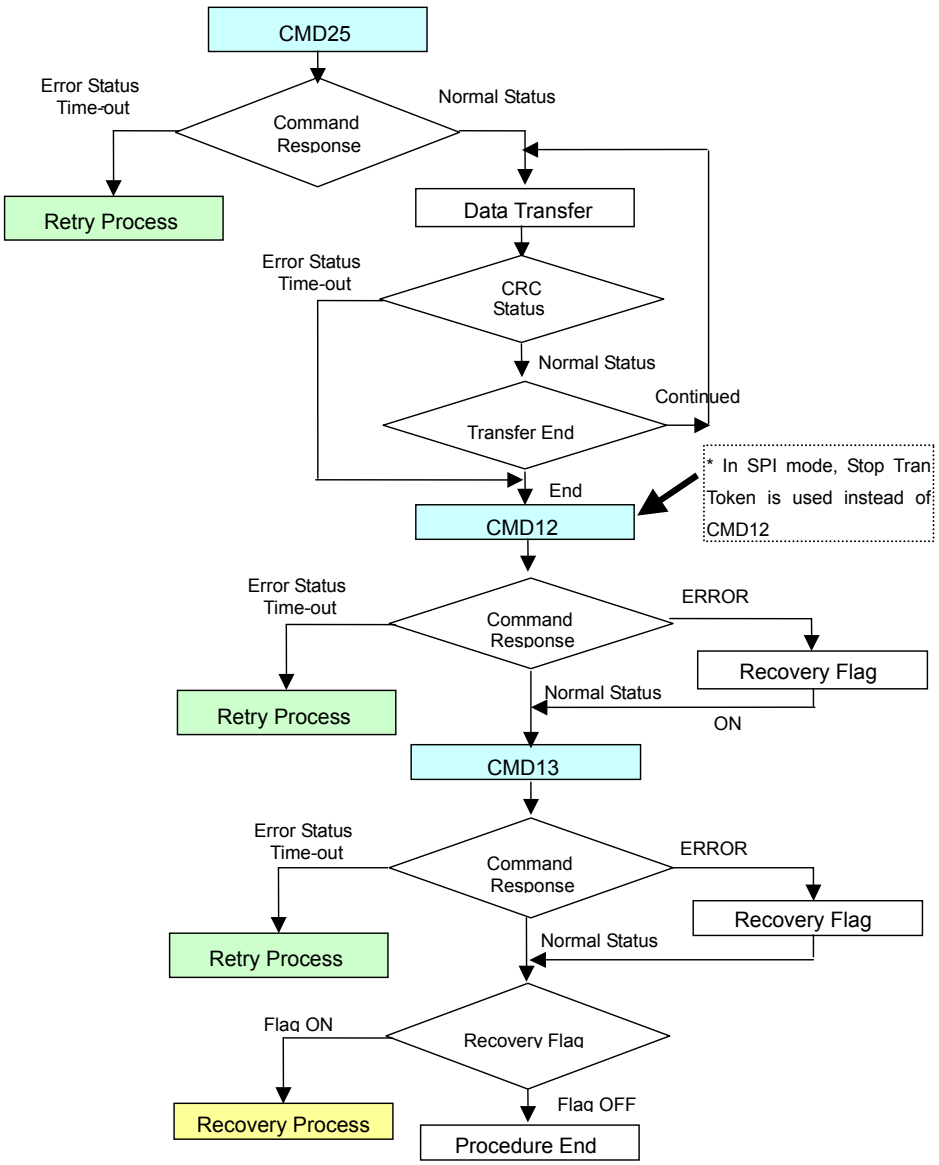
7.1.1.2.3 Clearing the error bit due to CMD13

Error handling shall be completed with checking SD_STATUS of CMD13 and read clear. Procedure from error detection to CMD13 shall be closed within one error handling so that no errors remain in a response to the next command. For issues to be noted after the time-out processing, refer to 7.2.

7.1.1.3 Error handling in SD mode

7.1.1.3.1 Error handling for WRITE_MULTIPLE_BLOCK (CMD25)

This product uses the NAND type flash memory. If the NAND type memory fails to write on a page, due to the configuration scheme, such failure may affect the data in other pages within the same delete block.
(Delete block refers to the minimum unit allowed to be deleted. It consists of multiple pages)
Thus, if CMD25 (WRITE_MULTIPLE_BLOCK) causes an error in writing multiple blocks, check the number of blocks successfully written by issuing ACMD22.
If the number of blocks successfully written differs from the expected value, some blocks may contain data not normally written. Thus, write it again. Standard flow (Figure 9), retry process flow (Figure 10), recovery process flow (Figure 11), and host's exception handling flow (Figure 12) including the error recovery for CMD25 are shown below.



(1) Writing data across the OUT_OF_RANGE boundary may expire the data CRC response timer.
(2) For an error taking place in writing, judge the condition if the recovery operation is required or not.
(3) Take the recovery action after using ACMD22 to count the blocks that was written.
(4) To the repetition process of retry and recovery operations, insert a condition for breaking the infinite loop.

Figure 9 Standard flow including the CMD25 error recovery process

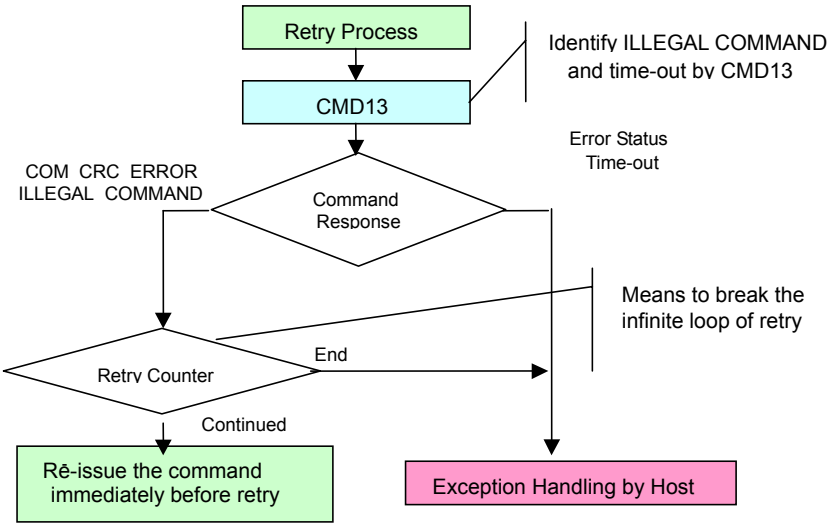


Figure 10 Retry process flow

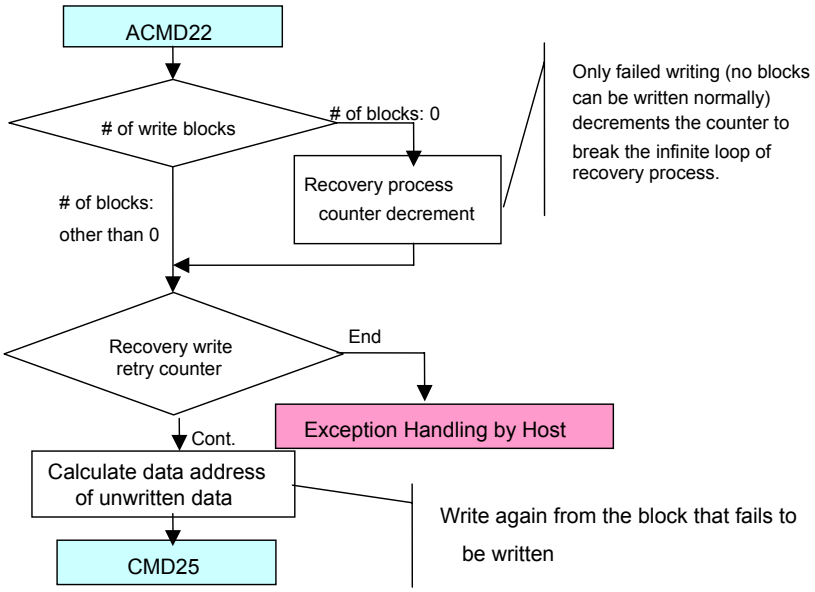


Figure 11 Recovery write flow

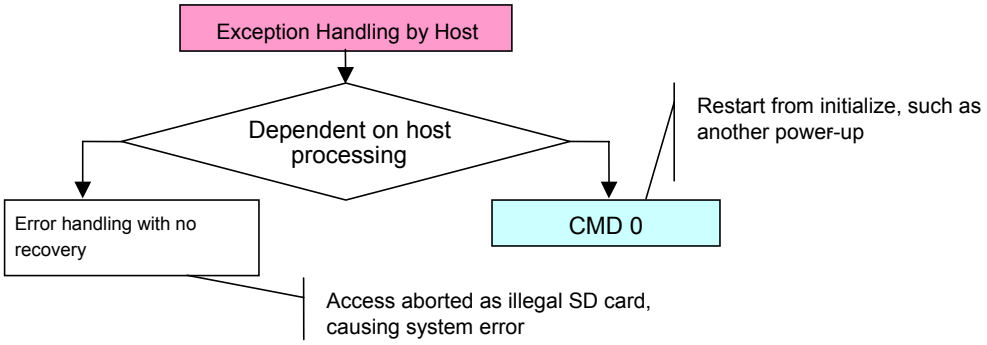


Figure 12 Flow of exception handling by host

7.1.1.3.2 Error handling for READ _MULTIPLE_BLOCK CMD18

Notes on CMD18 operations are listed below.

(1) Attempting to read the final block may cause OUT_OF_RANGE. In such case, ignore the OUT_OF_RANGE.
(2) If CARD_ECC_FAILED occurs, retry reading.
(3) Retry process shall follow Figure 13.
(4) Read recovery process shall follow Figure 14.

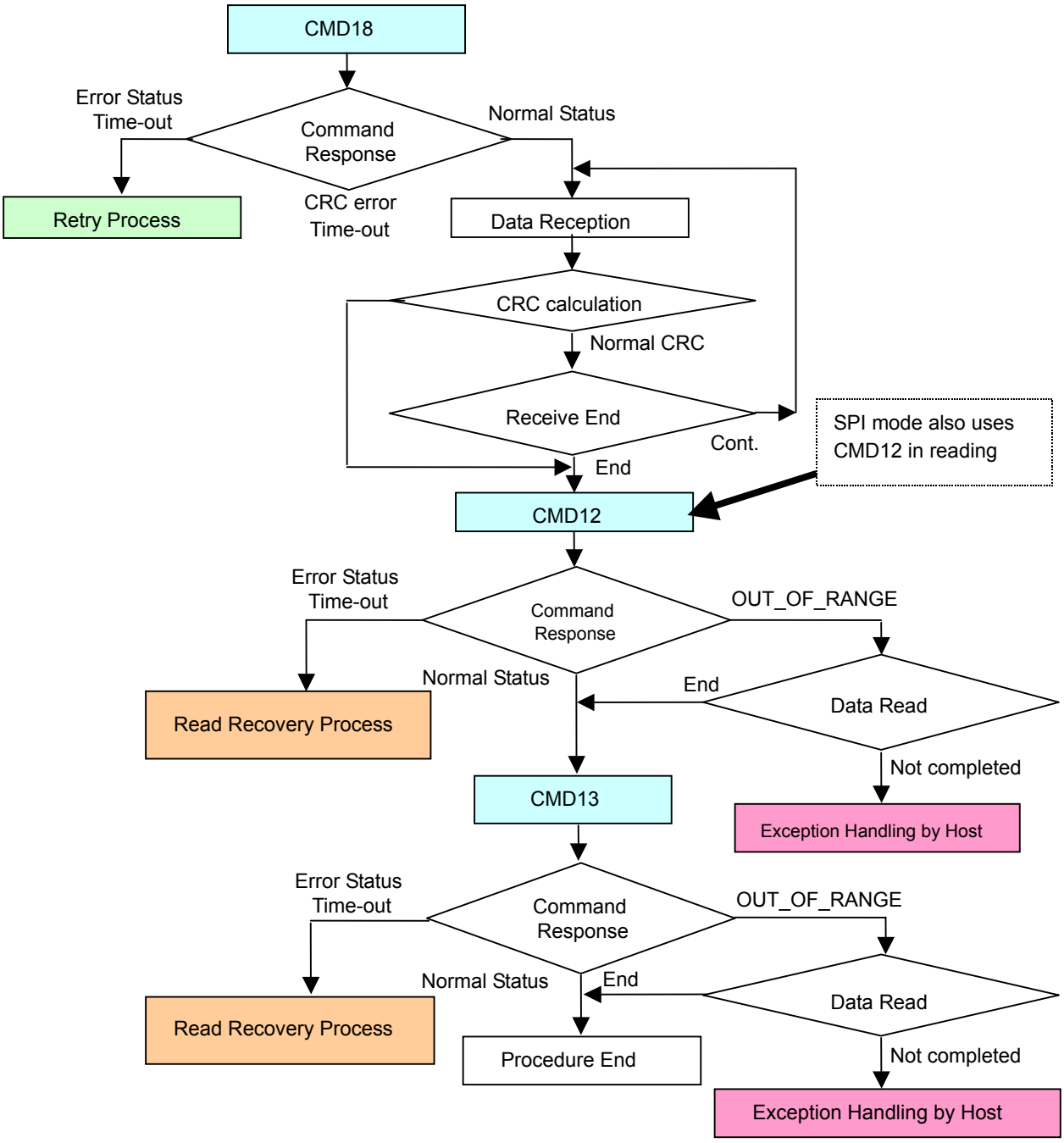


Figure 13 Standard flow including CMD18 error recovery process

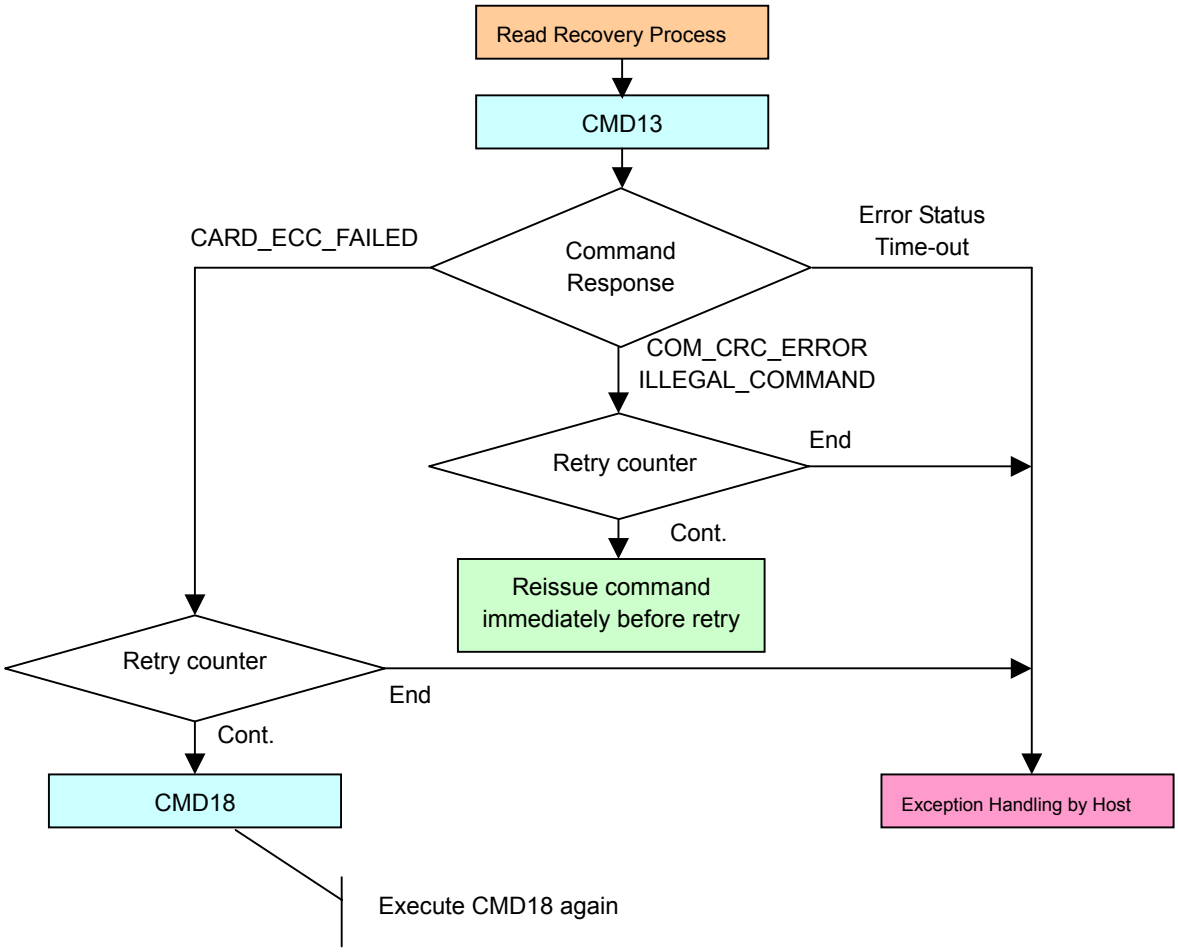


Figure 14 Read retry process flow of CMD18

7.2 Process after Timeout in case if Read or Write (Recommendation)

If there are no-response after the timeout passed in case of read or write (Recommendation), please issue the CMD12(Stop Transmission) and stop the data transfer to prevent the host stuck on waiting for the response.
(Reference :5.3.3. Data Token, 5.3.4.Data Error Token of SD PHYSICAL LAYER SPECIFICATION.)

In case of SPI mode, there are some restrictions regarding to access the out of range boundary.

1) Response error (*1) will be occurred when host issue CMD12 over the out of range boundary under WRITE_MULTIPLE (CMD25, ACMD25) action.
2) This maybe occurred when SD CLK is low frequency. In case of out of range token maybe duplicated, please check case (a) and case (b) when issue CMD12 after reading before the boundary using READ_MULTIPLE (CMD18, ACMD18).

   (a) Response error maybe occurred (*1)
   (b) Response of CMD12 maybe not issued.
   - Re-issue CMD12, then next command can be received
   - Neglect the response of re-issue CMD12

   *1: Response Error Descriptions
   - If CRC Check is On.
     Com CRC Error is responded.
   - If CRC Check is Off.
     In case of 1) above, R1=0x44(Parameter Error & Illegal Command)
     In case of 2) above, R1=0x44(Illegal Command)

7.3 Host Time Setup (Recommendation)

The timeout value is recommended as below. (Table 21)
The memory Erase function requires the longest time before the Card Response. The erase time for Memory Block is also included for the Timeout value in the Data erase operation in the SD Memory Card. (Table 22)
The Host system should chose the appropriate block size considering the erase time.

Table21: Recommended Time out value

Condition	Recommended Value (Max.)
Waiting for the CMD Response	64cycles
Read Data output after issue the Commands	100ms
Busy Status Change	1s

Table22: Erase time reference value

1GB	The Host system should chose the appropriate block size considering the erase time.

7.4 Efficient Data Writing to SD Memory Card (Recommendation)

To control the SD memory card with a higher speed and lower power consumption, it is recommended that Multiple Block Write should be used as a command for writing data and the size of data written by each command should be the FAT cluster size × n (n: integer).

7.4.1 WRITE_SINGLE_BLOCK and WRITE_MULTIPLE_BLOCK

WRITE_SINGLE_BLOCK (CMD24) is a command used to write data of 512Bytes, which is suitable for writing comparatively small capacity of data (512byte:SingleBlock) such as updating mainly a part of File System (e.g. FAT). *1

On the other hand, WRITE_MULTIPLE_BLOCK (CMD25) is a command for writing data to blocks that have consecutive addresses per command, which is suitable to write a large capacity of data (e.g. data section in a file). Using WRITE_MULTIPLE_BLOCK to write data with a cluster unit (512Byte×128Block=64KByte) in the file system (Figure 15) is an efficient access to the flash memory, providing a higher-speed writing compared to writing the same capacity of data with Single_Block_Write (*2). In addition, this command decreases internal processes in the SD memory card, reducing the power consumption for writing a block. By avoiding the issuing command per 512 bytes as in WRITE_SINGLE_BLOCK, software processes in the host device become faster. For this operation, check that the sectors in the SD memory card and file system have compatibility as described in Figure 16.

For writing the File System (e.g. FAT Table), it is recommended to update data of minimum amount with collective units. Updating every time when the cluster chain changes frequently causes writings of small amount of data, degrading the write performance.

*1 : Writing a large amount of data per block with WRITE_SINGLE_BLOCK causes updating the card system so to reliably store the 512Byte data in the flash memory, as a result, lowering the write performance and increasing the power consumption

*2 : If consecutive multiple clusters are available, efficient writing is obtained by writing 32Block (16kB)×n (n = integer).

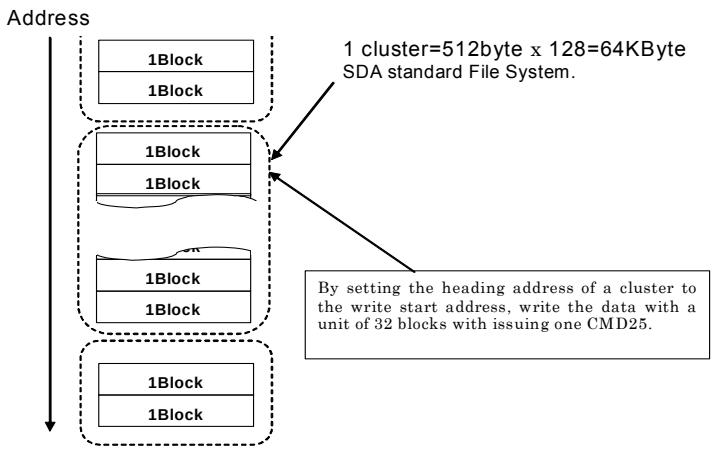


Figure 15 Writing multiple blocks with Multiple_Block_Write

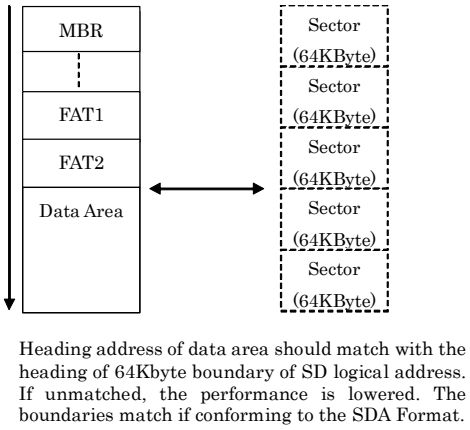


Figure 16 Matching between logical address and file system

7.4.2 Processing flow of WRITE_MULTIPLE_BLOCK

Figure 17 shows a flow chart of writing using WRITE_MULTIPLE_BLOCK command.
After issuing CMD25 and analyzing the response, write data of 512Bytes is output. Thereafter, while checking that CRC status sent from a card is normal, send the subsequent block. If the final block is sent, send Stop_Tran command (CMD12) to close the process.

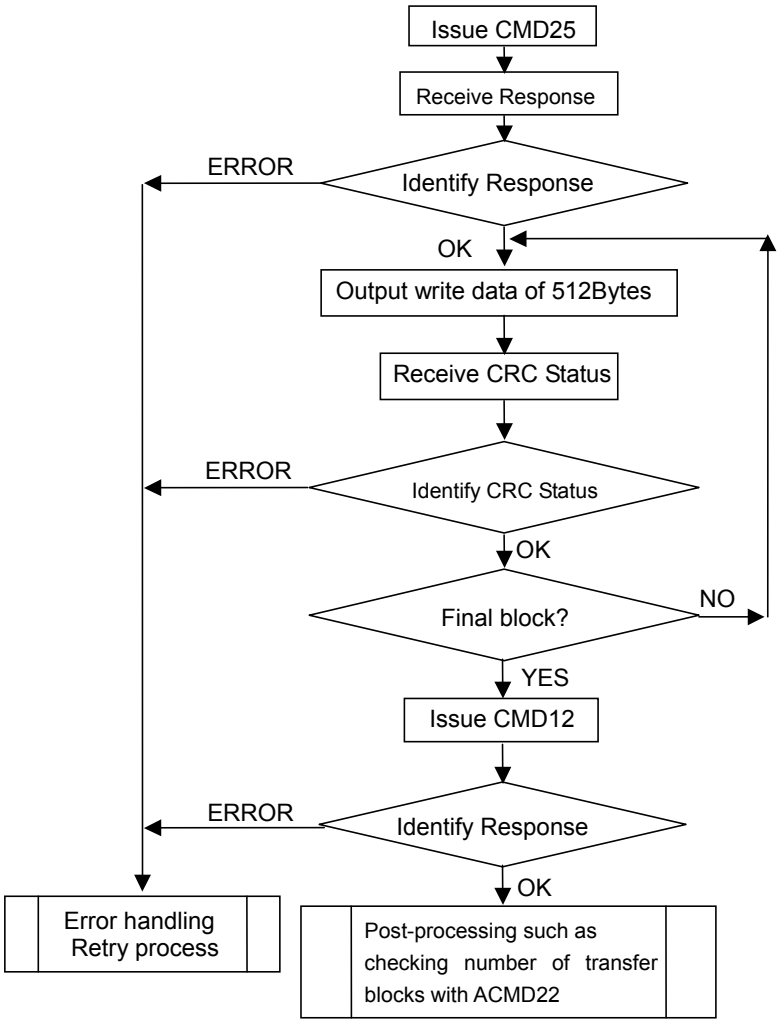


Figure 17 Write flow of WRITE_MULTIPLE_BLOCK processing

7.4.3 Power control (Recommended)

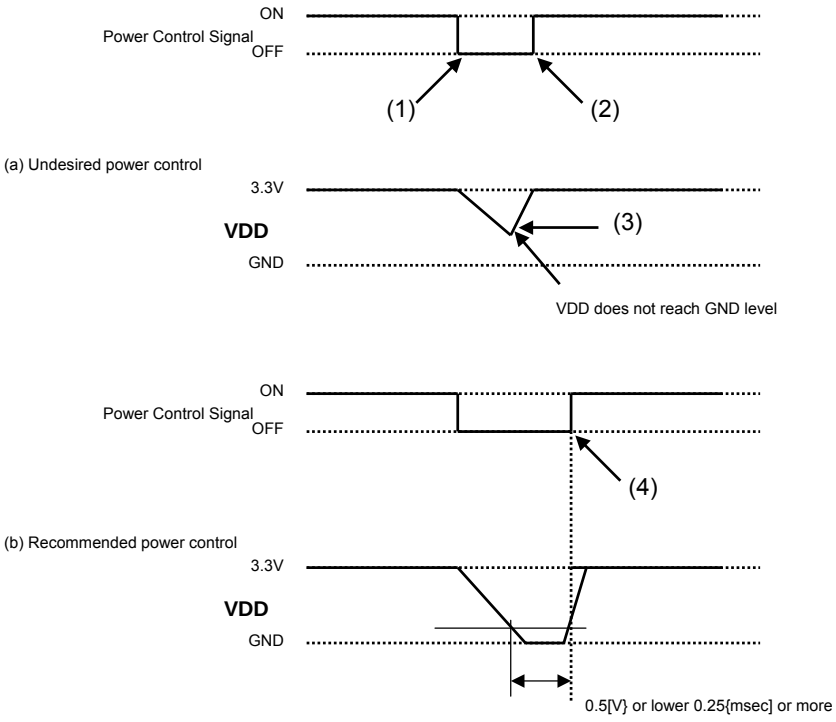
This device needs the initialization time of up to 1 second *4 for power-up. (It is similar to standard SD memory cards.) In other words, once the power is turned off, the initialization time is consumed before the next read/write processes, lowering the performance. Thus, it is recommended that normally, power is being turned on and the power is turned off after this device has no accesses for certain duration. If this device has no accesses, it enters the stand-by mode for saving the power consumption. (In stand-by mode, stand-by current is consumed.)

* 4: Specified in the SD Physical Specification.

• Reactivate the device

In reactivating this device (turn off and on mainly for reducing the power consumption) from the host device, check in advance that the power line reaches the GND level then turn it on. If the time from power-off to power-on is too short, resetting the card may not occur normally. On the specification, power off must keep the voltage of 0.5[V] or lower for 0.25[msec] at least.

The figure below illustrates undesired and recommended cases of power control. In developing the host devices, check the power control to prevent the undesired case.



Turn off at (1) in Undesired Case in Figure (a) and restart (turn on) when VDD does not reach GND level as shown in (2)(3) , and you may fail to reset normally.
Figure (b) shows the recommended power control. Turn on at the time of (4) when VDD reaches the GND level, and you can reset device surely with a higher reliability.

Figure 18 Power control

7.5 SPI-Mode initialization (Mandate)

The device shall be initialized by ACMD41. Do NOT use CMD1 for SPI-Mode initialization.

7.6 SPI-Mode RSV pin Pull up (Mandate)

RSV(#8,#9 in SPI Mode) shall be pulled up by 10-100k-ohm resistors.

7.7 Prohibition during Write (Mandate)

Do not turn off the power before read / write / mutual authentication operation is complete. Avoid using this device when the battery is low. Power shortage and/or power failure before read / write / mutual authentication operation is complete will cause malfunction of this device , loss of data and/or damage to data.
Please comment and inform this prohibition to the end users in proper way. (Manual or Instructions)

7.8 SD Command (Mandate)

1) CMD0 continuously issue
Do NOT continue the CMD0 with 1Pin(CD/DAT3)='Low' just after CMD0 or the SD Card initialized in SPI mode.
In case of 1 pin (CD/DAT3)="Low", it means SPI mode so be careful to the duration of CMD0 issue.
Please choose the appropriate timing interval for CMD0 to prevent this problem.
The interval is related with the pull up Resister value. of the host side.

2) After the Security Read Command
Please issue the CMD13 to ensure the status change to the transmission state(for SD mode) or wait SDCLK x n clock(n=8400 for SD 1bit mode or SPI mode, n=2100 for SD 4bit mode), after issue the ACMD18 or ACMD43.

3) CMD12(SD mode) or 'Stop Tran Token'(SPI mode) after Multiple Block Write Command
When the CMD12(STOP_TRANSMISSION, SD mode) or 'Stop Tran Token' (SPI mode) is issued after Multiple Block Write Command (CMD25, ACMD25), please issue the CMD12 or 'Stop Tran Token' immediately(*) after the last data block, to complete the data write transaction soon.
(*)It should be within 400μsec after the end of BUSY status for the last data block.

4) Time Interval between successive SD commands
Time interval between the BUSY end of the SD command and the start bit of the next SD command should be more than 15usec. If the time interval is less than 15μsec, SD bus error or device operation error may occur occasionally.

7.9 Pull Up resistors (Recommendation)

CMD and DAT [3:0] can pull up with 10-100k ohm resistors by the host side..
Pleased disable the Card-Internal pull up on CD by ACMD42 before access. (Refer Fig. 7)

7.10 Write/Erase Size management (Recommendation)

1) Erase Unit
The erase size is recommended to using Boundary unit indicated by Erase Sector size below.
The erase unit size is given as below.
Erase Sector Size = Block_length x (SECTOR_SIZE) = 512 Byte x 32-block= 16K Byte
(Block_length can calculate from WRITE_BL_LEN)

Appendix 2-1: initial value of OCR Register

Field	C RSV		3.6 – 1.6					RSV
Bit Position	31-28	27-24	23-20	19-16	15-12	11-8	7-4	3-0
Binary	*000	0000	1111	1111	1000	0000	0000	0000
Hexadecimal	*	0	F	F	8	0	0	0

2.7V - 3.6V operation

*: depends on card status (Card power up Status Bit)

Appendix 2-2: initial value of CID Register

Field	MID		OID				PNM									
Bit Position	127-124	123-120	119-116	115-112	111-108	107-104	103-100	99-96	95-92	91-88	87-84	83-80	79-76	75-72	71-68	67-64
Binary	0000	0010	0101	0100	0100	1101	0101	0011	0100	0100	0011	0000	0011	0001	0100	0111
Hexadecimal	0	2	5	4	4	D	5	3	4	4	3	0	3	1	4	7

Field	PRV		PSN								RSV	MDT			CRC7	1
Bit Position	63-60	59-56	55-52	51-48	47-44	43-40	39-36	35-32	31-28	27-24	23-20	19-16	15-12	11-8	7-4	3-0
Binary	****	****	****	****	****	****	****	****	****	****	0000	****	****	****	####	###1
Hexadecimal	*	*	*	*	*	*	*	*	*	*	0	*	*	*	#	#

*: depends on SD card

#: depends on its value

PSN: Product Serial Number

MDT: Manufacturing date

CRC7: CRC7 checksum

Appendix 2-3: initial value of CSD Register

Field	CS RSV		TAAC		NSAC		TRAN SPEED		CCC			READ_	R W R D	RS C_SIZE		
Bit Position	127-124	123-120	119-116	115-112	111-108	107-104	103-100	99-96	95-92	91-88	87-84	83-80	79-76	75-72	71-68	67-64
Binary	0000	0000	0010	1101	0000	0000	0011	0010	0001	1011	0101	1001	1000	0011	1101	0110
Hexadecimal	0	0	2	D	0	0	3	2	1	B	5	9	8	3	D	6

Field	VDD_	VDD_	VDD_ VDD_	C_SIZ	E SECTOR_SIZ		WP_GRP_SIZ		W RS R2W_	WRITE_	W RSV		F C P T	FIL RS	CRC7	1
Bit Position	63-60	59-56	55-52	51-48	47-44	43-40	39-36	35-32	31-28	27-24	23-20	19-16	15-12	11-8	7-4	3-0
Binary	0111	1110	1111	1011	1111	1111	1000	0000	0001	0110	0100	0000	0000	0000	####	###1
Hexadecimal	7	E	F	B	F	F	8	0	1	6	4	0	0	0	#	#

#: depends on its value

Appendix 2-4: initial value of SCR Register

Field	SCR_S	SD_SPI	D SD_S	SD_BU	RSV				reserved for manufacturer usage							
Bit Position	63-60	59-56	55-52	51-48	47-44	43-40	39-36	35-32	31-28	27-24	23-20	19-16	15-12	11-8	7-4	3-0
Binary	0000	0001	1010	0101	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000
Hexadecimal	0	1	A	5	0	0	0	0	#	#	#	#	#	#	#	#

#: depends on its value

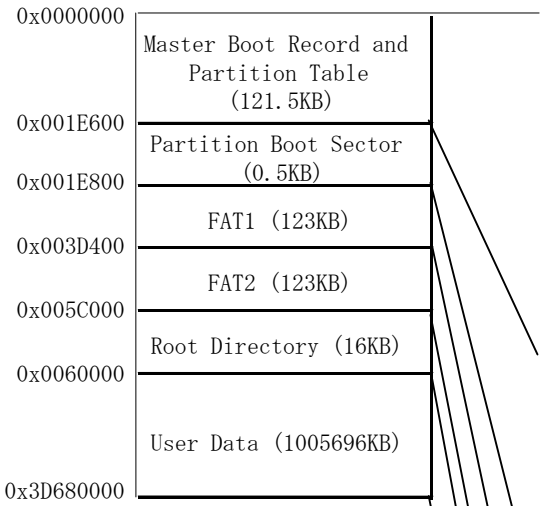
Appendix 2-5: initial value of SD Status

Field	DA S RSV				SD_CARD_TYPE				SIZE_OF_PROTECTED_AREA				
Bit Position	511-508	507-504	503-500	499-496	495-492	491-488	487-484	483-480	479-476	475-472	471-468	467-464	463-460
Binary	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000
Hexadecimal	0	0	0	0	0	0	0	0	0	0	0	0	0

Field				RSV				途中略					
Bit Position	459-456	455-452	451-448	447-444	443-440	439-436	435-434	[433:018]	17-16	15-12	11-8	7-4	3-0
Binary	0000	0010	1000	0000	0000	0000	00		00	0000	0000	0000	0000
Hexadecimal	0	2	8	0	0	0	0			0	0	0	0

Appendix 3 : Memory Map and Dump Data of User Data Area

Last address of this memory map indicates “actual last address + 1”.




```
ADDRESS    00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F
           (MBR and Partition Table)
0000000    00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
* (All 0x00)
00001b0    00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 03
00001c0    37 00 06 03 c3 e6 f3 00 00 00 0d b3 1e 00 00 00
00001d0    00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
* (All 0x00)
00001f0    00 00 00 00 00 00 00 00 00 00 00 00 00 00 55 aa
           (reserved)
0000200    ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
* (All 0xff)
           (Partition Boot Sector)
001e600    eb 00 90 xx xx xx xx xx xx xx xx 00 02 20 01 00
001e610    02 00 02 00 00 f8 f6 00 3f 00 20 00 f3 00 00 00
001e620    0d b3 1e 00 80 00 29 xx xx xx xx 4e 4f 20 4e 41
001e630    4d 45 20 20 20 20 46 41 54 31 36 20 20 20 00 00
001e640    00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
* (All 0x00)
001e7f0    00 00 00 00 00 00 00 00 00 00 00 00 00 00 55 aa
           (FAT1)
001e800    f8 ff ff ff 00 00 00 00 00 00 00 00 00 00 00 00
001e810    00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
* (All 0x00)
           (FAT2)
003d400    f8 ff ff ff 00 00 00 00 00 00 00 00 00 00 00 00
003d410    00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
* (All 0x00)
           (Root Directory)
005c000    00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
* (All 0x00)
           (User Data)
0060000    ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
* (All 0xff)
           (Last Sector)
```