


**Revision History**

**Model: SM 2258-G288\_2P5\_G152X16\_DB**

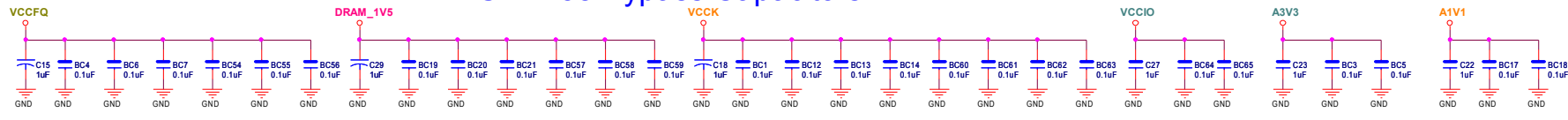
Revision	Date	Reason for redrawing	Page Update	Drawed	Checked	Approved
01A	0520Y16	Preliminary	--	Austin Lin		

Page1	Cover_Page
Page2	Controller_BGA288_2.5INCH
Page3	Power_Host_5V
Page4	NF_BGA152x8 (CH0, CH1)
Page5	NF_BGA152x8 (CH2, CH3)
Page6	DRAM_DDR3-16x2
Page7	Flash Mounting Guide

		<b>Silicon Motion, INC.</b>	
PageTitle	Cover Page		
DOC.Number	<Doc>		
Sch.FileName	SM2258G-AB-G288_2p5_G152X16_D2_DB_V01	Rev	01A
Date:	Tuesday, October 18, 2016	Sheet	1 of 7

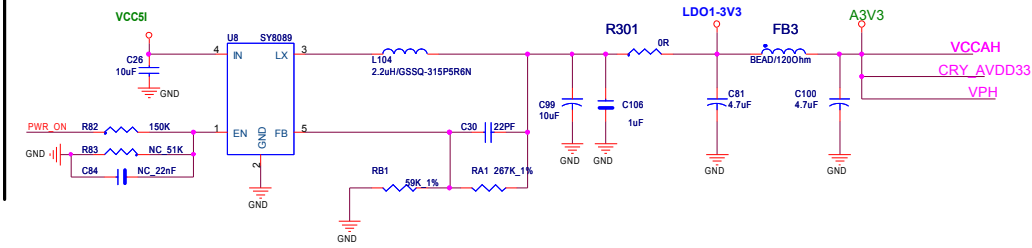
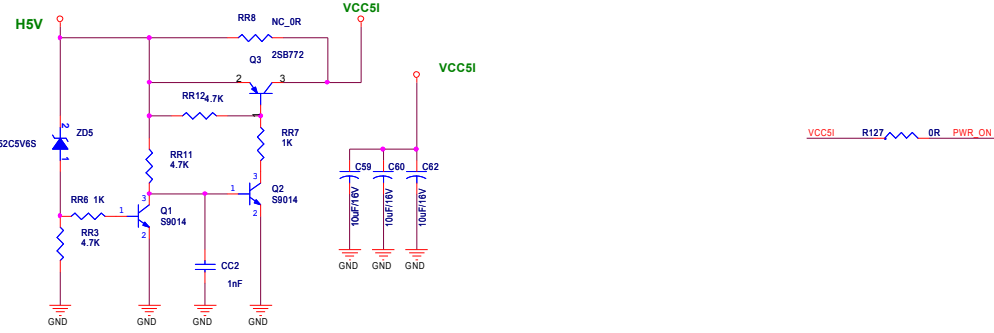


# SM2258 Bypass Capacitors



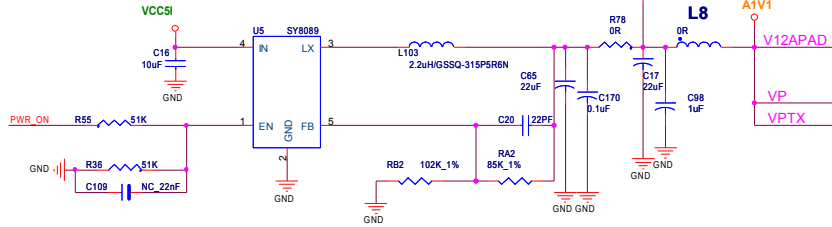
V18\_PAD = SM2246 Internal 1.8V LDO Vout  
 A3V3= 3.0 / 3.3 / 3.6 (V) For AIP power  
 A1V2=VDDTX\_PHY=VDDRX\_PHY= 1.14 / 1.2 / 1.26 (V) For AIP power  
 VCCK = 1.2 (V) For SM2246AA core power  
 VCC = 3.3 / 1.8 (V) For General IO power  
 VCCFQ = 3.3 (V) For NAND flash Core Power  
 VCCFQ = 3.3 / 1.8 (V) For NAND flash IO Power  
 DRAM\_1V5 = 1.5 / 1.8 (V) For DRAM Power

## OVP Circuit

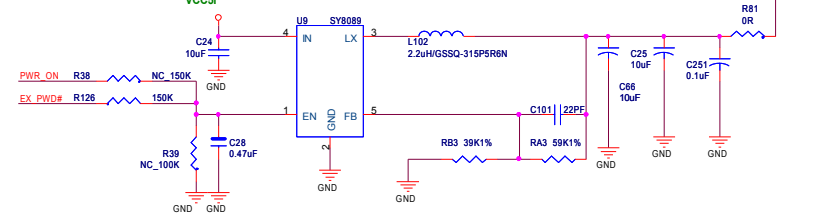


LDO\_1: VCCIO Power 3.3V

## POWER



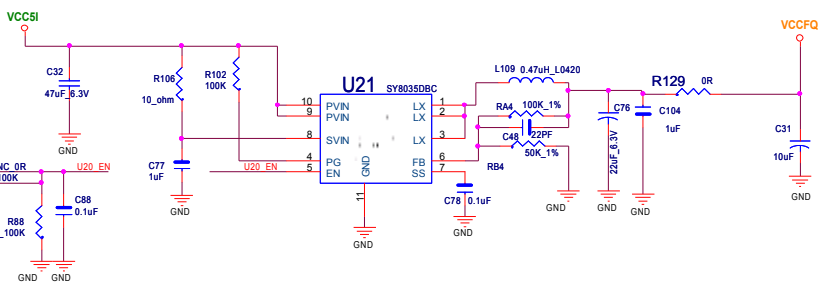
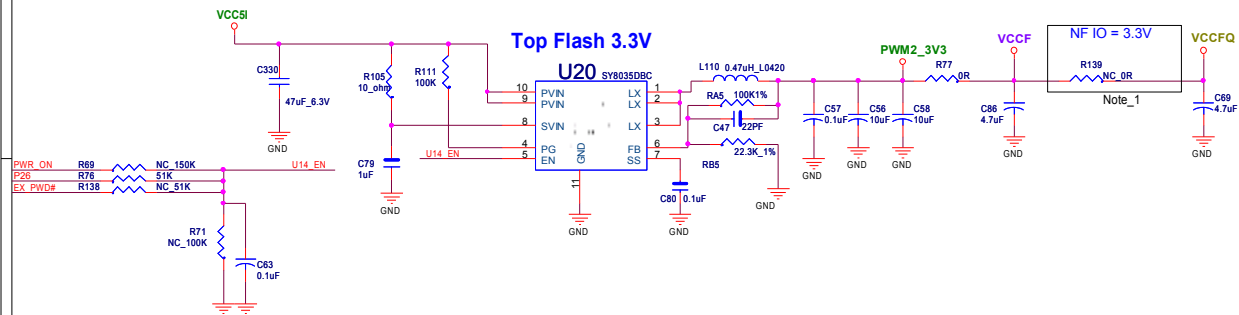
## POWER



$V_{out} = 0.6 \cdot (1 + RA/RB)$   
 $V_{out} = 1.35V, RB3=47K \text{ ohm},$   
 $V_{out} = 1.5V, RB3=39K \text{ ohm},$   
 $V_{out} = 1.8V, RB3=29.4K \text{ ohm},$   
 1%

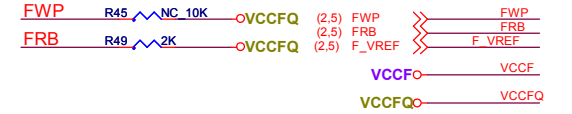
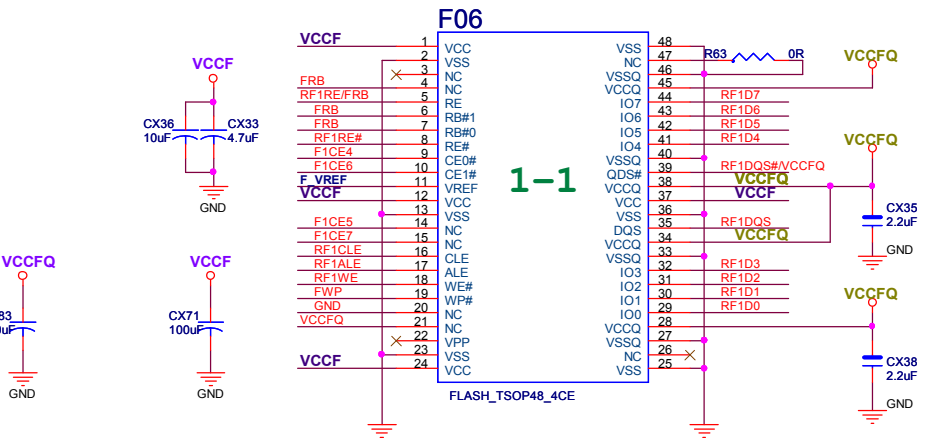
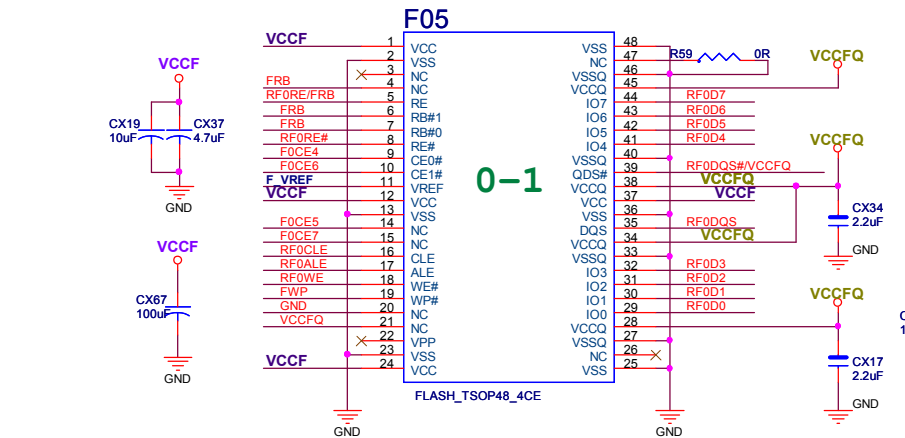
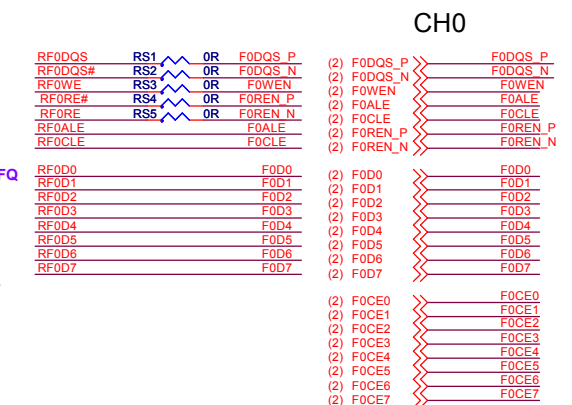
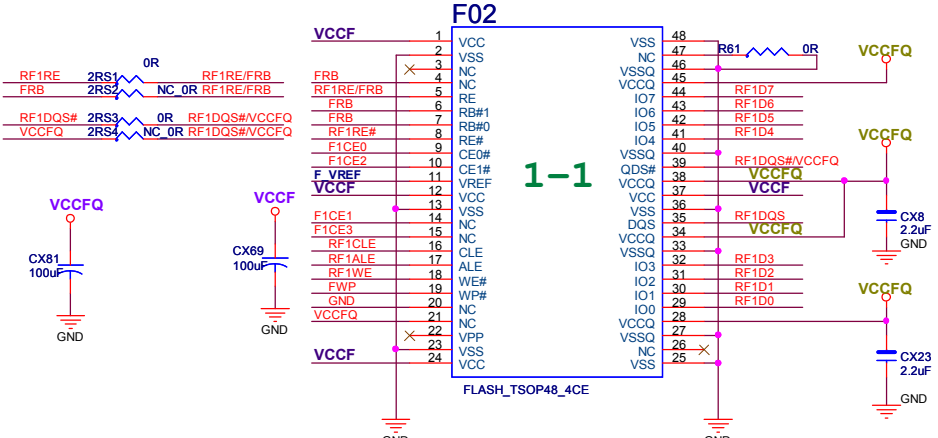
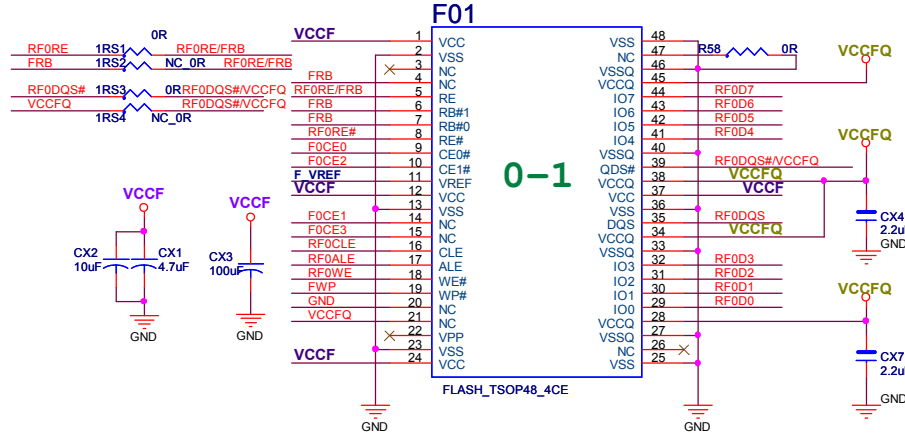
- (2) P26 >> P26
- (2) P27 >> P27
- (2) EX\_PWD# >> EX\_PWD#
- HSV ○ HSV
- VCCSI ○ VCCSI
- VCCFQ ○ VCCFQ
- VCCFQ ○ VCCFQ
- VCCIO ○ VCCIO
- A3V3 ○ VCCAH
- CRY\_AVDD33
- VCCCK ○ VCCCK
- A1V1 ○ V11APAD
- DRAM\_1V5 ○ DRAM\_1V5
- VCCFQ ○ VCCFQ
- VCCFQ ○ VCCFQ

## Top Flash 3.3V



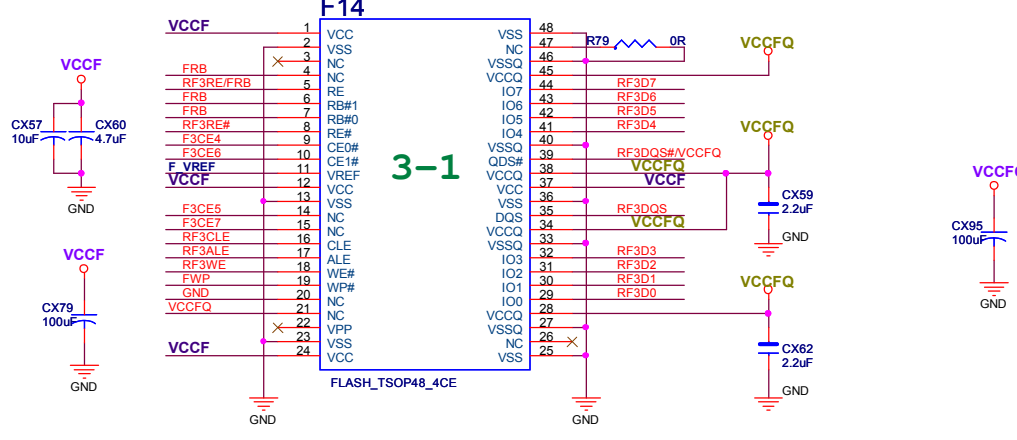
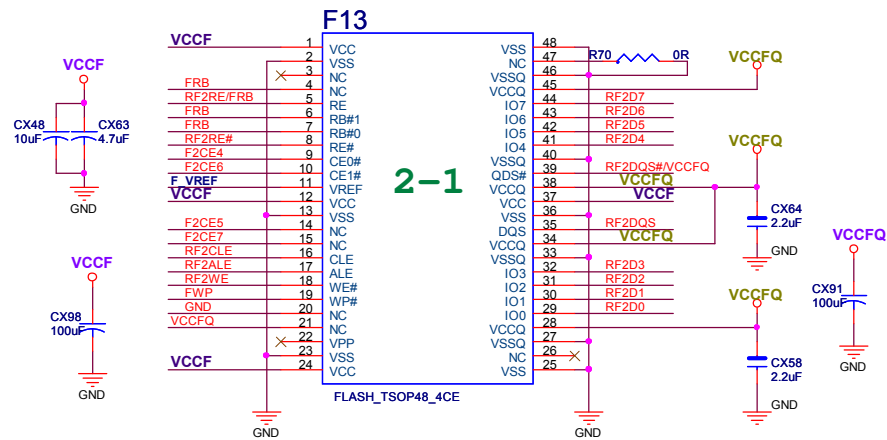
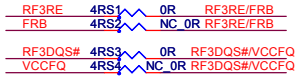
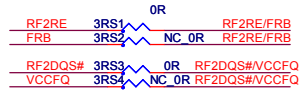
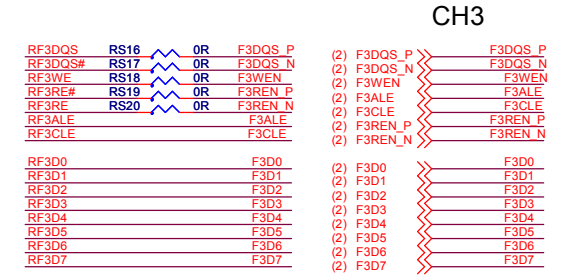
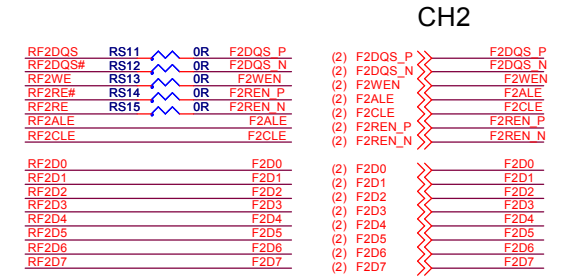
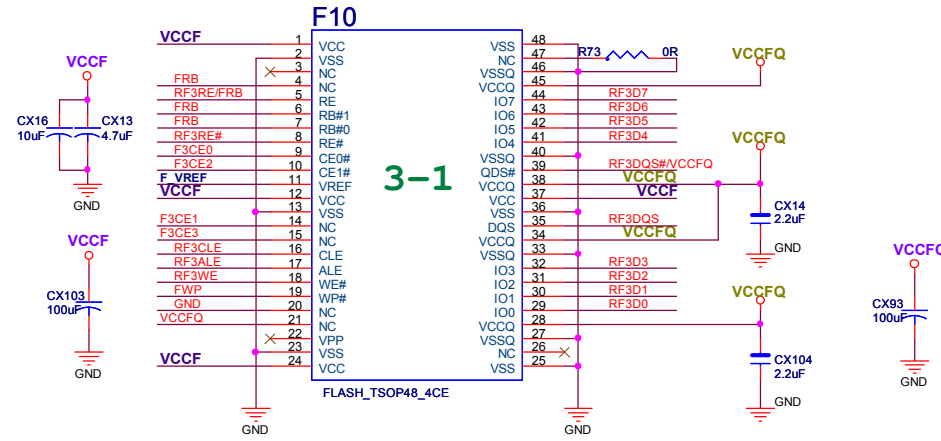
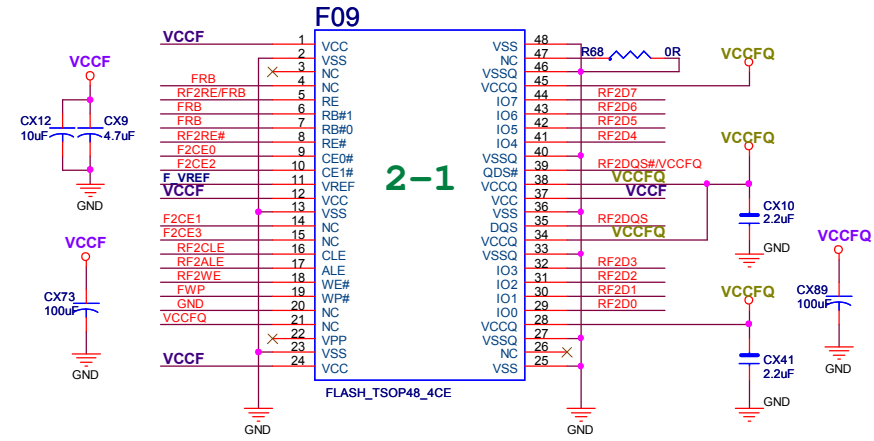
# Channel 0

# Channel 1

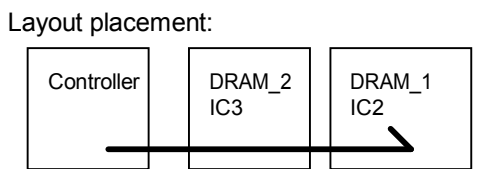
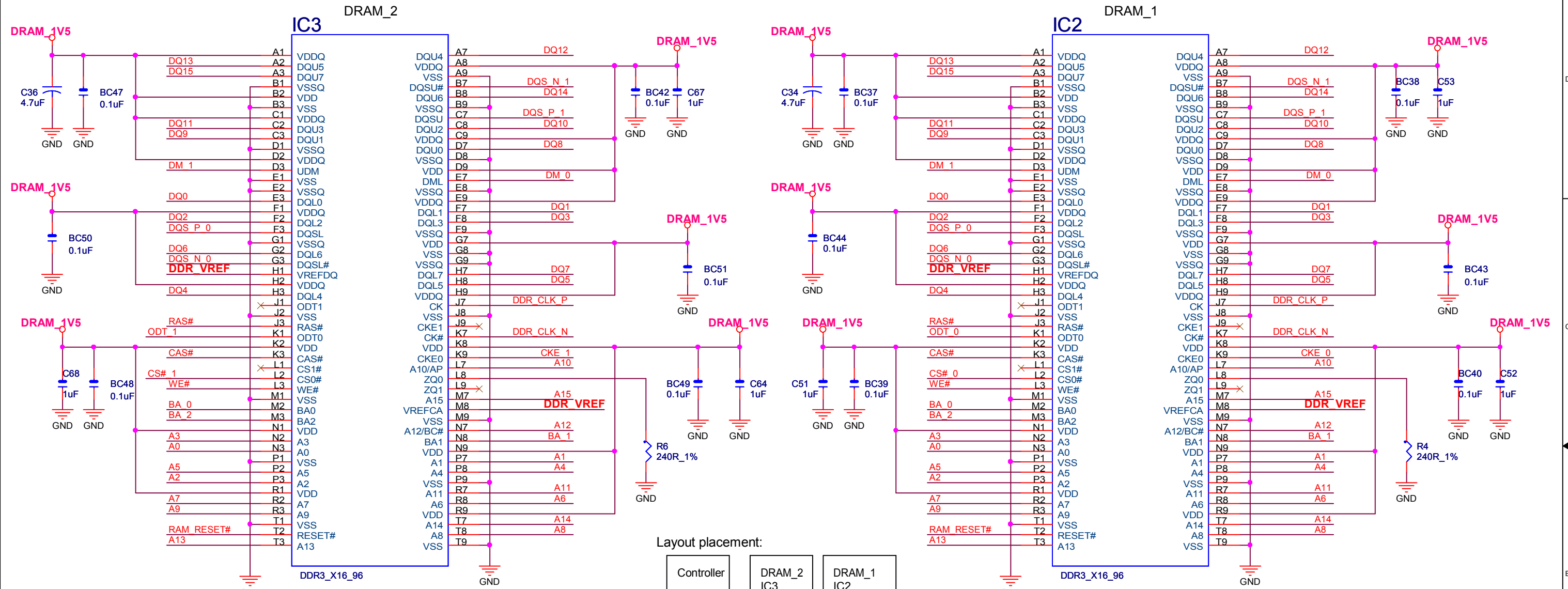


# Channel 2

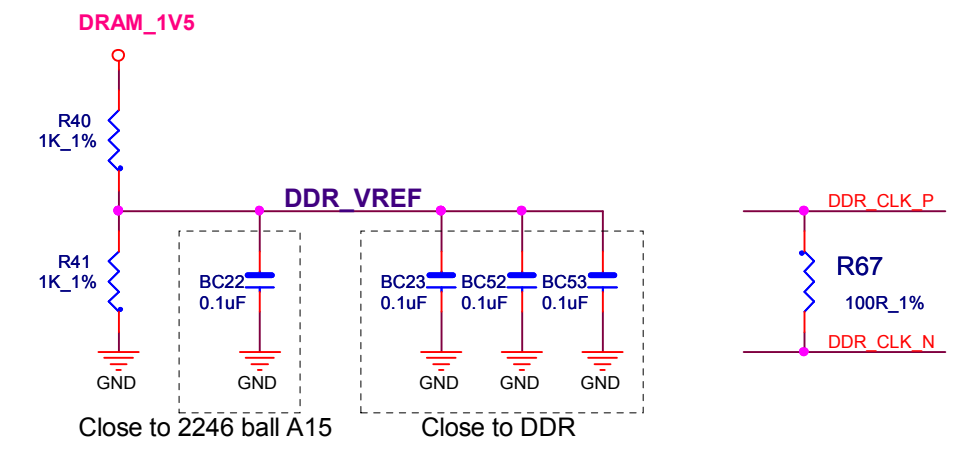
# Channel 3



# DRAM-DDR3



DRAM mounting order:  
 1. IC2  
 2. IC3



(2) BA_0	BA_0	(2) A0	A0	(2) DQ0	DQ0	(2) CKE_1	CKE_1	DRAM_1V5	DRAM_1V5
(2) BA_1	BA_1	(2) A1	A1	(2) DQ1	DQ1	(2) ODT_1	ODT_1	DDR_VREF	DDR_VREF
(2) BA_2	BA_2	(2) A2	A2	(2) DQ2	DQ2	(2) CS#_1	CS#_1		
(2) DDR_CLK_P	DDR_CLK_P	(2) A3	A3	(2) DQ3	DQ3				
(2) DDR_CLK_N	DDR_CLK_N	(2) A4	A4	(2) DQ4	DQ4				
(2) RAS#	RAS#	(2) A5	A5	(2) DQ5	DQ5				
(2) CAS#	CAS#	(2) A6	A6	(2) DQ6	DQ6				
(2) CS#_0	CS#_0	(2) A7	A7	(2) DQ7	DQ7				
(2) WE#	WE#	(2) A8	A8	(2) DQ8	DQ8				
(2) RAM_RESET#	RAM_RESET#	(2) A9	A9	(2) DQ9	DQ9				
(2) CKE_0	CKE_0	(2) A10	A10	(2) DQ10	DQ10				
(2) ODT_0	ODT_0	(2) A11	A11	(2) DQ11	DQ11				
(2) DM_0	DM_0	(2) A12	A12	(2) DQ12	DQ12				
(2) DM_1	DM_1	(2) A13	A13	(2) DQ13	DQ13				
(2) DQS_P_0	DQS_P_0	(2) A14	A14	(2) DQ14	DQ14				
(2) DQS_N_0	DQS_N_0	(2) A15	A15	(2) DQ15	DQ15				
(2) DQS_P_1	DQS_P_1								
(2) DQS_N_1	DQS_N_1								

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PageTitle: DRAM\_DDR3

DOC.Number: <Doc>

Sch.FileName: SM2258G-AB-G288 2p5\_G152X16\_D2\_DB\_V01 Rev: 01A

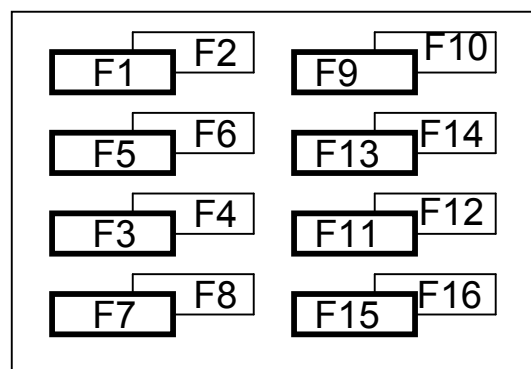
Date: Tuesday, October 18, 2016 Sheet: 6 of 7

TOP View For Flash PCB Placement

TOP BOT

CH0 / CH1: F1 ~ F8

CH2 / CH3: F9 ~ F16



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PageTitle	NF_Mounting_Guide		
DOC.Number	<Doc>		
Sch.FileName	SM2258G-AB-G288 2p5_G152X16_D2_DB_V01	Rev	01A
Date:	Tuesday, October 18, 2016	Sheet	7 of 7