SM2258XT IM/ B16 Flash F/W & ISP Release Information – R0509A0

Introduction
This purpose of this document is to provide release information on the SM22X family F/W and ISP release information

Fix Coverage
■ stands for the **"new fix"** or **"new support"** in the category
☐ stands for the **"no-update"** in the category

■ **MP Tool**	■ **Controller ISP**
☐ **Yield Issue**	☐ **Yield Issue**
■ **Flash Issue**	■ **Flash Issue**
■ 3D TLC Flash	■ 3D TLC Flash
☐ Samsung Flash	☐ Samsung Flash
☐ Toshiba/Sandisk Flash	☐ Toshiba/Sandisk Flash
■ Intel/Micron Flash	■ Intel/Micron Flash
☐ Hynix Flash	☐ Hynix Flash
☐ Others	☐ Others
☐ **MP Tool Bug Fix**	■ **ISP Bug Fix**
■ **MP Tool New Function**	■ **Feature Enhance**
■ **Feature Enhance**	

ISP Revision History

PKG Ver.	ISP Ver.	MPTool Ver.	RDT Ver.	Note
R0524A	R0510A0	R0511A	R0508A0	ISP 1. Fix restore Read Count after devSleep. 2. Fix multi-die cache read terminate CMD issue. 3. Support B0KB/B16 mix shallow erase die. 4. Support B16 1Ch1Way. 5. Fixed last 4 H2f tables which are not re-programmed when UGSD. 6. Modify erase block process when erase-fail block is occurred. 7. Modify retry flow for B16/B17 first read issue. 8. Add 3 Step GC. (Sync. BiCS) 9. Modify setClock for DLL value register meta-stable issue. 10. Adjust first read issue work-around flow. MPTool 1. Intel B16A/B05A/B0KB needs to disable shallow erase flag because ISP didn't check FlashID. 2. Modify Intel B16A/B17A mixed grade issue. 3. Modify RDT "TotalFailCntTH" set wrong issue 1. Disable Shallow Erase flag for all flash types except Micron. 2. Auto-enumerate port in MPTool upon drive insertion. 3. Support Mixed shallow Erase samples to initial card. 4. Add one flag to decide that disable or enable Shallow Erase option at read fail CE.
R0417A	R0327B0	R0416A	R0206A0	ISP 1. Fix FFU reset CPU failed when 1CE multi die. 2. Check shallow erase value before set. 3. Support Erase Interval. 4. Modify address of parameter table. 5. Modify write data size threshold to enter gc. 6. Shrink code 7. Add default read before table retry. 8. Add table retry+soft decode. 9. Fix DLL lock issue. 10. Fix read count bug. MPTool: 1. More display imprint data for micron/spectek B16A/B17A Sorting Tool. 2. Modify extend erase interval range as 1-50 option. 3. More display "Good as bad block count" at final pass result. 4. Record package special setting to MPInfo. 5. Modify that select "Check & Keep RDT" option and do pretest then also need to pre-check capacity enough or not? 6. Modify new MPISP Tag. 7. Always disable Internal/External interleave way setting. 8. Intel B16A/B05A/B0KB needs to disable shallow erase flag because ISP didn't check FlashID.

				9. Modify Intel B16A/B17A mixed grade issue. 10. Modify RDT "TotalFailCntTH" set wrong issue.
Q1225A	Q1204B0	Q1225A	Q1123A0	ISP 1. Disable program suspend by parameter 0xD0 bit0, default: enable. 2. Add the enable sign FW function by CID table. 3. Modify R/W unit of SMART ID for specific customer by define. 4. Enlarge command queue depth for gIntlvWay>4 5. Remove while(1) by using define 6. Dummy write by using define 7. Power on ExtraGC will finish gc state when spare only have 2 block. RDT: 1. Set limitation for max active die number to prevent VDT40 interrupt. MPTool: 1. Modify "TranADJ" fail location display issue. 2. Show "Idle time for background GC" option. 3. Show "Max Data Size for GC (GB)" option. 4. SNChanger tool did not fill 0x20 to SerialNumber string. 5. Take off "Program Mode" option. 6. Modify that disable program suspend flag changed from 0xD0.b0 to 0xD7.b0. 7. Just display 4-CE information at Error message dialog. 8. Add to check FlashID is matched with FlashDB or not. 9. Modify that initial card display error message "Compare Flash Fail (17)" at Intel B16A flash.
Q1124A	Q1115A0	Q1121A	Q1116A0	ISP 1. Enable read count 2. Fixed security erase issue 3. Enable cache read 4. Shrink code size 5. Modify Static SLC Thr. & Wear leveling with CID table. 6. Add force FFU option by mp tool. 7. Fix SLC Erase bug 8. Modify the copy cid table sequence for FFU issue RDT 1. Support retry for BOKB/ L06B 2. Support unbalanced die card mode MPtool 1. Enable Shallow Erase fixed check for B16A and B05A. 2. Add one setting to skip adjust flash clock at tranAdj function for RD debug used. ([OPTION] : SkipAdjClockAtTranAdj) 3. More display which CH-CE occur Flash Time out at [RDT Result] page. 4. Support "Reset SMART Tool". Just reset smart data and can't reset cpu. 5. Enable "RDT Read Retry" option for IM3D flash series at RDT Q1116A0 or later version.
Q1024B	Q0922A0	Q1020B	Q1006A0	ISP: 1. Add Swallow Erase Feature.

				2. Fix setClock DLL fail issue. 3. Fix Read Reclaim. 4. Add the MASK SMART ID 0x05 & 0xC5 (new bad block count) by MP tool option. 5. Add record Read TLC UECC when block had already mark as 0xF1(chkPostWriteRead). MPISP: 1. Modified eraseAll, add reset cmd. 2. Modify tran physical Ch bug. 3. Fix tranRTC issue. 4. Fix bug that getFlashType may find wrong flash id if channel 0 not exist. RDT: 1. Support Read ID table. 2. Fix code size issue for B16. MPTool: 1. Display GenChCeMap fail information 2. Restore InfoBlock if initial card fail 3. Support manual unbalanced mode initial card. 4. Fix bug: Reference RDT bad twice, can't be recognized by host.
Q0817B	Q0816C0	Q0816A	Q0808A0	ISP 1. Fix B16 2Ch1Way UGSD Fail. 2. Add the SMART extension table check point. 3. Initial the different customer temperature. 4. Fix bug of moveRiskyPage() with 4Plane, 16k per plane. 5. Define the customer WAF info for smart. 6. Add some unbalance check code for CacheRead 7. Fix read retry bug 8. Add GC Idle condition 9. Fix SLC/TLC erase info invert issue 10. Add SLC/TLC nand read count for HIK 11. Improve WL flow. 12. Support B16 toggle mode with DDR200 13. Support Devslp MPISP: 1. Flash clock under 100Mhz do not need differential mode. 2. Fix bug that TranAdj would hang up. 3. Support distinguish ES 4. Modify SmithWindow, Controller ODT settings 5. Fix disabling TranAdj. 6. Modify identify device, don't clear buffer flag. RDT: 1. Modify RDT test flow to cover JIRA issue. 2. Add RDT setting option "Bypass read check for first 2 loop" 3. Add bypass Erase/Program fail status option. 4. Fixed CH remapping bug. 5. Add bypass fail bit for last test block 6. Add force single plane program option 7. Fixed Reverse block order test mode bug. MPTool: 1. Pre-Check capacity at "Reference RDT Bad" pretest option to initial card.

				2. Add "Bypass read check for first 2 loop" option 3. Remove "New Bad Block" display at SSD Information dialog. 4. Add "Ignore Erase Fail" checkbox to set CID[0x33].b0 5. Add "bypass status fail bit" option at [RDT Setting] dialog. 6. Add "Force single plane program" option at [RDT Setting] dialog. 7. Fix bug: "Test Block Cnt" display nothing at [RDT Result] page. 8. Fix bug: Display gibberish at [ID Table] page when user use special string to fill SN/VendorSpecific. (Need to change font type) 9. Add Flash Clock "DDR-300" option. 10. Support that Micron B16A Distinguish ES function. 11. Fix bug: CPU Clock display wrong at SSD Information dialog. 12. Default Toggle mode and Flash Clock > 100MHz need to always enable differential signal. 13. More save "Temp" information at RDT log file. 14. Modify I/M SDR Mode corresponding setting 15. Pre-Check Capacity fail also need to parse super block counts information at error dialog. 16. Fix bug: DriveSettingTable may assign wrong when selected "Auto" capacity option. 17. Add "Bypass TranADJ" function.
Q0627A	Q0627A0	Q0620A	Q0607A0	ISP 1. First formal release to support Intel and Micron B16 NAND flash. 2. Not support Devslp yet.

Note:

1. F/W and ISP update is recommended.
2. History # is denoted by “Version-Date” .