AU6989SN-GT

USB2.0 Universal Flash Disk Controller

Technical Reference Manual

Rev. 1.00
Jan., 2014

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Revision History

Date	Revision	Description
Jan. 2014	1.00	Official Release

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1. Introduction

1.1 Description

The AU6989SN-GT (embedded Crystal) USB 2.0 Flash Disk Controller is the best high performance solutions for MLC, TLC SDR/DDR NAND flash with multiple dies data flash. AU6989SN-GT designs embedded crystal with Alcor's patent and it has 72bit/1K BCH ECC engines to correct high error bits of new generation flash (1x/1y nm) and provide the well performance for TLC flash especial DDR flash.

AU6989SN-GT provides dual channel access and ISP (In-System Programming) technologies with Alcor's patent, which are the most important features to allow manufacturers building high performance UFD easily and to have the flexibility of adopting different source of flash chips.

To enhance the usefulness and manageability of UFD further, Alcor Micro develops a smart application program iStar (Partition/Password Operation Tool) as a handy utility in managing partition, password and security. Having iStar as the companion of UFD, the data in a UFD could be protected from unauthorized access successfully.

1.2 Features

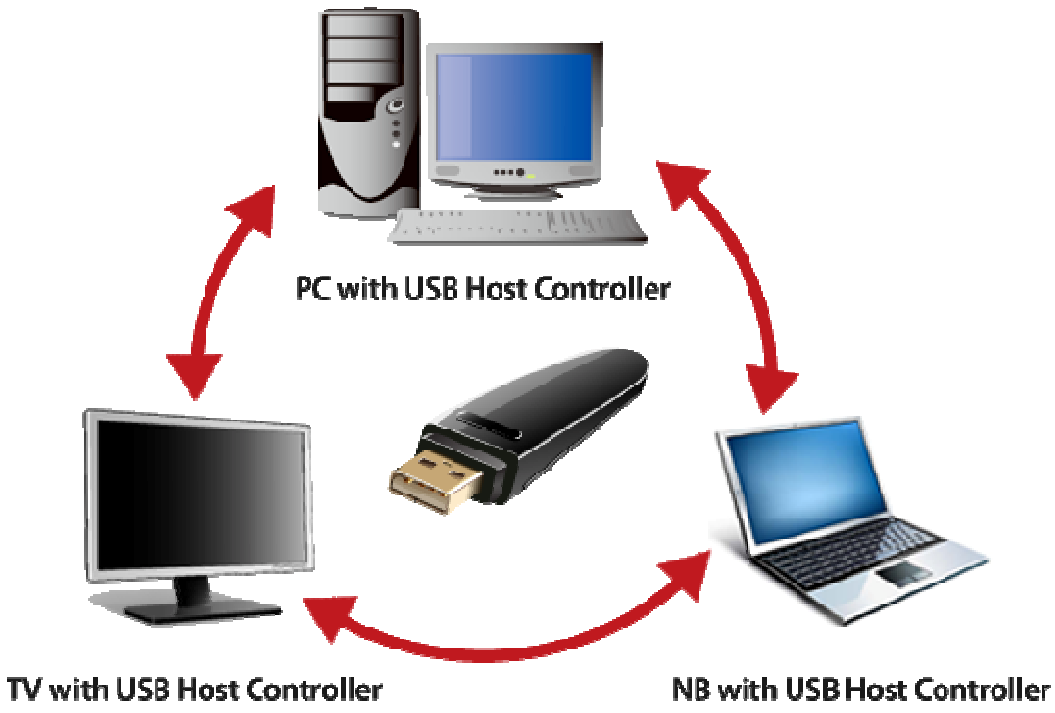
- PCBs are pin compatible with AU69XX USB2.0 series
- Integrated build-in Regulator
- Integrated build-in Crystal with Alcor's patent
- Supports 72bit/1K BCH ECC engines
- Supports new generation MLC/TLC flash
- Supports Toggle/ONFI DDR flash
- Not support the flash ECC requirement under 24bit/1K
- Well performance in TLC DDR flash
- Improved read performance reach 32MB/Sec
- Integrates hardware DMA engine to tune up the operation performance
- Works with default driver under the environments of Windows ME, Windows 2000, Windows XP, Vista, Window7, Windows 8, Mac 9.2, Mac OS 10.x. Using Alcor Micro's vendor driver for the environment under Windows 98SE
- Low power operation with SDR/DDR flash
- Supports software write protection
- Support Auto Run function

- Support erasable and read-only mode AP Disk
- Companion application program with UFD – iStar available for users
  - To have UFD partition management function
  - To do password protection for the security in data access
  - To guard data files with software write protection function
  - To lock up PC by UFD as the key
- Available in 48-pin LQFP 7x7mm / TQFP_7x7mm / QFN_6x6mm / QFN_7x7mm package to support 4CE pin flashx2pcs
- Available in 64-pin LQFP 7x7mm / TQFP_7x7mm package to support 4CE pin flashx4pcs

2. Application Block Diagram

The following figure shows the application diagram of a typical flash disk product with AU6989SN-GT. By connecting the flash disk to a desktop or notebook PC through USB bus, AU6989SN-GT is then turned into a bus-powered, high speed USB disk, which can be used as a bridge for data transfer between Desktop PC and Notebook PC.

Figure 2.1 Block Diagram



3. Pin Assignment

AU6989SN-GT is available in 48-pin LQFP & TQFP package. Below diagram shows signal name of each pin and table in the following page describes each pin in detail.

Figure 3.1 AU6989SN-GT-GHL 48-pin Pin Assignment Diagram

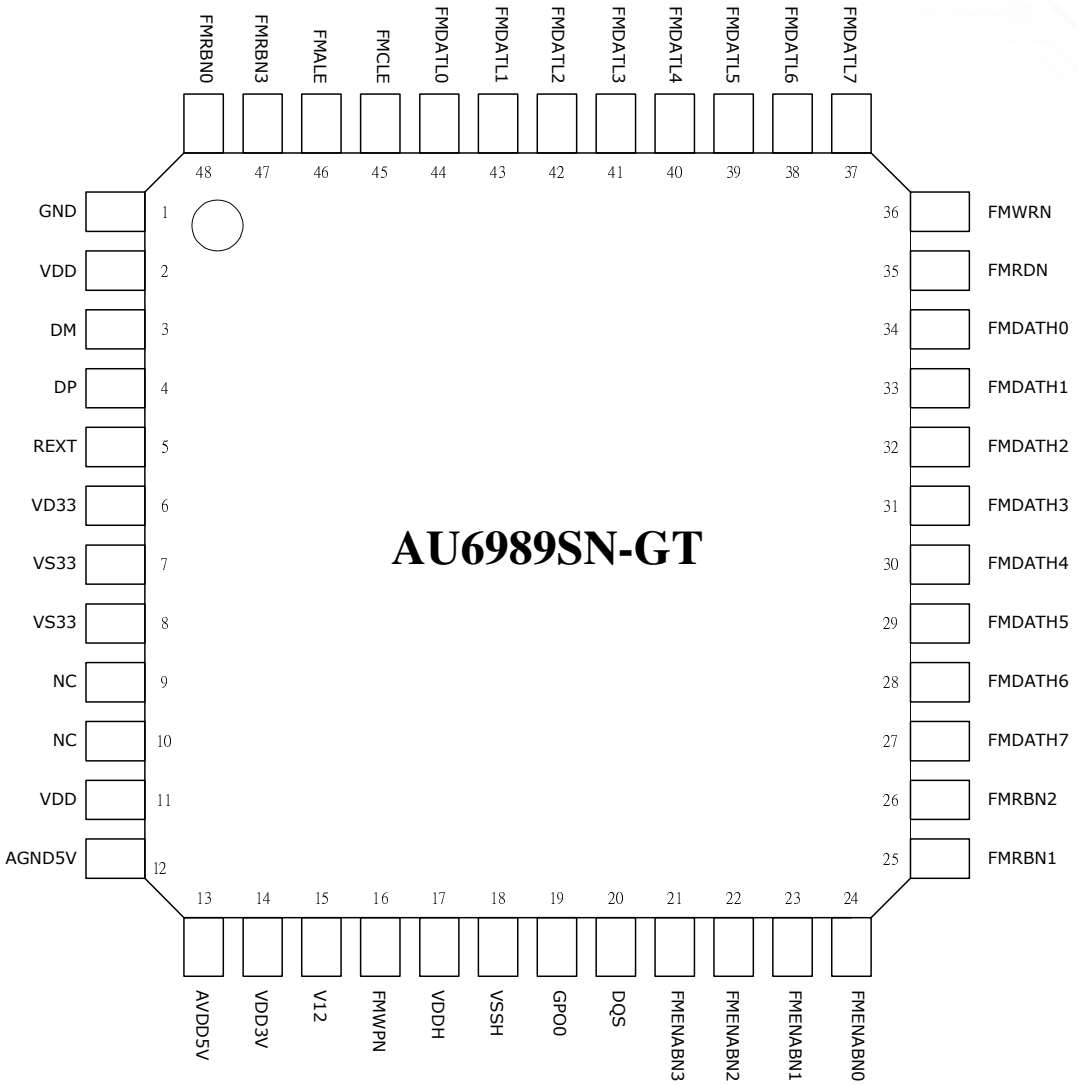


Table 3.1 AU6989SN-GT-GHL 48-pin Pin Descriptions

Pin #	Pin Name	I/O	Description
1	GND	I	Ground
2	VDD	I	1.2V input power pin
3	DM	I	USB DM
4	DP	I	USB DP
5	REXT	I	External resistor 330 to ground
6	VD33	I	3.3V input power pin
7	VS33	I	Ground
8	VS33		Ground
9	NC		
10	NC		
11	VDD		1.2V input power pin
12	AGND5V	I	Ground
13	AVDD5V	I	5V input power pin
14	VDD3V	O	3.3V output power pin
15	V12	O	1.2V output for Core
16	FMWPN	O	Flash Write protect pin
17	VDDH	I	3.3V input power pin
18	VSSH	I	Ground
19	GPO0	O	Blanking when system access
20	DQS	I/O	Flash data strobe
21	FMENABN3	O	Flash 3 select pin
22	FMENABN2	O	Flash 2 select pin
23	FMENABN1	O	Flash 1 select pin
24	FMENABN0	O	Flash 0 select pin
25	FMRBN1	I	Flash 1 ready pin
26	FMRBN2	I	Flash 2 ready pin
27	FMDATH7	I/O	Flash high data 7 pin
28	FMDATH6	I/O	Flash high data 6 pin
29	FMDATH5	I/O	Flash high data 5 pin
30	FMDATH4	I/O	Flash high data 4 pin
31	FMDATH3	I/O	Flash high data 3 pin
32	FMDATH2	I/O	Flash high data 2 pin

Pin #	Pin Name	I/O	Description
33	FMDATH1	I/O	Flash high data 1 pin
34	FMDATH0	I/O	Flash high data 0 pin
35	FMRDN	O	Flash read signal
36	FMWRN	O	Flash write signal
37	FMDATL7	I/O	Flash low data 7 pin
38	FMDATL6	I/O	Flash low data 6 pin
39	FMDATL5	I/O	Flash low data 5 pin
40	FMDATL4	I/O	Flash low data 4 pin
41	FMDATL3	I/O	Flash low data 3 pin
42	FMDATL2	I/O	Flash low data 2 pin
43	FMDATL1	I/O	Flash low data 1 pin
44	FMDATL0	I/O	Flash low data 0 pin
45	FMCLE	O	Flash command latch pin
46	FMALE	O	Flash address latch pin
47	FMRBN3	I	Flash 3 ready pin
48	FMRBN0	I	Flash 0 ready pin

The following figure shows signal name of each pin in 64-pin package and the table in the page after describes each pin in detail.

Figure 3.2 AU6989SN-GT 64-pin Pin Assignment Diagram

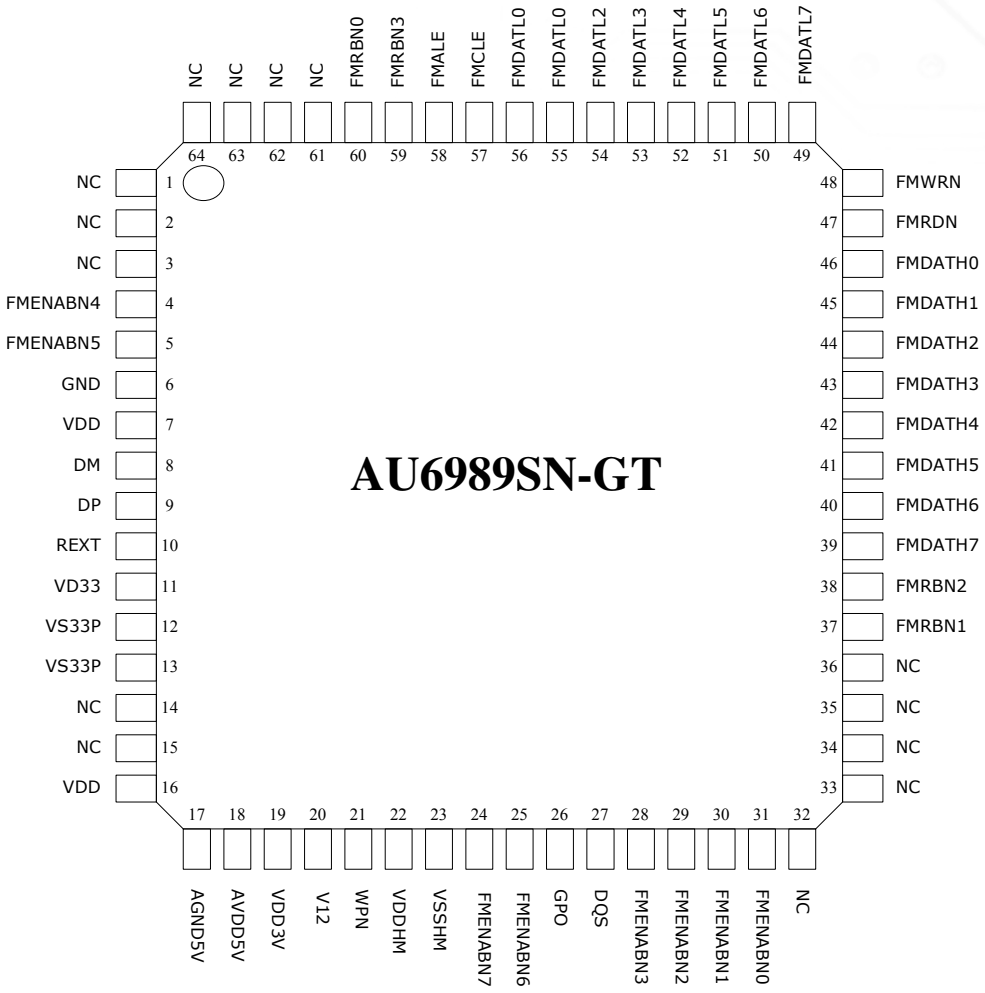


Table 3.2 AU6989SN-GT 64-pin Pin Descriptions

Pin #	Pin Name	I/O	Description
1	NC	-	NC
2	NC	-	NC
3	NC	-	NC
4	FMENABN4	O	Flash 4 select pin
5	FMENABN5	O	Flash 5 select pin
6	GND	GND	Ground
7	VDD	I	1.2V input power pin
8	DM	I/O	USB DM
9	DP	I/O	USB DP
10	REXT	I	External resistor 330 to ground
11	VD33	I	3.3V input power pin
12	VS33P	GND	Ground
13	VS33P	GND	Ground
14	NC	-	NC
15	NC	-	NC
16	VDD	I	1.2V input power pin
17	AGND5V	I	Ground
18	AVDD5V	I	5V input power pin
19	VDD3V	O	3.3V output power pin
20	V12	O	1.2V output for Core
21	FMWPN	O	Flash Write Protect Pin(Low Active)
22	VDDHM	I	3.3V input power pin
23	VSSHM	GND	Ground
24	FMENABN7	O	Flash 7 select pin
25	FMENABN6	O	Flash 6 select pin
26	GPO	O	blanking when system access
27	DQS	I/O	Flash data strobe
28	FMENABN3	O	Flash 3 select pin
29	FMENABN2	O	Flash 2 select pin
30	FMENABN1	O	Flash 1 select pin
31	FMENABN0	O	Flash 0 select pin
32	NC	-	NC

Pin #	Pin Name	I/O	Description
33	NC	-	NC
34	NC	-	NC
35	NC	-	NC
36	NC	-	NC
37	FMRBN1	I	Flash 1 ready pin
38	FMRBN2	I	Flash 2 ready pin
39	FMDATH7	I/O	Flash high data 7 pin
40	FMDATH6	I/O	Flash high data 6 pin
41	FMDATH5	I/O	Flash high data 5 pin
42	FMDATH4	I/O	Flash high data 4 pin
43	FMDATH3	I/O	Flash high data 3 pin
44	FMDATH2	I/O	Flash high data 2 pin
45	FMDATH1	I/O	Flash high data 1 pin
46	FMDATH0	I/O	Flash high data 0 pin
47	FMRDN	O	Flash read signal
48	FMWRN	O	Flash write signal
49	FMDATL7	I/O	Flash low data 7 pin
50	FMDATL6	I/O	Flash low data 6 pin
51	FMDATL5	I/O	Flash low data 5 pin
52	FMDATL4	I/O	Flash low data 4 pin
53	FMDATL3	I/O	Flash low data 3 pin
54	FMDATL2	I/O	Flash low data 2 pin
55	FMDATL1	I/O	Flash low data 1 pin
56	FMDATL0	I/O	Flash low data 0 pin
57	FMCLE	O	Flash command latch pin
58	FMALE	O	Flash address latch pin
59	FMRBN3	I	Flash 3 ready pin
60	FMRBN0	I	Flash 0 ready pin
61	NC	-	NC
62	NC	-	NC
63	NC	-	NC

Pin #	Pin Name	I/O	Description
64	NC	-	NC

Figure 3.3 AU6989SN-GT-GPL 48-pin Pin Assignment Diagram

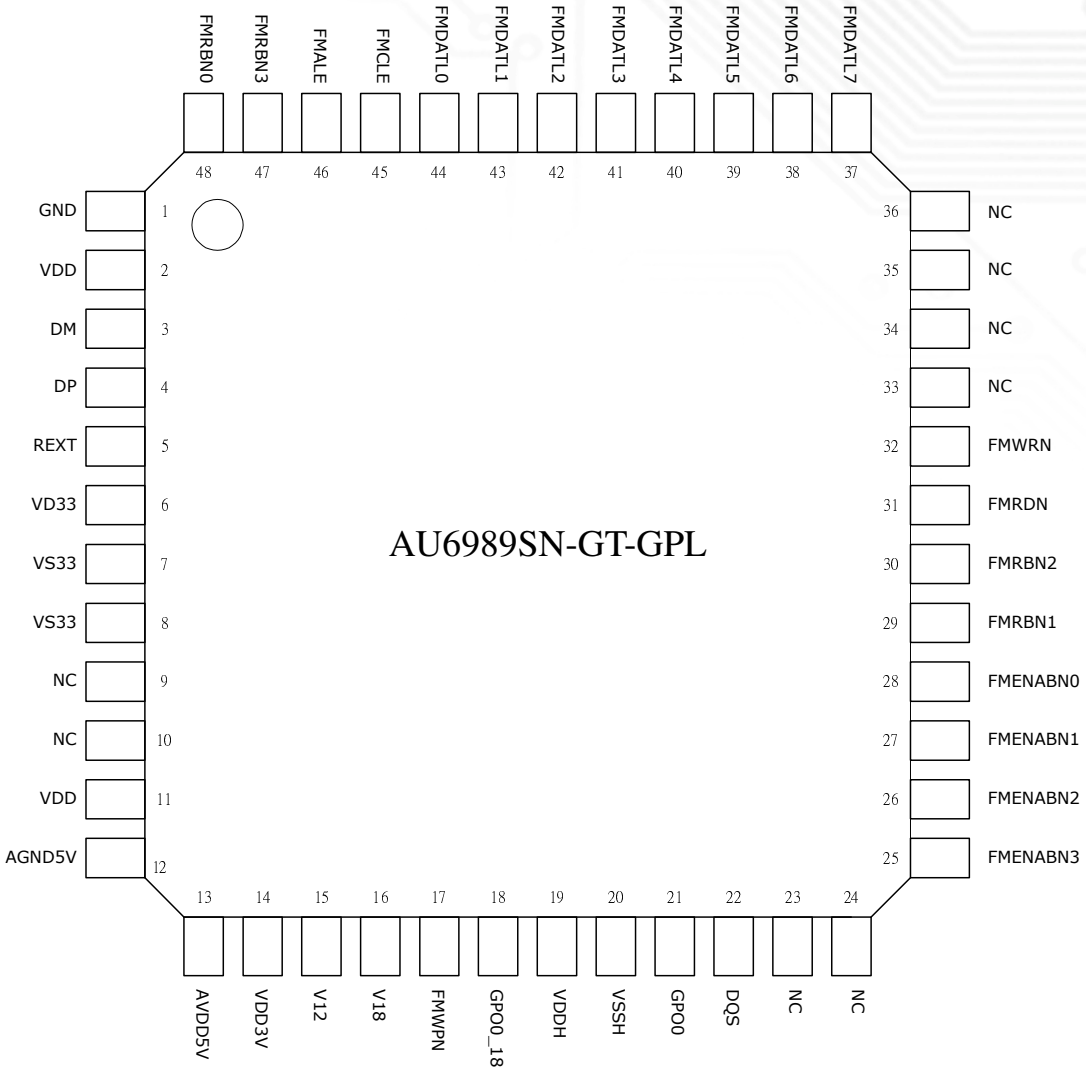


Table 3.3 AU6989SN-GT-GPL 48-pin Pin Descriptions

Pin #	Pin Name	I/O	Description
1	GND	I	Ground
2	VDD	I	1.2V input power pin
3	DM	I	USB DM
4	DP	I	USB DP
5	REXT	I	External resistor 330 to ground
6	VD33	I	3.3V input power pin
7	VS33	I	Ground
8	VS33		Ground
9	NC		
10	NC		
11	VDD		1.2V input power pin
12	AGND5V	I	Ground
13	AVDD5V	I	5V input power pin
14	VDD3V	O	3.3V output power pin
15	V12	O	1.2V output for Core
16	V18	O	1.8V output
17	FMWPN	O	Flash Write protect pin
18	NC		
19	VDDH	I	FLASH IO input power pin
20	VSSH	I	Ground
21	GPO	O	LED Blanking when system access
22	DQS	I/O	Flash data strobe
23	NC		
24	NC		
25	FMENABN3	O	Flash 3 select pin
26	FMENABN2	O	Flash 2 select pin
27	FMENABN1	O	Flash 1 select pin
28	FMENABN0	O	Flash 0 select pin
29	FMRBN1	I	Flash 1 ready pin
30	FMRBN2	I	Flash 2 ready pin
31	FMRDN	O	Flash read signal
32	FMWRN	O	Flash write signal

Pin #	Pin Name	I/O	Description
33	NC		
34	NC		
35	NC		
36	NC		
37	FMDATL7	I/O	Flash low data 7 pin
38	FMDATL6	I/O	Flash low data 6 pin
39	FMDATL5	I/O	Flash low data 5 pin
40	FMDATL4	I/O	Flash low data 4 pin
41	FMDATL3	I/O	Flash low data 3 pin
42	FMDATL2	I/O	Flash low data 2 pin
43	FMDATL1	I/O	Flash low data 1 pin
44	FMDATL0	I/O	Flash low data 0 pin
45	FMCLE	O	Flash command latch pin
46	FMALE	O	Flash address latch pin
47	FMRBN3	I	Flash 3 ready pin
48	FMRBN0	I	Flash 0 ready pin

Figure 3.4 AU6989SN-GT-GBN 48-pin Pin Assignment Diagram

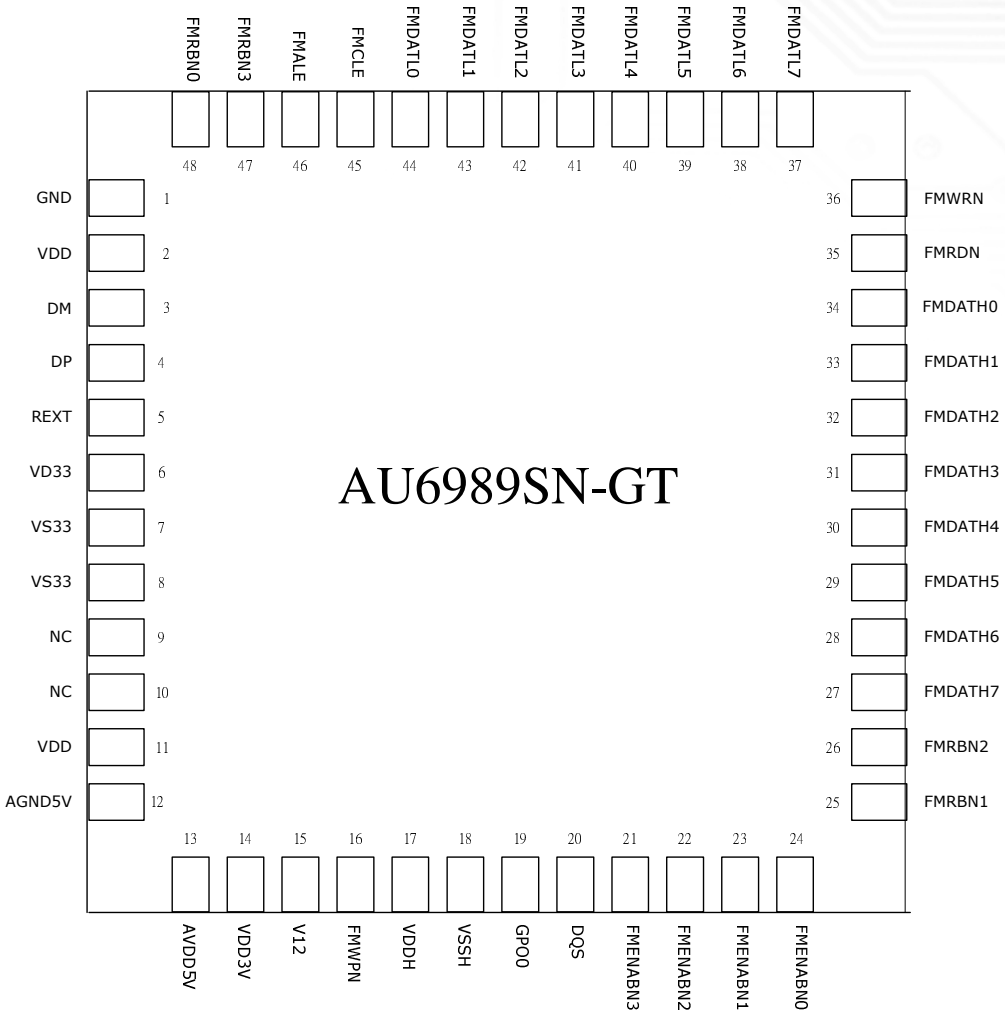


Table 3.4 AU6989SN-GT-GBN 48-pin Pin Descriptions

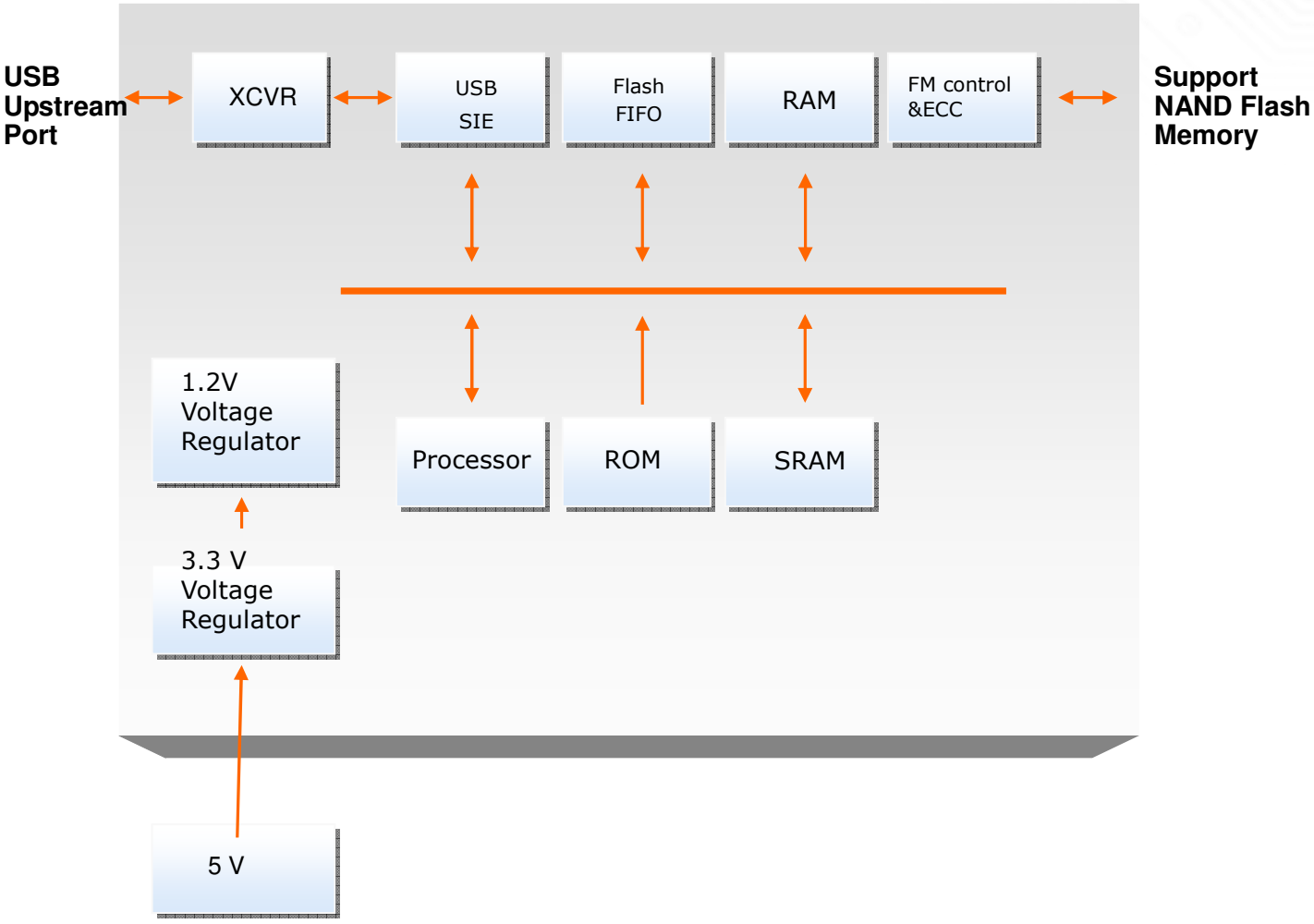
Pin #	Pin Name	I/O	Description
1	GND	I	Ground
2	VDD	I	1.2V input power pin
3	DM	I	USB DM
4	DP	I	USB DP
5	REXT	I	External resistor 330 to ground
6	VD33	I	3.3V input power pin
7	VS33	I	Ground
8	VS33		Ground
9	NC		
10	NC		
11	VDD		1.2V input power pin
12	AGND5V	I	Ground
13	AVDD5V	I	5V input power pin
14	VDD3V	O	3.3V output power pin
15	V12	O	1.2V output for Core
16	FMWPN	O	Flash Write protect pin
17	VDDH	I	3.3V input power pin
18	VSSH	I	Ground
19	GPO0	O	Blanking when system access
20	DQS	I/O	Flash data strobe
21	FMENABN3	O	Flash 3 select pin
22	FMENABN2	O	Flash 2 select pin
23	FMENABN1	O	Flash 1 select pin
24	FMENABN0	O	Flash 0 select pin
25	FMRBN1	I	Flash 1 ready pin
26	FMRBN2	I	Flash 2 ready pin
27	FMDATH7	I/O	Flash high data 7 pin
28	FMDATH6	I/O	Flash high data 6 pin
29	FMDATH5	I/O	Flash high data 5 pin
30	FMDATH4	I/O	Flash high data 4 pin
31	FMDATH3	I/O	Flash high data 3 pin
32	FMDATH2	I/O	Flash high data 2 pin

Pin #	Pin Name	I/O	Description
33	FMDATH1	I/O	Flash high data 1 pin
34	FMDATH0	I/O	Flash high data 0 pin
35	FMRDN	O	Flash read signal
36	FMWRN	O	Flash write signal
37	FMDATL7	I/O	Flash low data 7 pin
38	FMDATL6	I/O	Flash low data 6 pin
39	FMDATL5	I/O	Flash low data 5 pin
40	FMDATL4	I/O	Flash low data 4 pin
41	FMDATL3	I/O	Flash low data 3 pin
42	FMDATL2	I/O	Flash low data 2 pin
43	FMDATL1	I/O	Flash low data 1 pin
44	FMDATL0	I/O	Flash low data 0 pin
45	FMCLE	O	Flash command latch pin
46	FMALE	O	Flash address latch pin
47	FMRBN3	I	Flash 3 ready pin
48	FMRBN0	I	Flash 0 ready pin

4. System Architecture and Reference Design

4.1 AU6989SN-GT Block Diagram

Figure 4.1 AU6989SN-GT Block Diagram



5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{DDH}	Power Supply	-0.3 to V_{DDH} +0.3	V
V_{IN}	Input Signal Voltage	-0.3 to 3.6	V
V_{OUT}	Output Signal Voltage	-0.3 to V_{DDH} +0.3	V
T_{STG}	Storage Temperature	-40 to 150	^{O}C
A_{DD}	5V Power Supply	4.5 to 5.5	V

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
A_{DD}	5V Power Supply	4.75	5.0	5.25	V
V_{DDH}	Power Supply	3.0	3.3	3.6	V
V_{DD}	Digital Supply	1.14	1.2	1.26	V
V_{IN}	Input Signal Voltage	0	3.3	3.6	V
T_{OPR}	Operating Temperature	0		70	^{O}C

5.3 General DC Characteristics

Table 5.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IN}	Input current	No pull-up or pull-down	-10	±1	10	µA
I_{OZ}	Tri-state leakage current		-10	±1	10	µA
C_{IN}	Input capacitance	Pad Limit		2.8		ρF
C_{OUT}	Output capacitance	Pad Limit		2.8		ρF
C_{BID}	Bi-directional buffer capacitance	Pad Limit		2.8		ρF

5.4 DC Electrical Characteristics of 3.3V I/O Cells

Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells

SYMBOL	PARAMETER	CONDITIONS	Limits			UNIT
			MIN	TYP	MAX	
V_{DDH}	Power supply	3.3V I/O	3.0	3.3	3.6	V
V_{il}	Input low voltage	LVTTL			0.8	V
V_{ih}	Input high voltage		2.0			V
V_{ol}	Output low voltage	$\lvert I_{ol} \rvert$ =2~16mA			0.4	V
V_{oh}	Output high voltage	$\lvert I_{oh} \rvert$ =2~16mA	2.4			V
R_{pu}	Input pull-up resistance	PU=high, PD=low	55	75	110	KΩ
R_{pd}	Input pull-down resistance	PU=low, PD=high	40	75	150	KΩ
I_{in}	Input leakage current	V_{in}= V_{D33P} or 0	-10	±1	10	μA
I_{oz}	Tri-state output leakage current		-10	±1	10	μA

5.5 USB Transceiver Characteristics

Table 5.5 Electrical characteristics

SYMBOL	PARAMETER	CONDITIONS	Limits			UNIT
			MIN	TYP	MAX	
V_{D33}	Analog supply Voltage		3.0	3.3	3.6	V
V_{DDU} V_{DDA}	Digital supply Voltage		1.14	1.2	1.26	V
I_{CC}	Operating supply current	High speed operating at 480		65		mA
$I_{CC(susp)}$	Suspend supply current	In suspend mode, current with 1.5kΩ pull-up resistor on pin RPU disconnected		300		μA

Table 5.6 Static characteristic：Digital pin

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input levels						
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		2.0			V
Output levels						
V_{OL}	Low-level output voltage				0.2	V
V_{OH}	High-level output voltage		VDDH-0.2			V

Table 5.7 Static characteristic：Analog I/O pins（DP/DM）

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
USB2.0 Transceiver (HS)						
Input Levels (differential receiver)						
V_{HSDIFF}	High speed differential input sensitivity	$\lvert V_{I(DP)}-V_{I(DM)} \rvert$ measured at the connection as application circuit	300			mV
V_{HSCM}	High speed data signaling common mode voltage range		-50		500	mV
V_{HSSQ}	High speed squelch detection threshold	Squelch detected			100	mV
		No squelch detected	150			mV
V_{HSDSC}	High speed disconnection detection threshold	Disconnection detected	625			mV
		Disconnection not detected			525	mV
Output Levels						
V_{HSOI}	High speed idle level output voltage(differential)		-10		10	mV
V_{HSOL}	High speed low level output voltage(differential)		-10		10	mV
V_{HSOH}	High speed high level output voltage(differential)		360		440	mV
V_{CHIRPJ}	Chirp-J output voltage（differential）		700		1100	mV
V_{CHIRPK}	Chirp-K output voltage（differential）		-900		-500	mV
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used as internal chip only	3	6	9	Ω

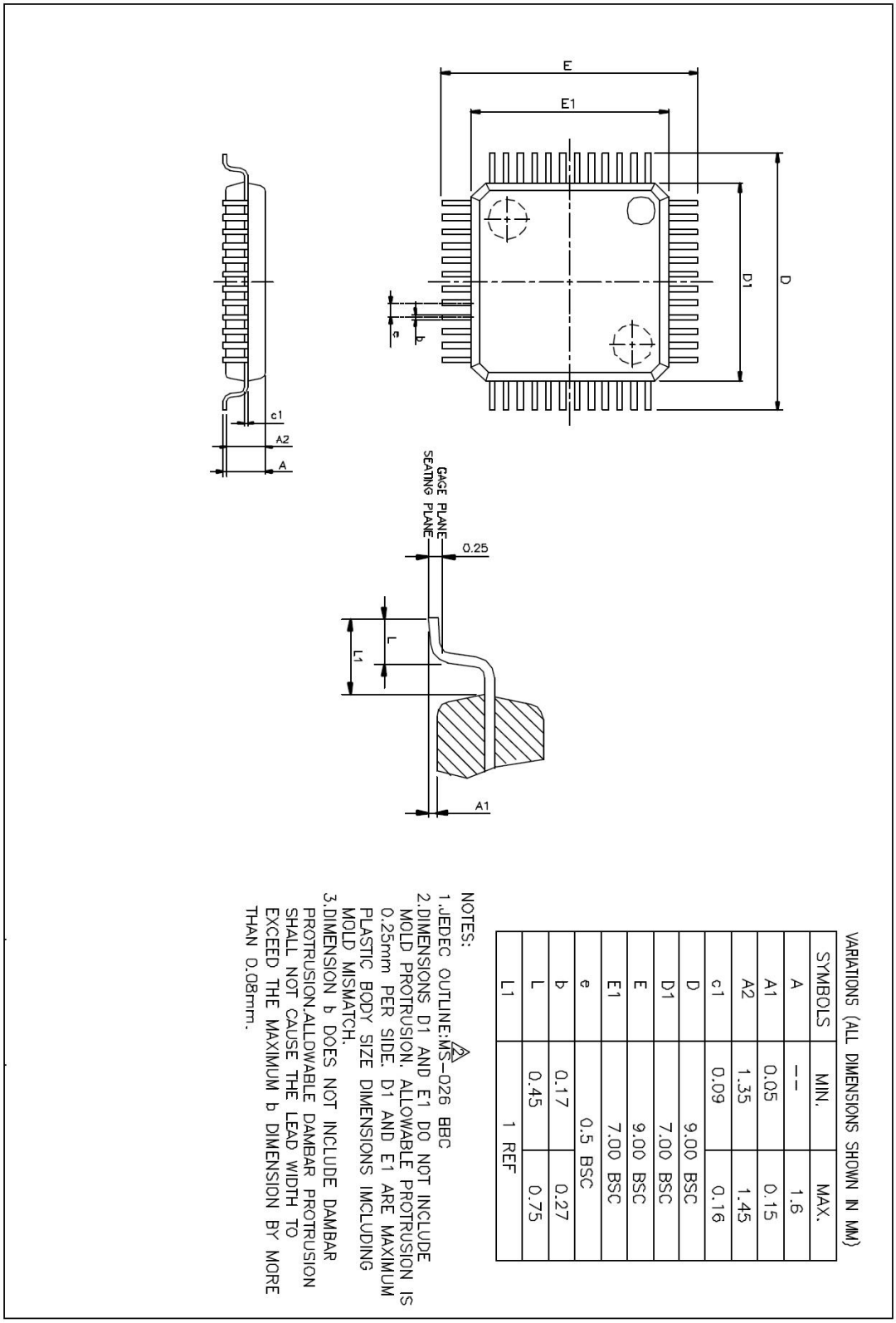
		Overall resistance including external resistor	40.5	45	49.5	
Termination						
V_{TERM}	Termination voltage for pull-up resistor on pin RPU		3.0		3.6	V
USB1.1 Transceiver (FS)						
Input Levels（differential receiver）						
V_{DI}	Differential input sensitivity	$\lvert V_{I(DP)}-V_{I(DM)} \rvert$	0.2			V
V_{CM}	Differential common mode voltage		0.8		2.5	V
Input Levels（single-ended receivers）						
V_{SE}	Single ended receiver threshold		0.8		2.0	V
Output levels						
V_{OL}	Low-level output voltage		0		0.3	V
V_{OH}	High-level output voltage		2.8		3.6	V

Table 5.8 Dynamic characteristic：Analog I/O pins（DP/DM）

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Driver Characteristics						
High-Speed Mode						
t_{HSR}	High-speed differential rise time		500			ps
t_{HSF}	High-speed differential fall time		500			ps
Full-Speed Mode						
t_{FR}	Rise time	CL=50pF；10 to 90 % of $\lvert V_{OH}-V_{OL} \rvert$；	4		20	ns
t_{FF}	Fall time	CL=50pF；90 to 10 % of $\lvert V_{OH}-V_{OL} \rvert$；	4		20	ns
t_{FRMA}	Differential rise/fall time matching（t_{FR} / t_{FF}）	Excluding the first transition from idle mode	90		110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V

6. Mechanical Information

Figure 6.1 48 LQFP Mechanical Information Diagram



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

NOTES:

1.JEDEC OUTLINE:MS-026 BBC

2.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.

3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

Figure 6.2 48 TQFP_7x7mm Mechanical Information Diagram

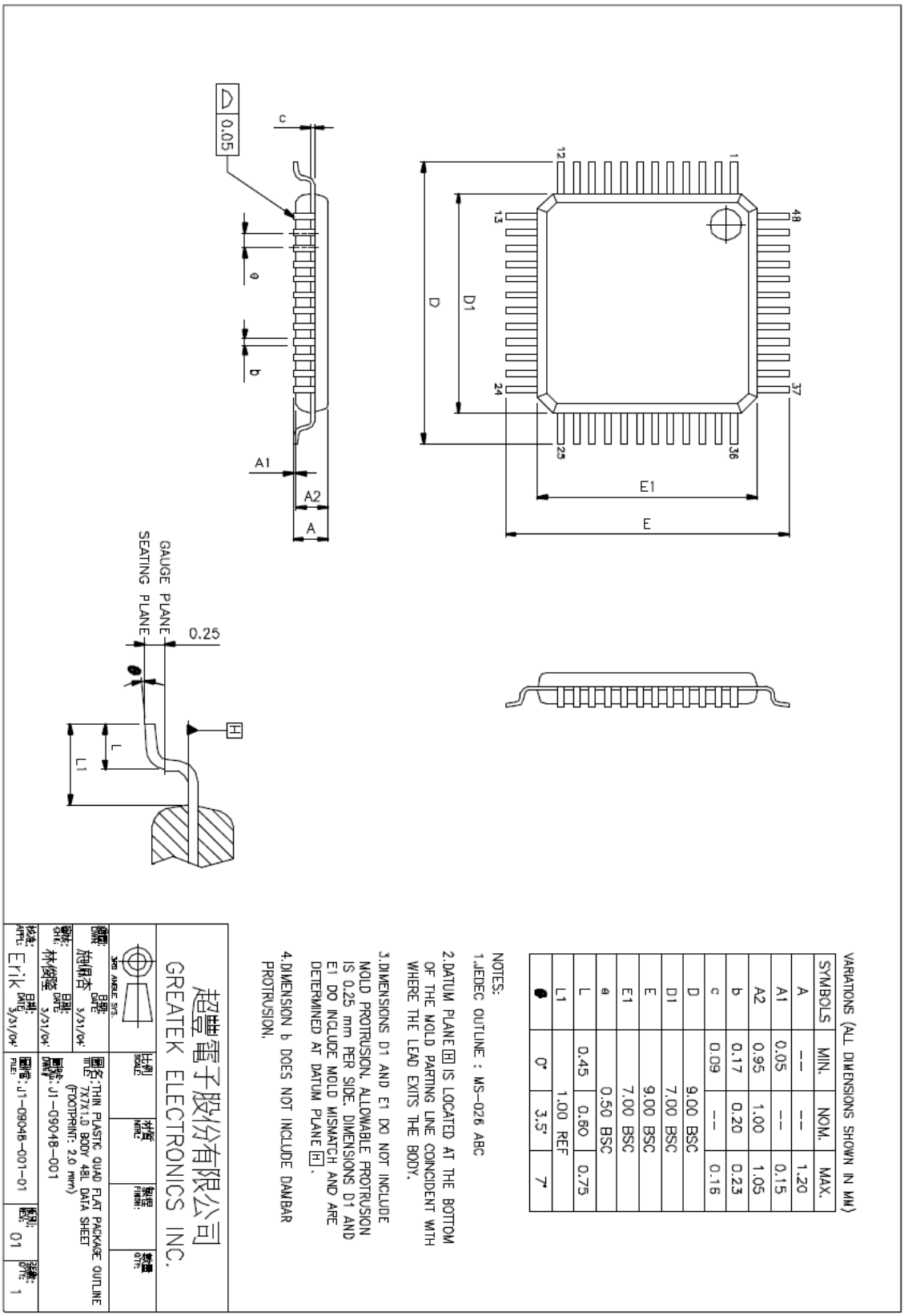
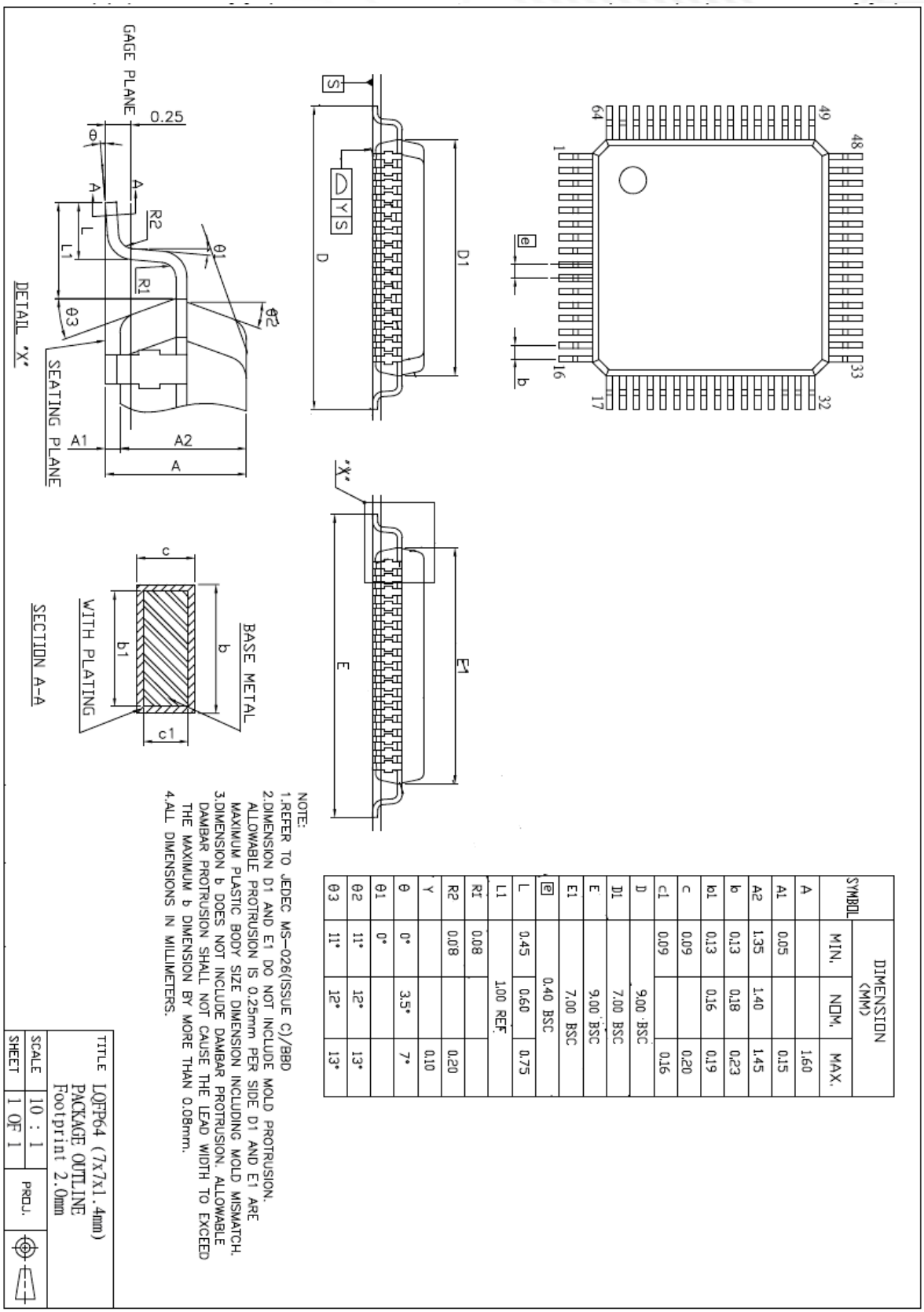


Figure 6.3 64 LQFP_7x7mm Mechanical Information Diagram



SYMBOL	DIMENSION (MM) MIN.	NOM.	MAX.
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
b1	0.13	0.16	0.19
c	0.09		0.20
c1	0.09		0.16
D		9.00 BSC	
D1		7.00 BSC	
E		9.00 BSC	
E1		7.00 BSC	
e		0.40 BSC	
L	0.45	0.60	0.75
L1		1.00 REF.	
R1	0.08		
R2	0.08		0.20
Y			0.10
θ	0°	3.5°	7°
θ1	0°		
θ2	11°	12°	13°
θ3	11°	12°	13°

Figure 6.4 64 TQFP_7x7mm Mechanical Information Diagram

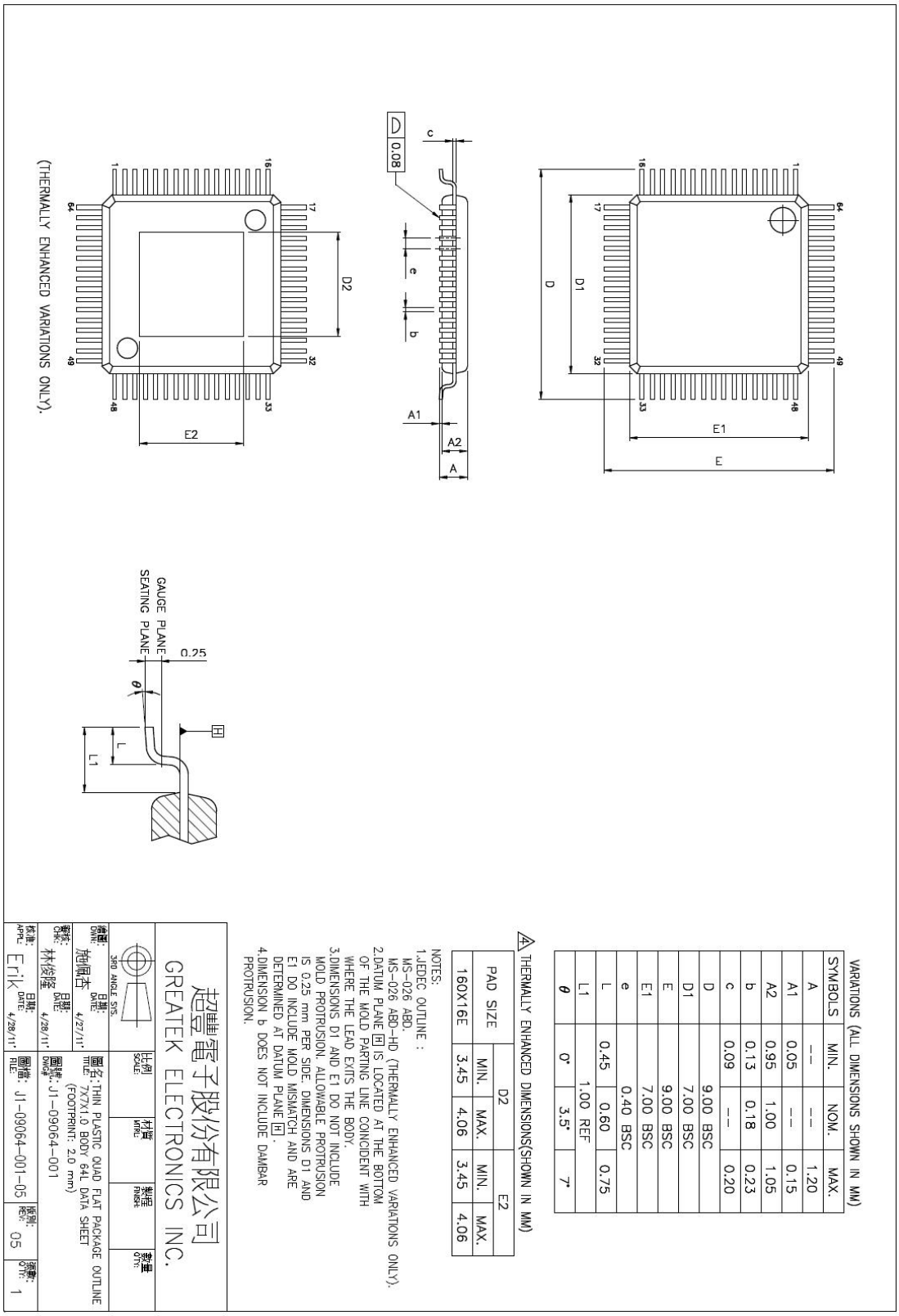
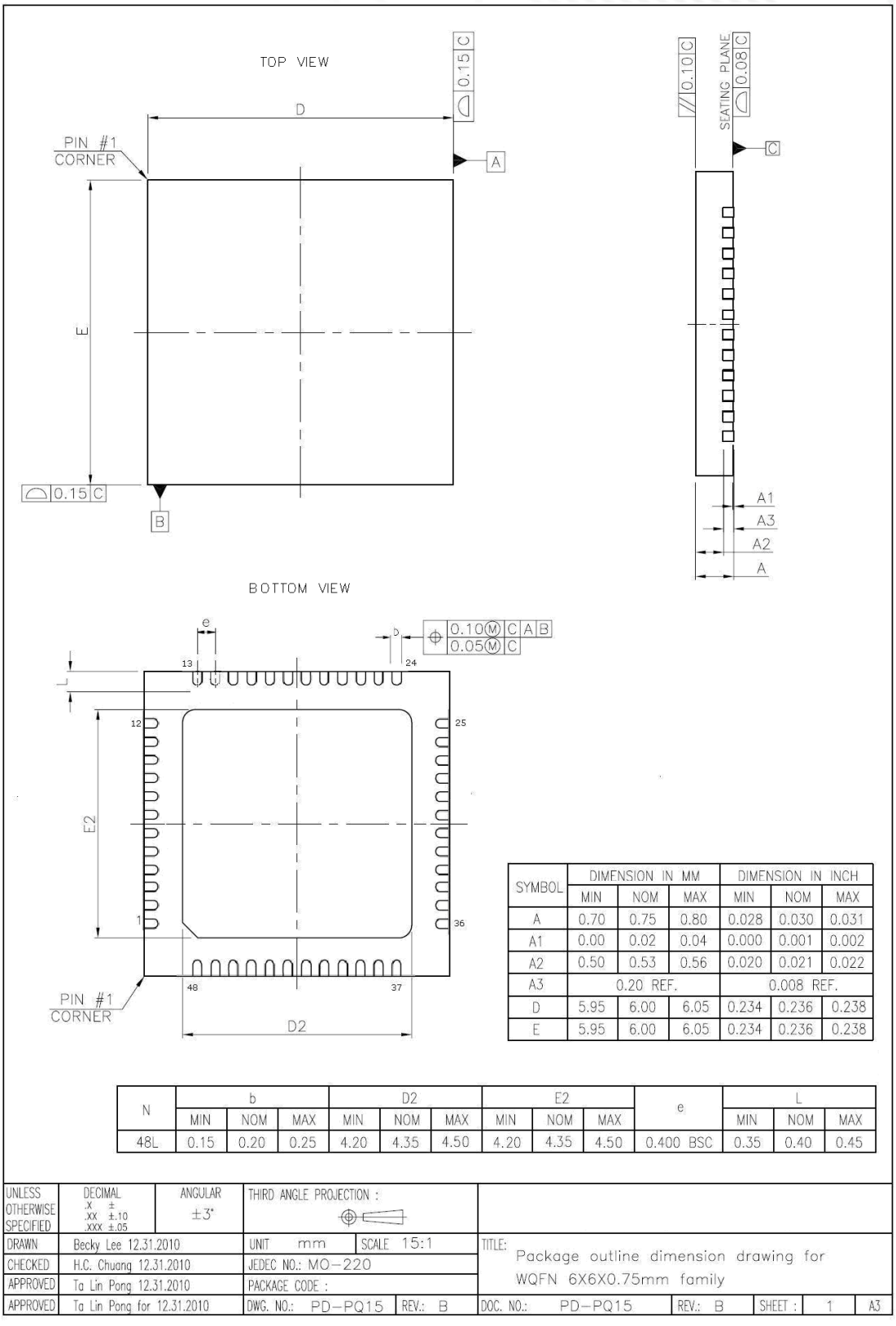


Figure 6.5 48 QFN_6x6mm Mechanical Information Diagram

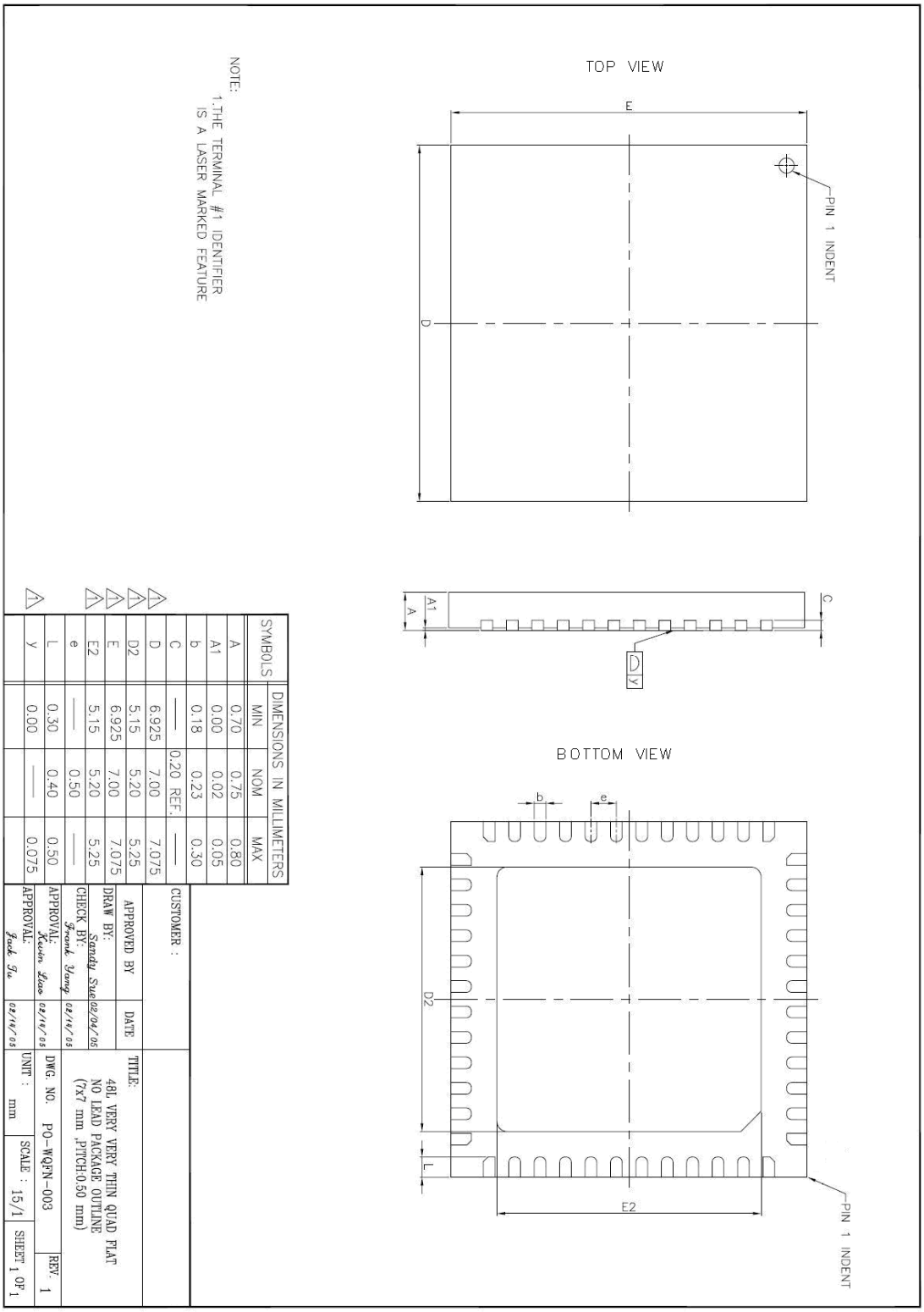


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.04	0.000	0.001	0.002
A2	0.50	0.53	0.56	0.020	0.021	0.022
A3	0.20 REF.			0.008 REF.		
D	5.95	6.00	6.05	0.234	0.236	0.238
E	5.95	6.00	6.05	0.234	0.236	0.238

N	b			D2			E2			e	L		
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX		MIN	NOM	MAX
48L	0.15	0.20	0.25	4.20	4.35	4.50	4.20	4.35	4.50	0.400 BSC	0.35	0.40	0.45

UNLESS OTHERWISE SPECIFIED	DECIMAL .X ± .XX ±.10 .XXX ±.05	ANGULAR ±3°	THIRD ANGLE PROJECTION :		
DRAWN	Becky Lee 12.31.2010	UNIT mm	SCALE 15:1	TITLE: Package outline dimension drawing for WQFN 6X6X0.75mm family	
CHECKED	H.C. Chuang 12.31.2010	JEDEC NO.: MO-220			
APPROVED	Ta Lin Pong 12.31.2010	PACKAGE CODE :			
APPROVED	Ta Lin Pong for 12.31.2010	DWG. NO.: PD-PQ15	REV.: B	DOC. NO.: PD-PQ15 REV.: B SHEET : 1	A3

Figure 6.6 48 QFN_7x7mm Mechanical Information Diagram



7 Abbreviations

In this chapter some of the terms and abbreviations used throughout the technical reference manual are listed as follows.

SIE	Serial Interface Engine
UTMI	USB Transceiver Macrocell Interface

About Alcor Micro, Corp.

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader…etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California. Alcor Micro is distinguished by its ability to provide innovative solutions for spec-driven products. Innovations like single chip solutions for traditional multiple chip products and on-board voltage regulators enable the company to provide cost-efficiency solutions for the computer peripheral device OEM customers worldwide.