Revision History

Revision	Date	Reason for redrawing	Page Update	Drawed	Checked	Approved
01A	0520Y16	Preliminary	--	Austin Lin		

Model: SM2258-G288_2P5_G152X16_DB

Silicon Motion, INC.

PageTitle	Cover Page
DOC.Number	<Doc>
Sch.FileName	SM2258G-AB-G288_2p5_G152X16_D2_DB_V01
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SATA PLUG 7P+15P CONNECTOR

CN1

SATA_PLUG_7P+15P

C1 10nF RX_P
C2 10nF RX_N
C3 10nF TX_N
C4 10nF TX_P

ZD1 Schottky_1SS389 VF=0.37V

VCCAH R30 33K
SATA_DEVSLP R19 0R DEVSLP_AIP
BC10 1nF
R97 NC_0R
DAS/DSS R5 NC_0R P10
H5V

GND DGND AGND

Crystal

XC1 8.2pF
Y1 XTAL-50MHz/2520
XC2 8.2pF
R2 1M
R1 0R
XIN XOUT
N1219A

JTAG Port

J1 NC_SIP_2x4_2.0mm
JTCK JTMS RSTIN VCCIO JTDI JTDO 3RST GND
C94 10uF

AIP

VCCAH R31 NC_33K EX_PWD#

VCCIO R33 1K DAS/DSS R57 NC_10K
D5 REDLED P10
VCCIO R34 1K
D3 REDLED P15

GPIO Definition

P00 R48 NC_10K VCCIO
P01 R50 10K VCCIO

JP2 NC_SIP-2P P11 HWP (1:normal/0:enable)
JP1 NC_SIP-2P P13 FORCE-ROM 0: ROM code mode
VCCFQ R180 0R P14 NAND Flash IO PG detect
JP3 NC_SIP-2P P15 Quick Erase for ISP (1:normal/0:enable)
P16 R51 NC_10K VCCIO
P17 R56 NC_10K VCCIO
P20 R20 NC_10K VCCIO

0:Legacy / 1:Toggle P23 R23 NC_10K VCCIO
SPI Load / 1: enable P24 R24 NC_10K VCCIO N1031A

JP4 with jumper 2P, 2.0mm
R46 10K P25 Reliable / 0: enable
N1103A

LED function

GND D6 NC_REDLED R9 NC_10K VCC5I

SM2256 / SM2258 Option circuit

V25_PAD V25_PAD
Near SM2256/SM2258 ball
C110 1uF 0603 1A
GND

Efuse_VQPS R166 0R GND SM2258 GND for general setting
SM2256: H6
SM2258: K8
R167 NC_0R V25_PAD SM2258 Efuse (VQPS) Vin
SM2256: D1,D2
SM2258: F3,F4

Setting For Boundary Scan Check

For SM2258 Only

0325Y15
VCCIO
TP10 TP11 TP12 T0 T1 T2 R70 R71 R72 NC_10K
TP13 P22 R32 NC_10K VCCIO
R22 set pg P22 voltage level

Voltage Detector

VCC5VI R25 5.1K VCC5I
ZD3 NC_Zener_BZT52C5V6S

Internal VDT for DDR I/O Power

1.5V VDTD_VIN R27 0R DRAM_1V5

Internal VDT for Flash Core Power

VDTF_VIN R26 0R VCCF

Controller SM2258-BGA288

IC1 SM2258-AB-BGA288

R22 240R_1%
R43 200R_1%
RESREF
VCCK
DDR_VREF
V11APAD
VCCAH
V25_PAD
DRAM_1V5

F_VREF
VCCFQ
VCCIO
DGND
AGND

RESET
VCCK VCCF
RR4 4.7K
RR10 4.7K
RR9 1K
Q101 2N9014
Q102
RR5 R0402_10K
BC41 0.47uF
R101 510K
RSTIN

H1 H2

R183 R185 R184 R182 R181 NC_10K R0402A
P04 P14 P05 P03 P02
R171 NC_10K P06

CH0

F0DQS_P F0DQS_N F0WEN F0ALE F0CLE F0REN_P F0REN_N F0D0 F0D1 F0D2 F0D3 F0D4 F0D5 F0D6 F0D7
F0CE0 F0CE1 F0CE2 F0CE3 F0CE4 F0CE5 F0CE6 F0CE7
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15

CH1

F1DQS_P F1DQS_N F1WEN F1ALE F1CLE F1REN_P F1REN_N F1D0 F1D1 F1D2 F1D3 F1D4 F1D5 F1D6 F1D7
F1CE0 F1CE1 F1CE2 F1CE3 F1CE4 F1CE5 F1CE6 F1CE7
BA_0 BA_1 BA_2 DDR_CLK_P DDR_CLK_N RAS# CAS# CS#_0 WE# RAM_RESET# CKE_0 ODT_0 DM_0 DM_1 DQS_P_0 DQS_N_0 DQS_P_1 DQS_N_1
ODT_1 CKE_1 CS#_1

CH2

F2DQS_P F2DQS_N F2WEN F2ALE F2CLE F2REN_P F2REN_N F2D0 F2D1 F2D2 F2D3 F2D4 F2D5 F2D6 F2D7
F2CE0 F2CE1 F2CE2 F2CE3 F2CE4 F2CE5 F2CE6 F2CE7

CH3

F3DQS_P F3DQS_N F3WEN F3ALE F3CLE F3REN_P F3REN_N F3D0 F3D1 F3D2 F3D3 F3D4 F3D5 F3D6 F3D7
F3CE0 F3CE1 F3CE2 F3CE3 F3CE4 F3CE5 F3CE6 F3CE7

FRB FWP F_VREF
P26 P27
EX_PWD#

H5V VCC5I VCCF VCCFQ VCCIO A3V3 VCCAH CRY_AVDD33 VCCK A1V1 V11APAD DRAM_1V5 DDR_VREF

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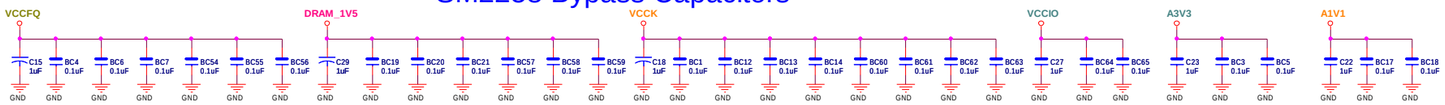
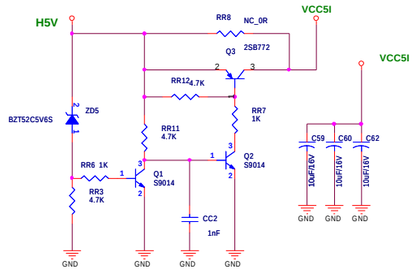
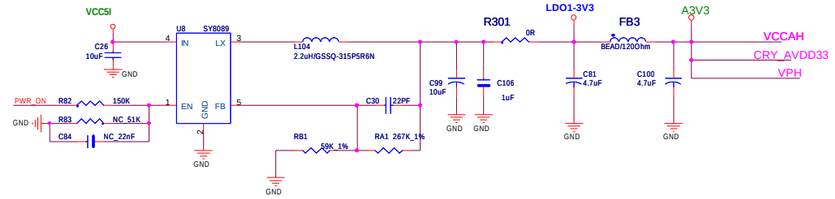
SM2258 Bypass Capacitors



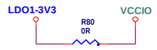
V18_PAD = SM2246 Internal 1.8V LDO Vout
A3V3= 3.0 / 3.3 / 3.6 (V) For AIP power
A1V2=VDDTX_PHY=VDDRX_PHY= 1.14 / 1.2 / 1.26 (V) For AIP power
VCCK = 1.2 (V) For SM2246AA core power
VCC = 3.3 / 1.8 (V) For General IO power
VCCF = 3.3 (V) For NAND flash Core Power
VCCFQ = 3.3 / 1.8 (V) For NAND flash IO Power
DRAM_1V5 = 1.5 / 1.8 (V) For DRAM Power

OVP Circuit

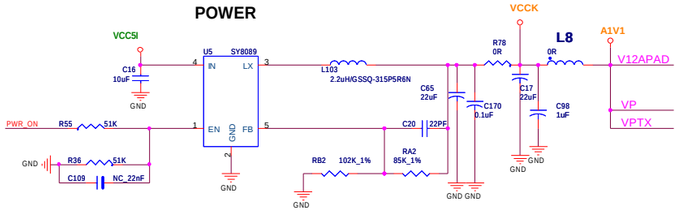




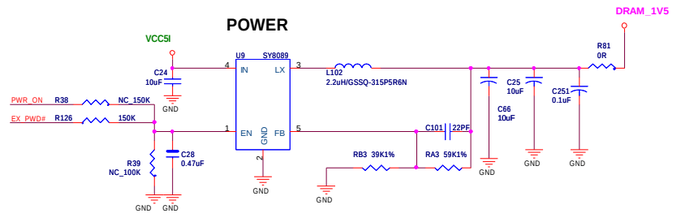
LDO_1: VCCIO Power 3.3V



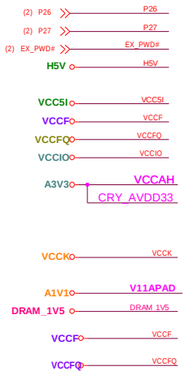
POWER



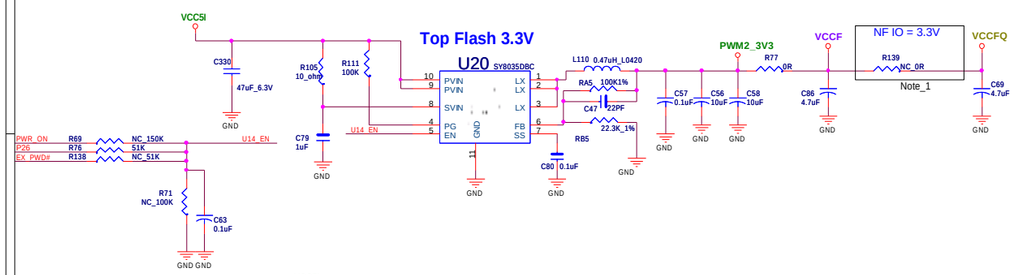
POWER

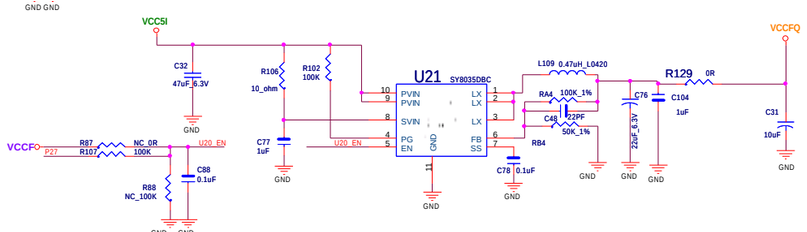


Vout = 0.6*(1+RA/RB)
Vout = 1.35V, RB3=47K ohm, 1%
Vout = 1.5V, RB3=39K ohm, 1%
Vout = 1.8V, RB3=29.4K ohm, 1%



Top Flash 3.3V





Silicon Motion, INC.	
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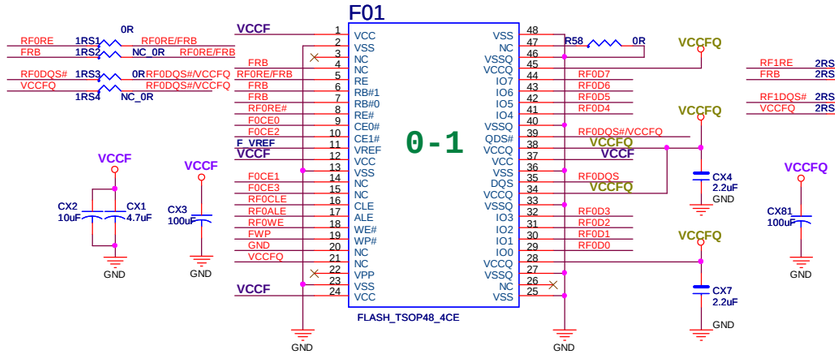
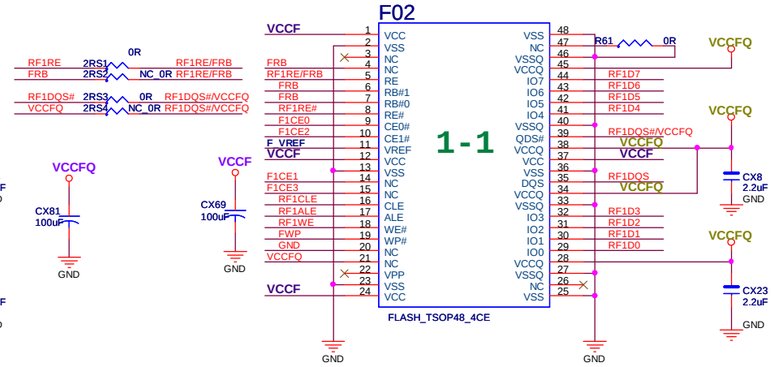
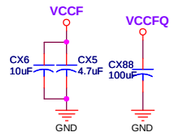
NAND Flash

Channel 0

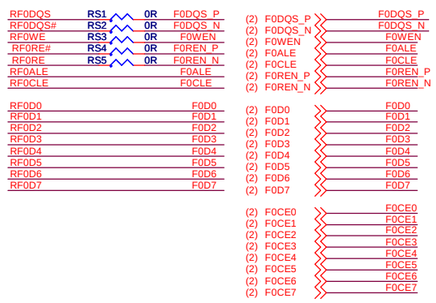




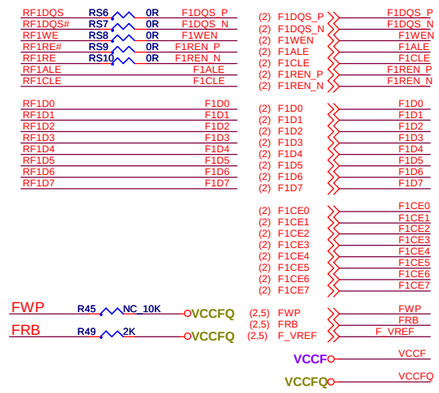


已批准
亿光速电子维修 17-05-23, 09:50

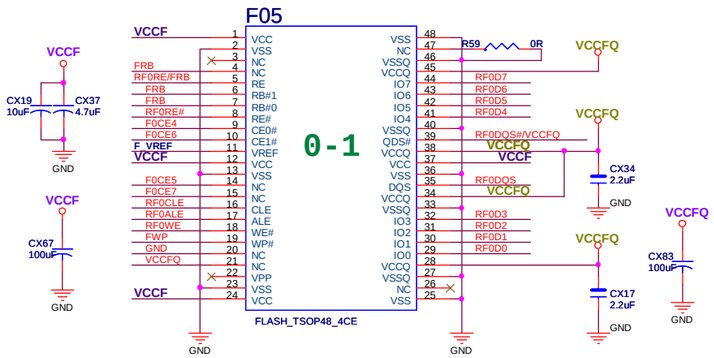
CH0

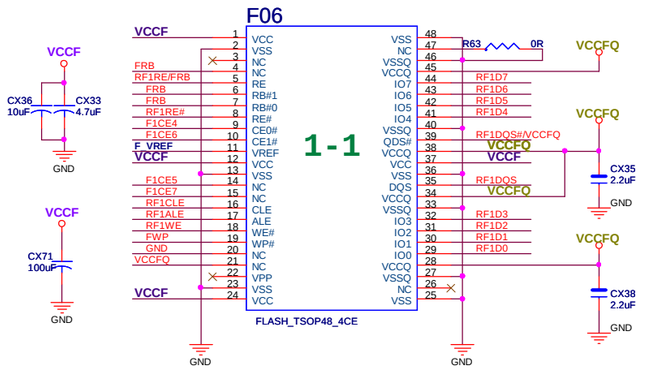


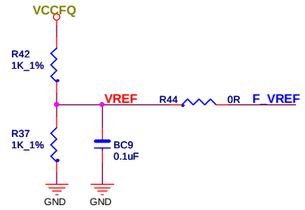
CH1



Channel 1







Silicon Motion, INC.	
PageTitle	NF_TSOPx8 (CH0, CH1)
DOC.Number	<Doc>
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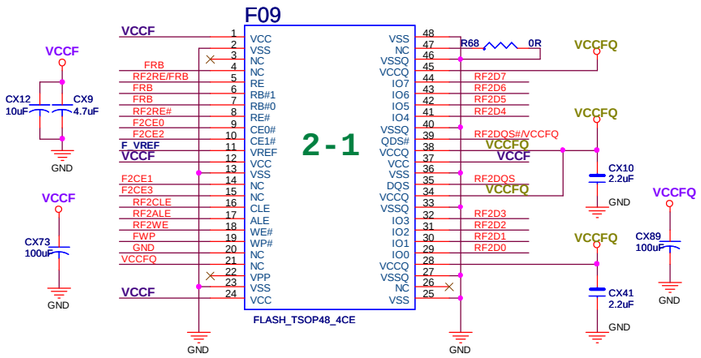
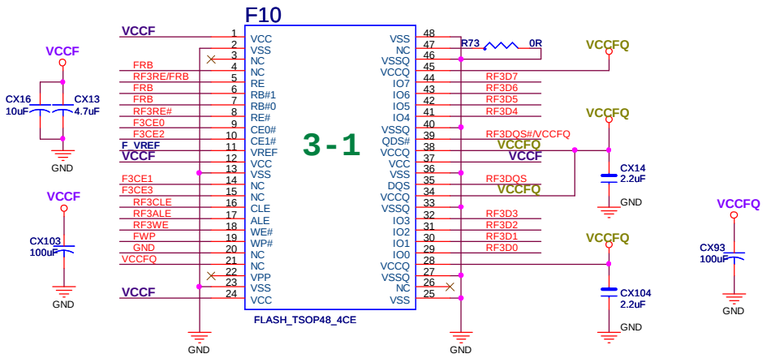
NAND Flash

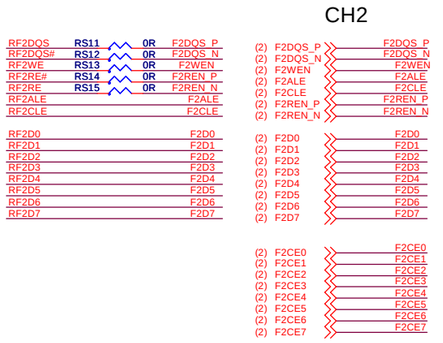
Channel 2



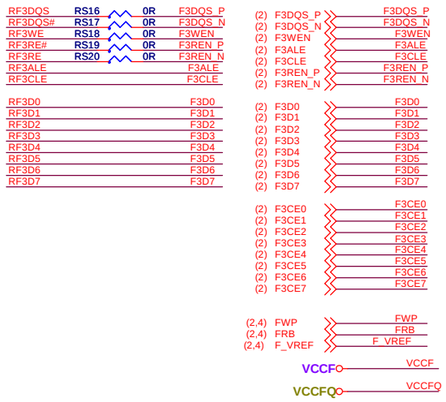
Channel 3



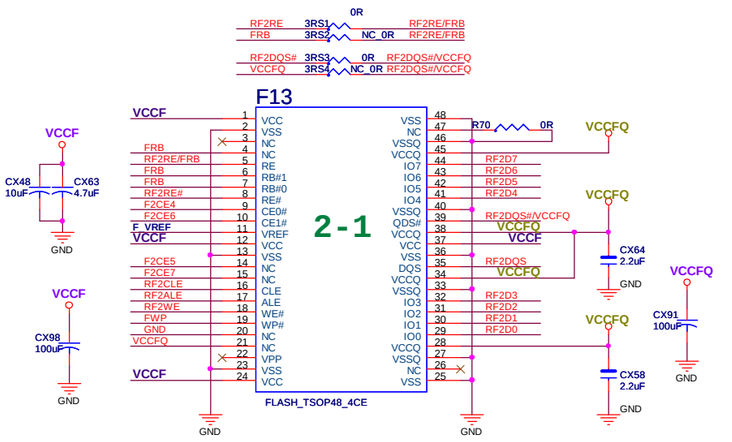
CH2



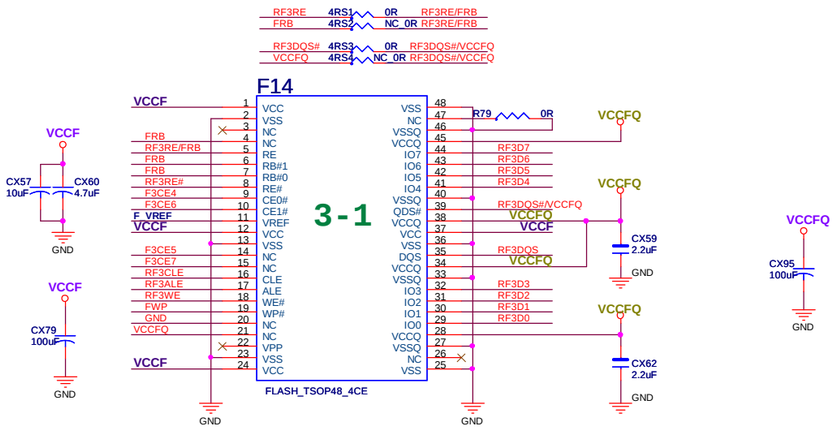
CH3



Channel 2



Channel 3



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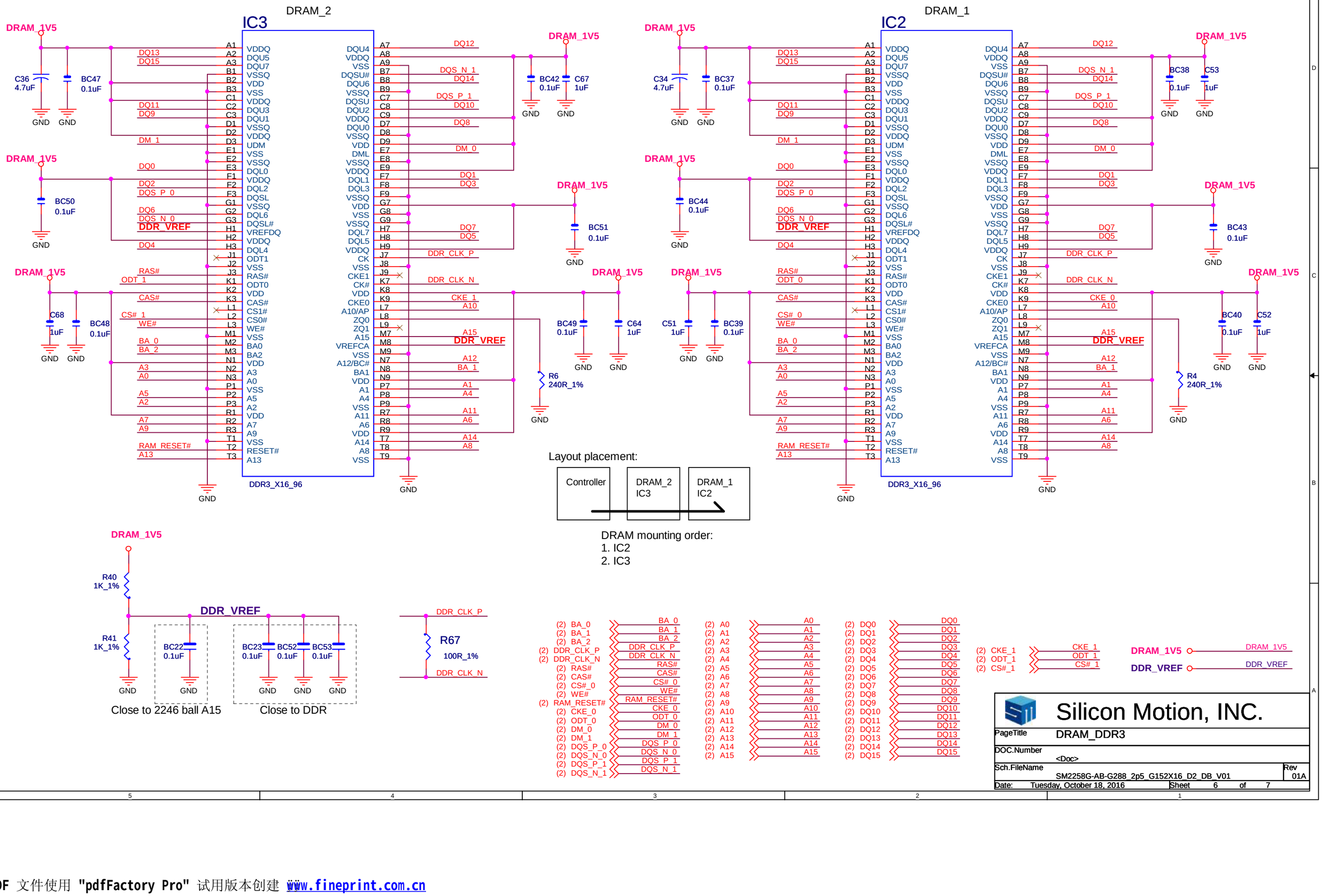
DRAM-DDR3



Layout placement:

DRAM mounting order:
1. IC2
2. IC3

Silicon Motion, INC.

PageTitle	DRAM_DDR3
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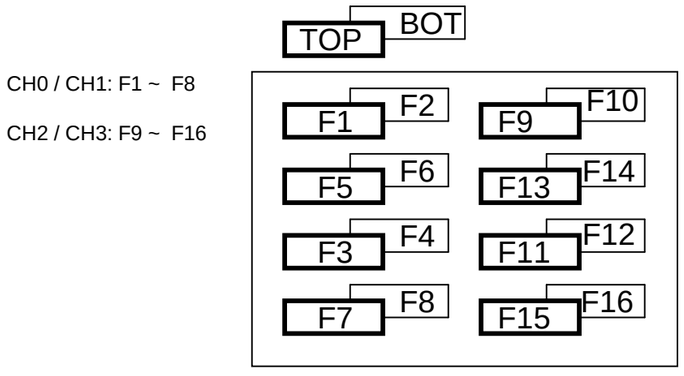
已修订

17-05-23, 09:52

TOP View For Flash PCB Placement



CH0 / CH1: F1 ~ F8

CH2 / CH3: F9 ~ F16

Silicon Motion, INC.

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