
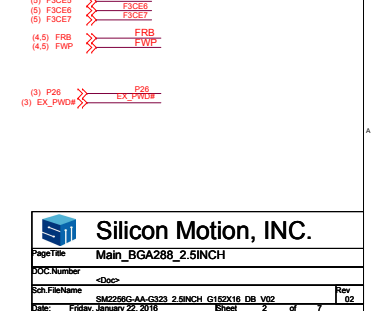
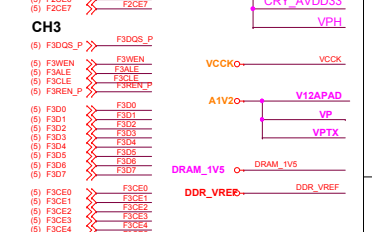
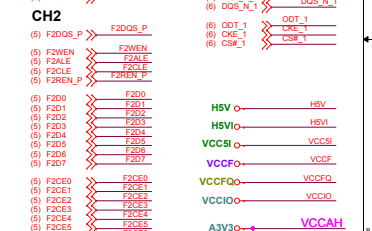
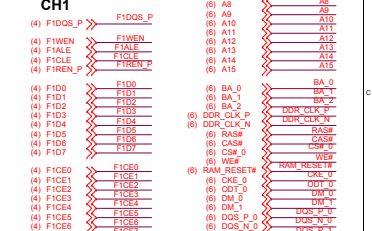
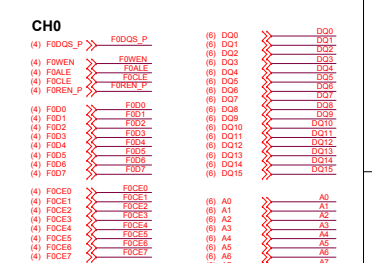
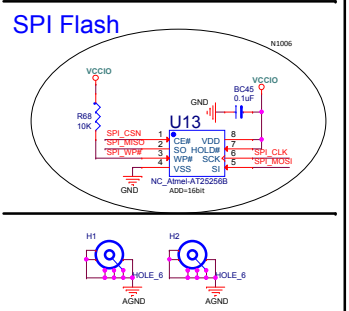
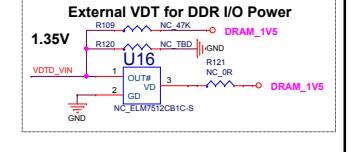
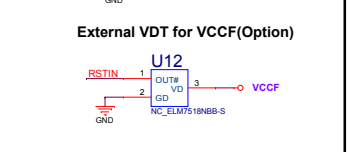
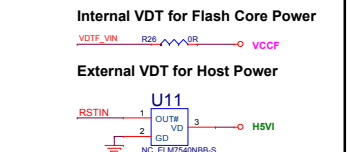
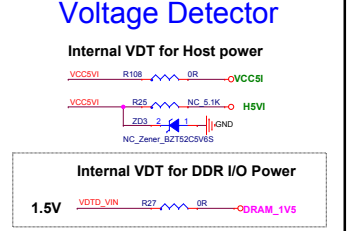
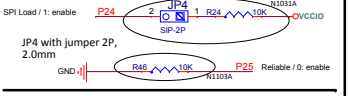
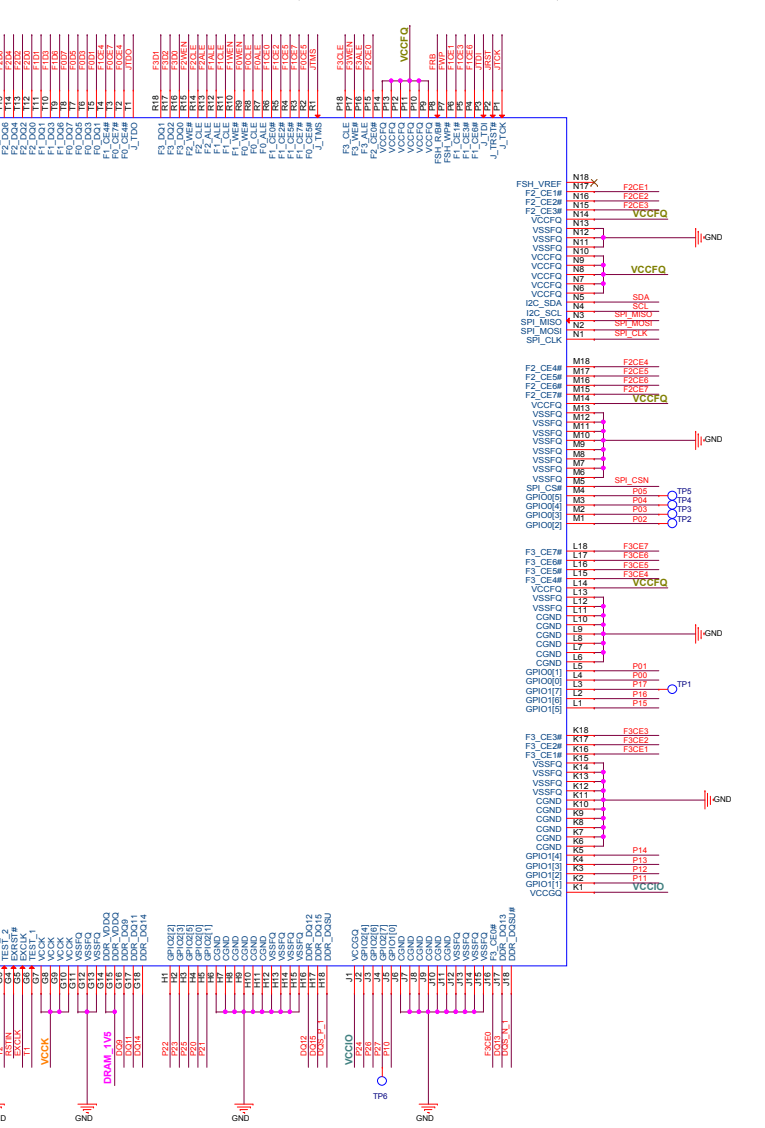
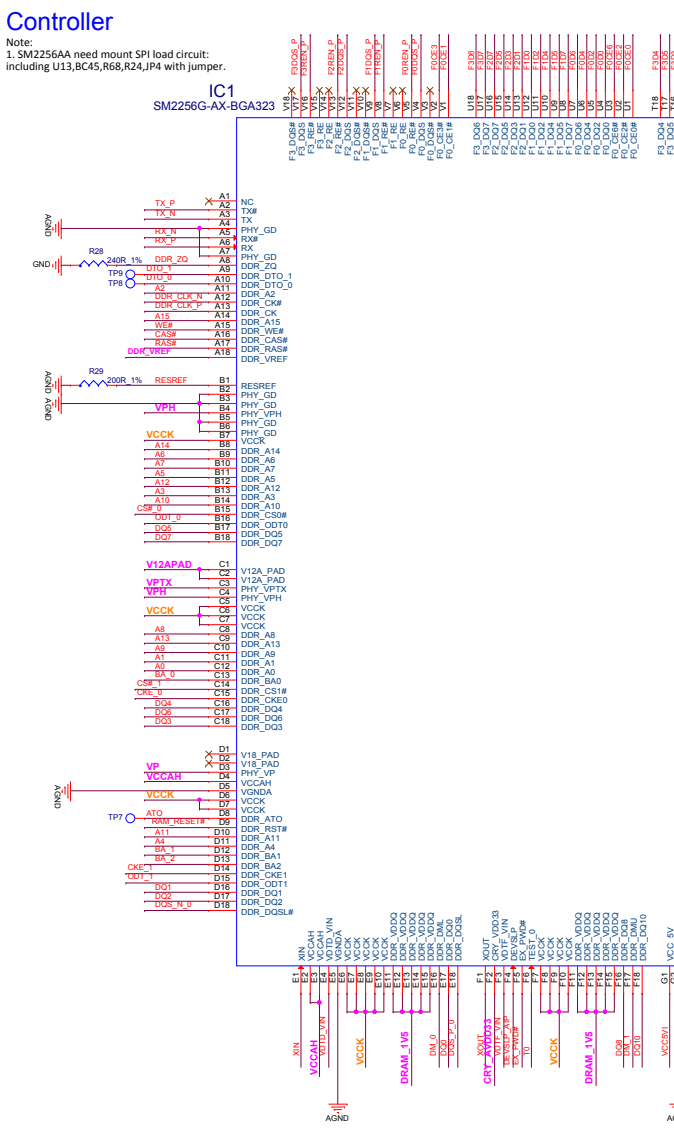
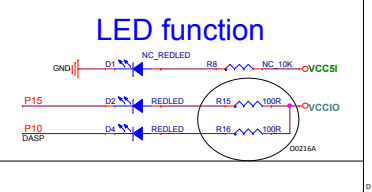
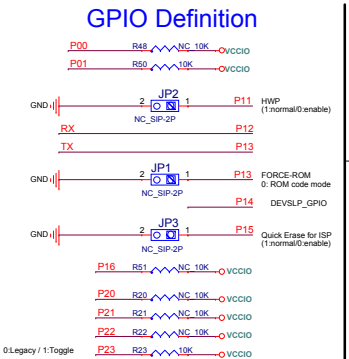
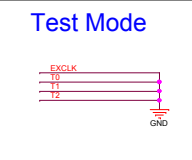
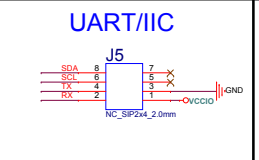
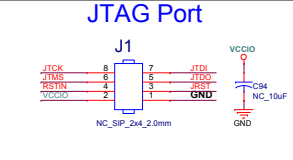
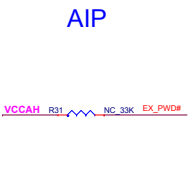
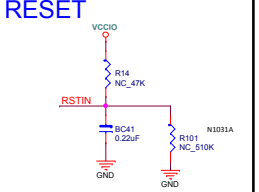
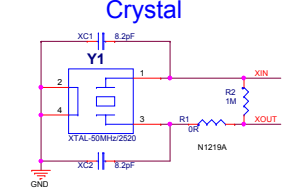
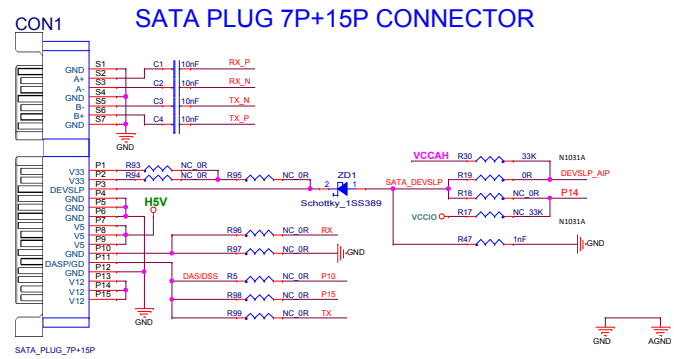


Revision History

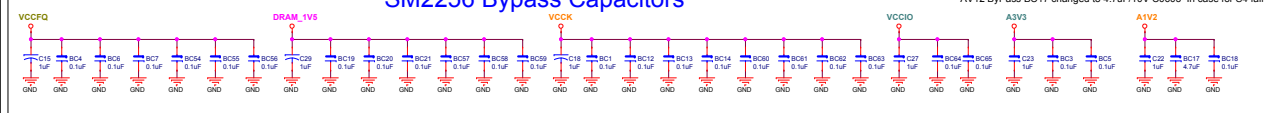
Revision	Date	Reason for redrawing	Page Update	Drawed	Checked	Approved
01	2014.06.13	Preliminary	--	Brian Lee	Austin Lin	Barry Chang
02	2014.09.12	First Time Release 1.For reduce power circuit, change U5 from SY8047 to SY8003L. And delete DEVSLP option circuit. 2.Confirm device sleep mode power circuit 2.1VCCCK equal to 0.98V, Turn off VCCF, VCCFQ and DRAM power at device sleep mode. 2.2 A3V3 and GPIO power doesn't turn off at device sleep mode	3	Austin Lin	Brian Lee	Barry Chang
02	2014.10.06	BOM modify. Add SPI EEROM circuit. Change below parts from NC to mounting. 1.U13 (25AA256-I/SN), R68 (10 ohm/0402), BC45 (0.1uF/0402)	2	Brian Lee	Austin Lin	Barry Chang
02	2014.10.31	1. Update BOM Sheet_1: FSH=16, SPI, BOM list with SPI EEPROM. (for enable SPI load) 1.1 Change R24 from NC to 10K ohm, 0402. 1.2 Change JP4 from NC to SIP, 2P, 2.0mm with jumper (2P, 2.0mm) 2. 2 sheet BOM update. 2.1 Change R15,R16 from 10K ohm, 0402 to 2K ohm, 0402. 2.2 Change R30 from 10K ohm, 0402 to 33K ohm, 0402. 2.3 Change R101 from NC to 510K ohm, 0402	2	Brian Lee	Austin Lin	Barry Chang
02	2014.11.03	BOM modify. For enable NAND reliable mode setting. Change R46 from NC to 10K ohm, 0402.	2	Brian Lee	Austin Lin	Barry Chang
02	2014.12.01	1. For Samsung TLC 19nm (ID: EC,3C,E9,DE,88,C5): setting VCCF=VCCFQ=3.0V (RA4=240K, 0402, 1%) 2. Modify power control circuit: 2.1 Change U22 from VDT 4V to NC 2.2 Change R127 from NC to 0 ohm, 0402.	3	Brian Lee	Austin Lin	Barry Chang
02	2014.12.19	1.Modify power circuit BOM for cost down. Change SD1 from SCHOTTKY_SS2040/2A to resistor 0 ohm/1206. 2.For fine tune crystal signal quality, modify R1 from resistor 100 ohm_1%/0402 to 0 ohm/0402.	3	Brian Lee	Austin Lin	Barry Chang
02	2015.02.02	1.Modify power circuit BOM. 1.1 Change U22 from 4V VDT to 3V VDT. 1.2 Change R127 from OR to NC. 1.3 Change R52 from 5.49K 1% to 3.65K 1%. I_limit increase from 2A to 3A.	3	Brian Lee	Austin Lin	Barry Chang
02	2015.02.16	For SM2256-AB BOM 1.Adjust LED brightness Change R15,R16 resistor value from 2K ohm to 100 ohm (0402) 2.Change GPIO VCC voltage from 3.3V to 1.8V 2.1 Change U21 from NC to LDO ELM88181BAS(SOT-23) 2.2 Change R80 from resistor 0 ohm to NC.(0603) 3.SPI EEROM circuit remove BOM option.	2,3	Brian Lee	Austin Lin	Barry Chang
02	2015.05.04	1. Modify power control circuit BOM, for FW control NAND data protection flow, 1.1 Change U22 from VDT 3V to NC 1.2 Change R127 from NC to 0 ohm, 0402.	2	Brian Lee	Austin Lin	Barry Chang

Page1	Cover_Page
Page2	Controller_BGA323_2.5INCH
Page3	Power_Host_5V
Page4	NF_BGA152x8 (CH0, CH1)
Page5	NF_BGA152x8 (CH2, CH3)
Page6	DRAM_DDR3-16x2
Page7	Flash Mounting Guide

 Silicon Motion, INC.	
PageTitle	Cover Page
DOC.Number	<Doc>
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Date:	Friday, January 22, 2016
Sheet	1 of 7
Rev	02

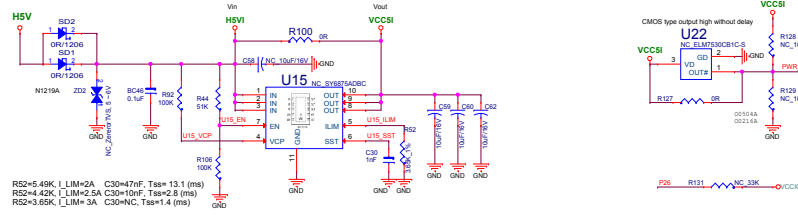


SM2256 Bypass Capacitors



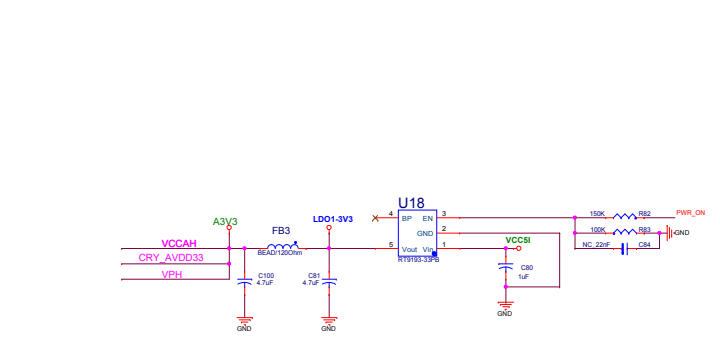
V18_PAD = SM2246 Internal 1.8V LDO Vout
 A3V3= 3.0 / 3.3 / 3.6 (V) For AIP power
 A1V2=VDDTX_PHY=VDDR_X_PHY= 1.14 / 1.2 / 1.26 (V) For AIP power
 VCCCK = 1.2 (V) For SM2246AA core power
 VCC = 3.3 / 1.8 (V) For General IO power
 VCCFQ = 3.3 (V) For NAND flash Core Power
 VCCFQ = 3.3 / 1.8 (V) For NAND flash IO Power
 DRAM_1V5 = 1.5 / 1.8 (V) For DRAM Power

OVP Circuit

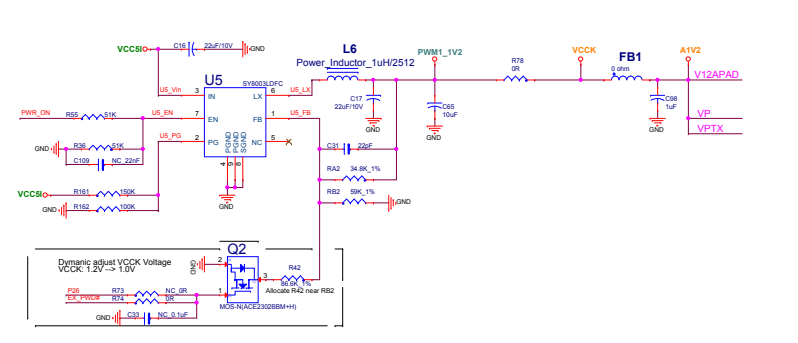


R52=5.49K, L_LIM=2A, C30=47nF, Tss= 13.1 (ms)
 R52=4.42K, L_LIM=2.5A, C30=10nF, Tss=2.8 (ms)
 R52=3.65K, L_LIM=3A, C30=NC, Tss=1.4 (ms)

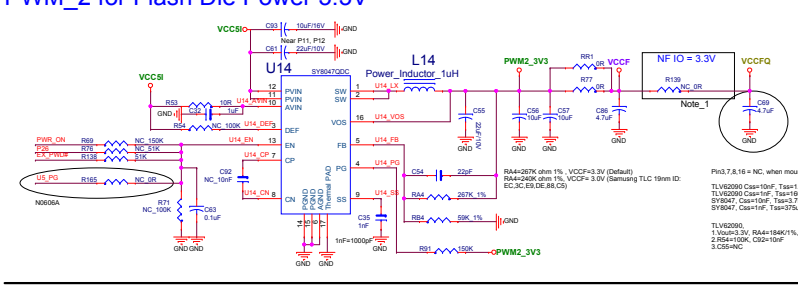
LDO_1: Analog Power 3.3V



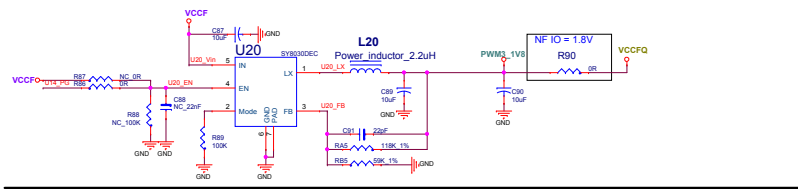
PWM_1 for VCCCK/A1V2 1.2V



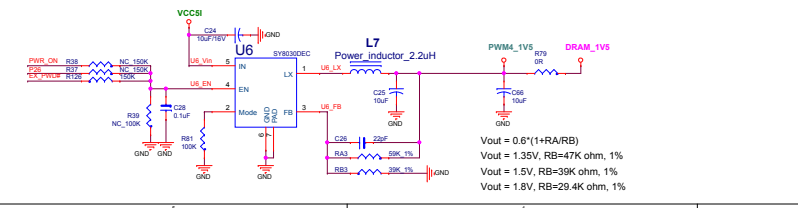
PWM_2 for Flash Die Power 3.3V



PWM_3 for Flash I/O Power 1.8V



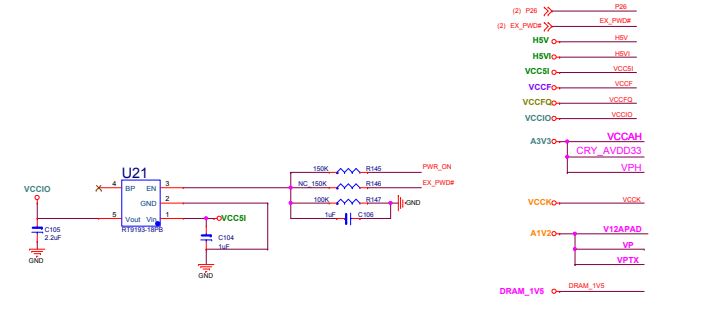
PWM_4 for DRAM-DDR3 Power 1.5V



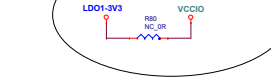
Vout = 0.6*(1+RA/RB)
 Vout = 1.35V, RB=47K ohm, 1%
 Vout = 1.5V, RB=39K ohm, 1%
 Vout = 1.8V, RB=29.4K ohm, 1%

LDO_2: VCCIO Power

LDO_2: VCCIO Power 1.8V



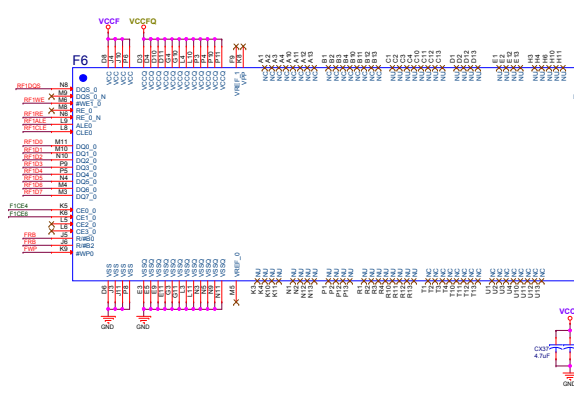
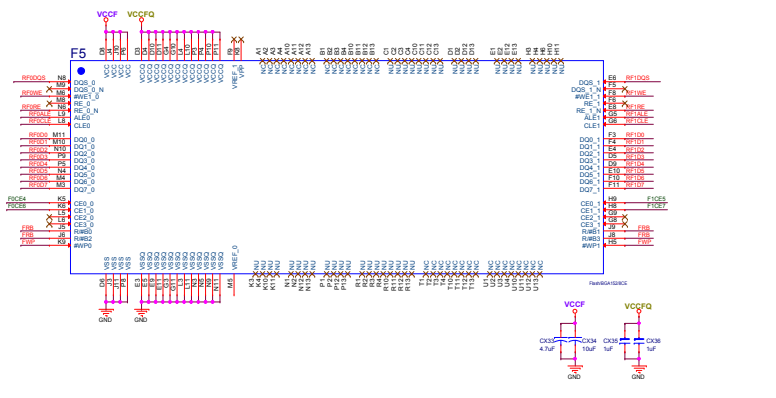
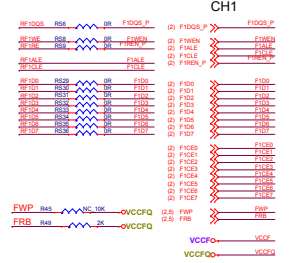
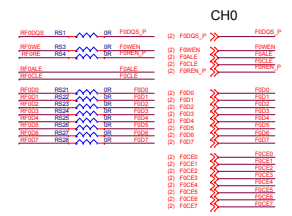
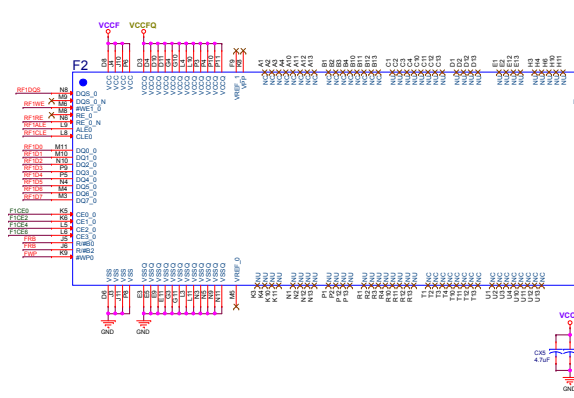
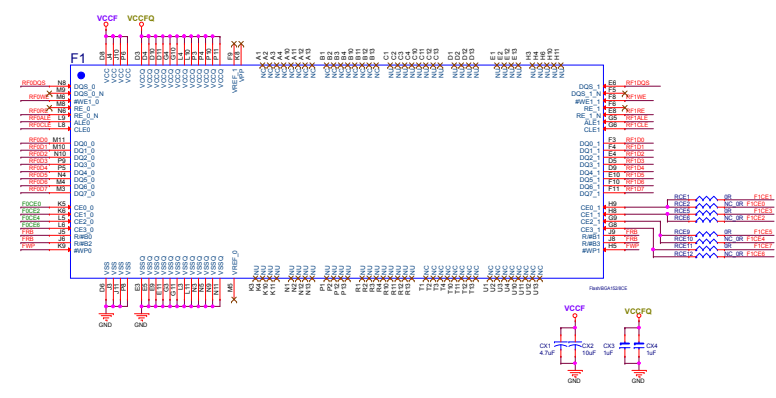
LDO_1: VCCIO Power 3.3V



- (2) PWR_0
- (2) EX_PWR0
- HSV_0
- HSV0L
- VCCSI_0
- VCCFQ_0
- VCCFQ_0
- VCCIO_0
- VCCAH
- CRY_AVDD33
- VPH
- VCCCK_0
- V12APAD
- VP
- VPTX
- DRAM_1V5_0
- DRAM_1V5

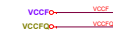
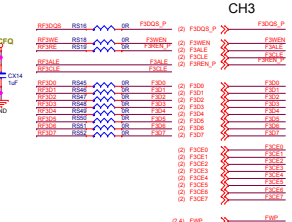
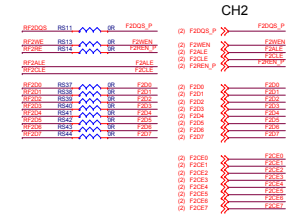
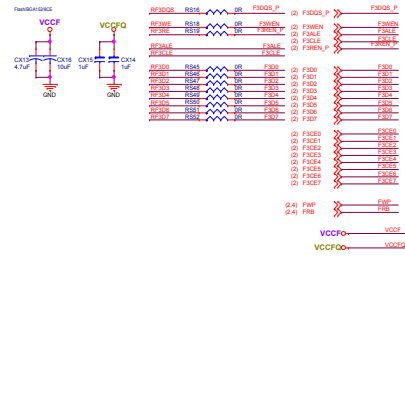
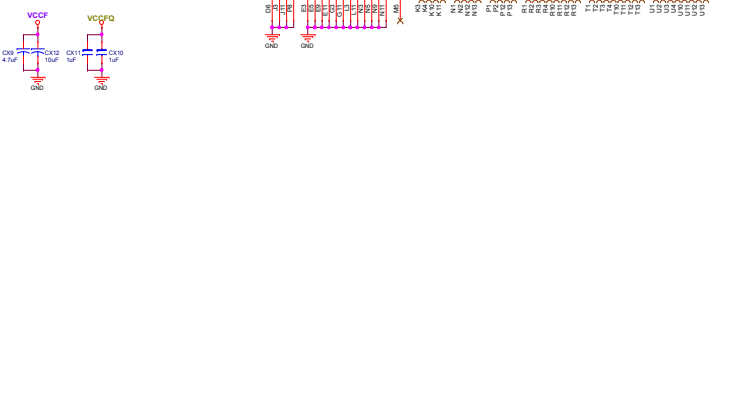
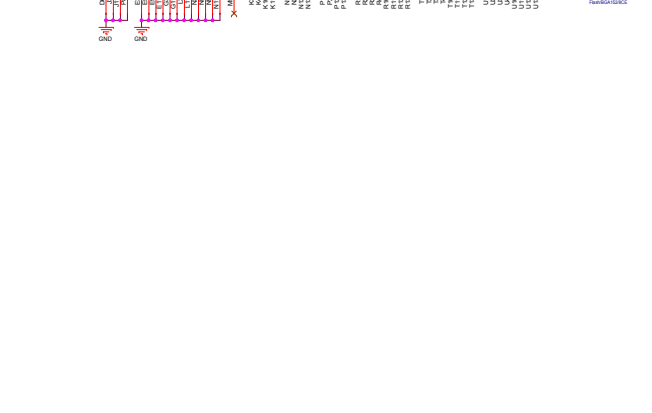
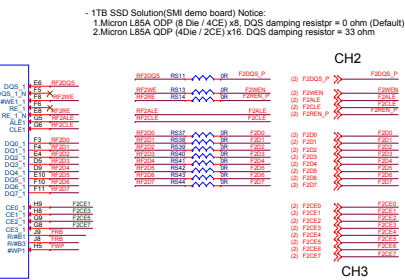
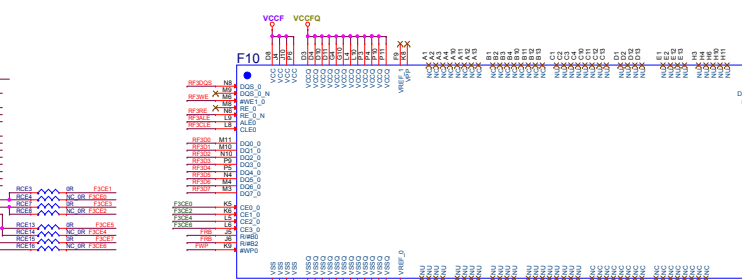
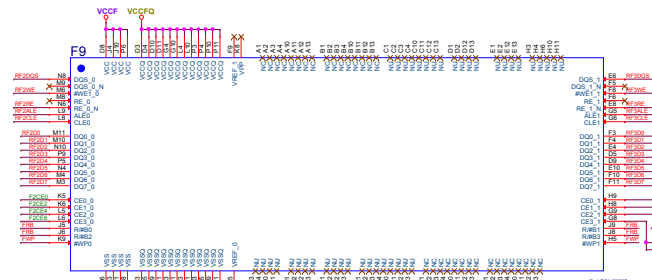
Channel 0 & 1

- 1TB SSD Solution(SMI demo board) Notice:
 1.Micron 185A GDP (8 Die / ACE) x8. DQS damping resistor = 0 ohm (Default)
 2.Micron L85A GDP (4Die / 2CE) x16. DQS damping resistor = 33 ohm

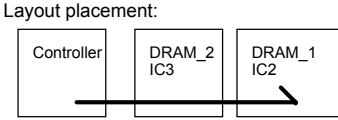
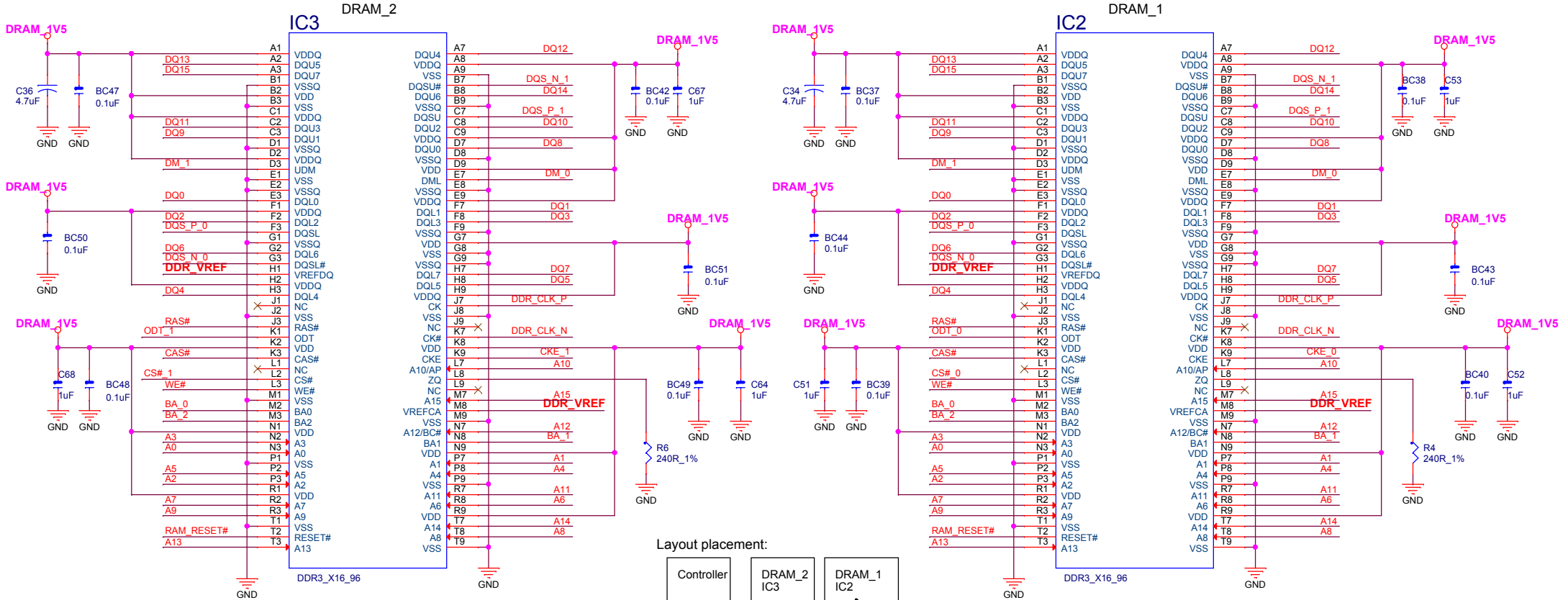


Channel 2 & 3

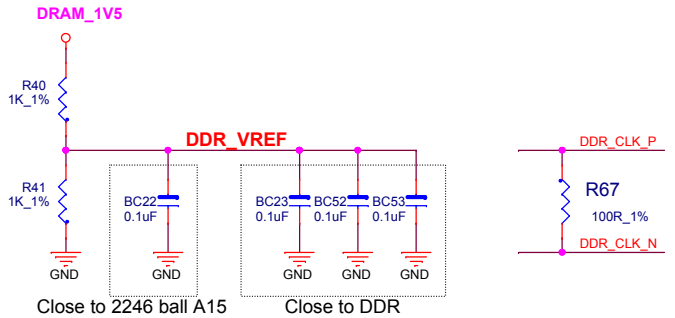
- 1TB SSD Solution(SM demo board) Notice
 1.Micron L85A GDP (8 Die / 4CE) x8. DQS damping resistor = 0 ohm (Default)
 2.Micron L85A GDP (4Die / 2CE) x16. DQS damping resistor = 33 ohm



DRAM-DDR3



DRAM mounting order:
 1. IC2
 2. IC3



(2) BA_0	>>>	BA_0	(2) A0	>>>	A0	(2) DQ0	>>>	DQ0	(2) CKE_1	>>>	CKE_1	DRAM_1V5
(2) BA_1	>>>	BA_1	(2) A1	>>>	A1	(2) DQ1	>>>	DQ1	(2) ODT_1	>>>	ODT_1	DRAM_1V5
(2) BA_2	>>>	BA_2	(2) A2	>>>	A2	(2) DQ2	>>>	DQ2	(2) CS#_1	>>>	CS#_1	DRAM_1V5
(2) DDR_CLK_P	>>>	DDR_CLK_P	(2) A3	>>>	A3	(2) DQ3	>>>	DQ3				
(2) DDR_CLK_N	>>>	DDR_CLK_N	(2) A4	>>>	A4	(2) DQ4	>>>	DQ4				
(2) RAS#	>>>	RAS#	(2) A5	>>>	A5	(2) DQ5	>>>	DQ5				
(2) CAS#_0	>>>	CAS#_0	(2) A6	>>>	A6	(2) DQ6	>>>	DQ6				
(2) CS#_0	>>>	CS#_0	(2) A7	>>>	A7	(2) DQ7	>>>	DQ7				
(2) WE#	>>>	WE#	(2) A8	>>>	A8	(2) DQ8	>>>	DQ8				
(2) RAM_RESET#	>>>	RAM_RESET#	(2) A9	>>>	A9	(2) DQ9	>>>	DQ9				
(2) CKE_0	>>>	CKE_0	(2) A10	>>>	A10	(2) DQ10	>>>	DQ10				
(2) ODT_0	>>>	ODT_0	(2) A11	>>>	A11	(2) DQ11	>>>	DQ11				
(2) DM_0	>>>	DM_0	(2) A12	>>>	A12	(2) DQ12	>>>	DQ12				
(2) DM_1	>>>	DM_1	(2) A13	>>>	A13	(2) DQ13	>>>	DQ13				
(2) DQS_P_0	>>>	DQS_P_0	(2) A14	>>>	A14	(2) DQ14	>>>	DQ14				
(2) DQS_N_0	>>>	DQS_N_0	(2) A15	>>>	A15	(2) DQ15	>>>	DQ15				
(2) DQS_P_1	>>>	DQS_P_1										
(2) DQS_N_1	>>>	DQS_N_1										

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PageTitle: DRAM_DDR3

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Sch.FileName: SM2256G-AA-G323_2.5INCH_G152X16_DB_V02

Date: Friday, January 22, 2016

Rev: 02
Sheet: 6 of 7

NAND FLASH Mounting Guide

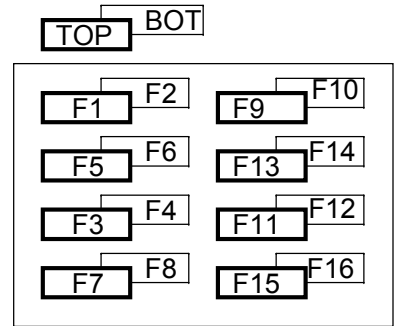
2.5INCH BGA152x16 NAND Flash Mounting Guide

NAND Flash ID	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	NF Config.	RCE1	RCE2	RCE3	RCE4	RCE5	RCE6	RCE7	RCE8	RCE9	RCE10	RCE11	RCE12	RCE13	RCE14	RCE15	RCE16	CE usage
Single CE flash x1	⊗	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1CH/1CE	△	△	△	△	△	△	△	△	△	△	△	△	△	△	△	△	CE0
Single CE flash x2	⊗	⊗	X	X	X	X	X	X	X	X	X	X	X	X	X	X	2CH/1CE	△	△	△	△	△	△	△	△	△	△	△	△	△	△	△	△	CE0
Single CE flash x3	⊗	⊗	X	X	X	X	X	X	X	X	X	X	X	X	X	X	3CH/1CE	△	△	△	△	△	△	△	△	△	△	△	△	△	△	△	△	CE0
Single CE flash x4	⊗	⊗	X	X	X	X	X	X	X	X	X	X	X	X	X	X	4CH/1CE	△	△	△	△	△	△	△	△	△	△	△	△	△	△	△	△	CE0
Single CE flash x8	⊗	⊗	X	X	X	X	X	X	X	X	X	X	X	X	X	X	4CH/2CE	△	△	△	△	△	△	△	△	△	△	△	△	△	△	△	△	CE0, CE4
Single CE flash x16	⊗	⊗	⊗	⊗	⊗	⊗	⊗	⊗	⊗	⊗	⊗	⊗	⊗	⊗	⊗	⊗	4CH/4CE	△	△	△	△	△	△	△	△	△	△	△	△	△	△	△	△	CE0, CE2, CE4, CE6
Dual CE flash x1	⊗	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	2CH/1CE	X	⊗	△	△	△	△	△	△	△	△	△	△	△	△	△	△	CE0
Dual CE flash x2	⊗	⊗	X	X	X	X	X	X	X	X	X	X	X	X	X	X	2CH/2CE	⊗	X	△	△	△	△	△	△	△	△	△	△	△	△	△	△	CE0, CE1
Dual CE flash x2	⊗	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	4CH/1CE	X	⊗	X	⊗	△	△	△	△	△	△	△	△	△	△	△	△	CE0
Dual CE flash x4	⊗	⊗	X	X	X	X	X	X	X	X	X	X	X	X	X	X	4CH/2CE	⊗	X	⊗	X	△	△	△	△	△	△	△	△	△	△	△	△	CE0, CE1
Dual CE flash x8	⊗	⊗	X	X	⊗	⊗	X	X	⊗	⊗	X	X	⊗	⊗	X	X	4CH/4CE	⊗	X	⊗	X	△	△	△	△	△	△	△	△	△	△	△	△	CE0, CE1, CE4, CE5
Dual CE flash x16	⊗	⊗	⊗	⊗	⊗	⊗	⊗	⊗	⊗	⊗	⊗	⊗	⊗	⊗	⊗	⊗	4CH/8CE	⊗	X	⊗	X	△	△	△	△	△	△	△	△	△	△	△	△	CE0, CE1, CE2, CE3 CE4, CE5, CE6, CE7
Quad CE flash x1	⊗	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	2CH/2CE	X	⊗	△	△	X	⊗	△	△	△	△	△	△	△	△	△	△	CE0, CE2
Quad CE flash x2	⊗	⊗	X	X	X	X	X	X	X	X	X	X	X	X	X	X	2CH/4CE	⊗	X	△	△	⊗	X	△	△	△	△	△	△	△	△	△	△	CE0, CE1, CE2, CE3
Quad CE flash x2	⊗	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	4CH/2CE	X	⊗	X	⊗	X	⊗	X	⊗	△	△	△	△	△	△	△	△	CE0, CE2
Quad CE flash x4	⊗	⊗	X	X	X	X	X	X	X	X	X	X	X	X	X	X	4CH/4CE	⊗	X	⊗	X	⊗	X	⊗	X	△	△	△	△	△	△	△	△	CE0, CE1, CE2, CE3
Quad CE flash x8	⊗	⊗	X	X	⊗	⊗	X	X	⊗	⊗	X	X	⊗	⊗	X	X	4CH/8CE	⊗	X	⊗	X	⊗	X	⊗	X	△	△	△	△	△	△	△	△	CE0, CE1, CE2, CE3 CE4, CE5, CE6, CE7
8 CE flash x1	⊗	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	2CH/4CE	X	⊗	X	⊗	X	⊗	X	⊗	△	△	△	△	△	△	△	△	CE0, CE2, CE4, CE6
8 CE flash x2	⊗	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	4CH/4CE	X	⊗	X	⊗	X	⊗	X	⊗	X	⊗	X	⊗	X	⊗	X	⊗	CE0, CE2, CE4, CE6
8 CE flash x4	⊗	⊗	X	X	X	X	X	X	⊗	⊗	X	X	X	X	X	X	4CH/8CE	⊗	X	⊗	X	⊗	X	⊗	X	⊗	X	⊗	X	⊗	X	⊗	X	CE0, CE1, CE2, CE3 CE4, CE5, CE6, CE7

M1023A

⊗	Install
X	un-install
△	Don't care (it is fine if resistor mousing or not.)

TOP View For Flash PCB Placement



CH0 / CH1: F1 ~ F8
CH2 / CH3: F9 ~ F16