SF-2000
Solid State Drive Processor

Hardware Reference Manual

Revision 1.03

PRELIMINARY INFORMATION – Subject to Change

May 2011

Revision History

Document		Description of Changes Since Last Revision
Version	Date	
1.00	10/28/2010	Initial release of document.
1.01	11/05/2010	Assorted formatting edits.
1.02	2/3/2011	Updated the following tables and figures: • Table 2-2: 400-Ball TBGA Thermal Design Parameters • Table 2-4: 256-Ball TBGA Thermal Design Parameters • Table 3-2: 400-Ball TBGA Power and Ground Balls • Table 3-3: 256-Ball TBGA Power and Ground Balls • Table 3-1: Ball List • Figure 3-3: 400-Ball TBGA Ball Assignments (3) • Table 4-1: Power Supply Operating Conditions • Table 5-6: PFAIL and DATA_HARDENED Timing Added Section 3.2 – No Connect Pins. Modified Section 6.3 – Flash Memory Connectivity Assorted formatting edits.
1.03	5/19/2011	New information on the BGA ball diameter and materials

Legal Information

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1 Document Overview

This Hardware Reference Manual (HRM) is for use by system architects and engineers to assist with the hardware electrical design of SF-2000 SSD processor family devices into systems.

1.1 Related Documents

- SF-2000 Software Reference Manual (SRM)
- SF-2000 PCB Design Guide
- SF-25xx SF-26xx Power Fail Calculator

2 Mechanical and Thermal Package Parameters

The SF-2000 processor family is available in two package options:

- 400-Ball TBGA
  - Supports up to 16 flash sites.
- 256-Ball TBGA
  - Supports up to 8 flash sites.

2.1 400-Ball TBGA Mechanical and Thermal Parameters

2.1.1 400-Ball TBGA Mechanical Description

Table 2-1 provides the 400-ball TBGA package dimensions.

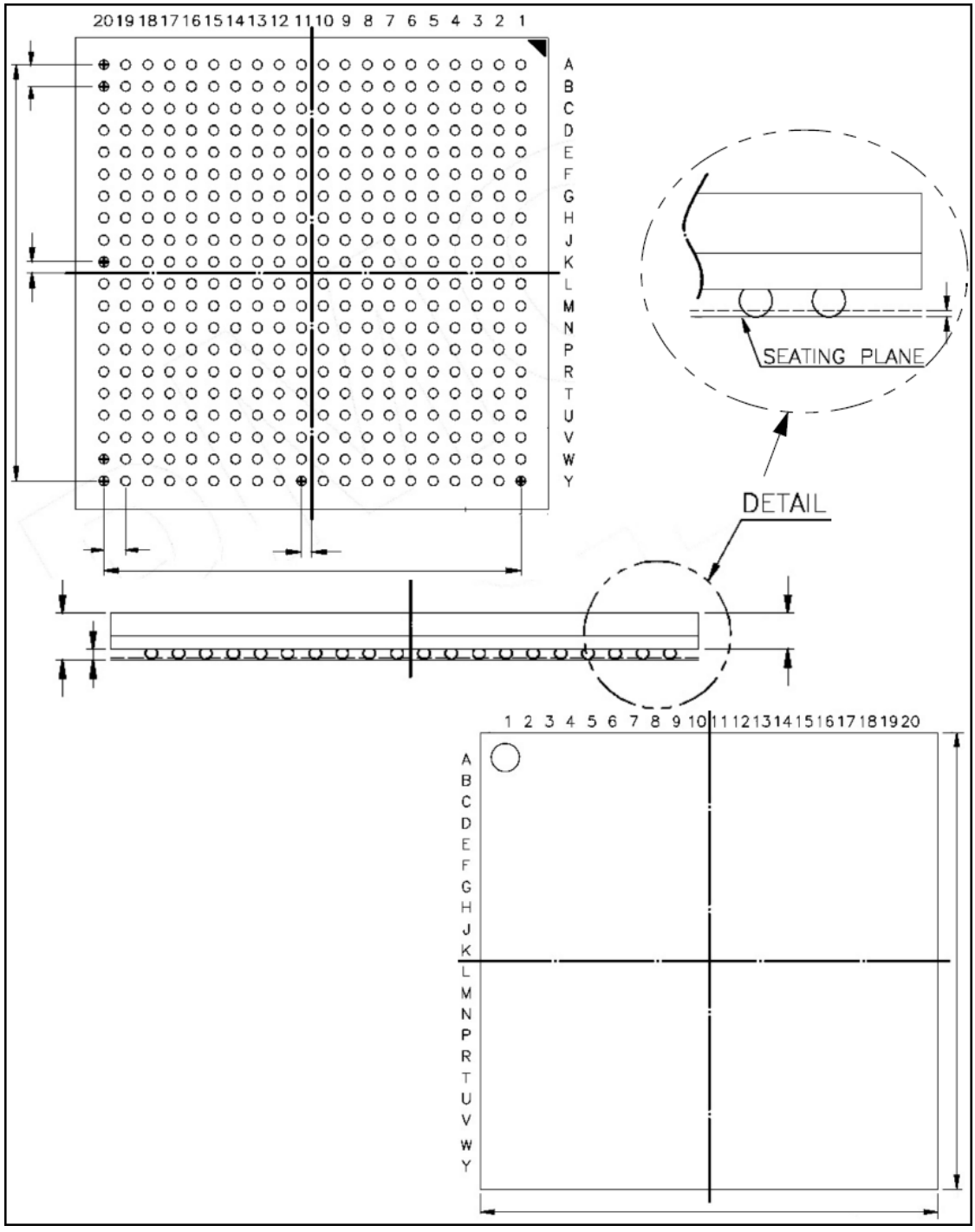
Table 2-1: 400-Ball TBGA Package Dimensions

Feature	Min	Nom	Max	Units
Overall Height (Including Ball Stand-Off)	--	--	1.20	mm
Ball Array Pattern		20 x 20		balls
Pad Diameter	--	0.325	-	mm
Ball Pitch	--	0.650	--	mm
Ball Width	--	0.30	--	mm
Ball SRO	--	0.25	--	mm
Ball Height (Stand-Off)	0.20	0.25	0.30	mm
Side Dimension	13.90	14.00	14.10	mm
Ball Matrix Side Dimension (Ball Center to Ball Center)	--	12.350	--	mm

2.1.2 400-Ball TBGA Mechanical Drawing

Figure 2-1 provides the 400-ball package drawing.

Figure 2-1: 400-Ball TBGA Package Drawing



2.1.3 400-Ball TBGA Thermal Specification

Table 2-2 provides the 400-ball TBGA thermal design parameters.

Table 2-2: 400-Ball TBGA Thermal Design Parameters

Parameter	Value	Units
$T_{J\text{-}MAX}$ - Maximum Junction Temperature	115	°C
Θ_{JC} - Junction to Case Thermal Resistance	5.8	°C/W

2.1.4 400-Ball TBGA Ball Material Specification

Table 2-3 provides the materials and finish for the 400-ball TBGA package

Table 2-3: 400-Ball TBGA Materials Specification

Item	Value
Solder Ball Material	M705 / SAC305 (96.5Sn2Ag0.5Cu)
Substrate Solder Mask	Taiyo PSR4000 AUS 308
Surface Finish	COPPER: Min. 15um NICKEL: Min. 5um GOLD: Min. 0.3um
Flux Type	Qualitek PF-708

2.2 256-Ball TBGA Mechanical and Thermal Parameters

2.2.1 256-Ball TBGA Mechanical Description

Table 2-4 provides the 256-ball TBGA package dimensions.

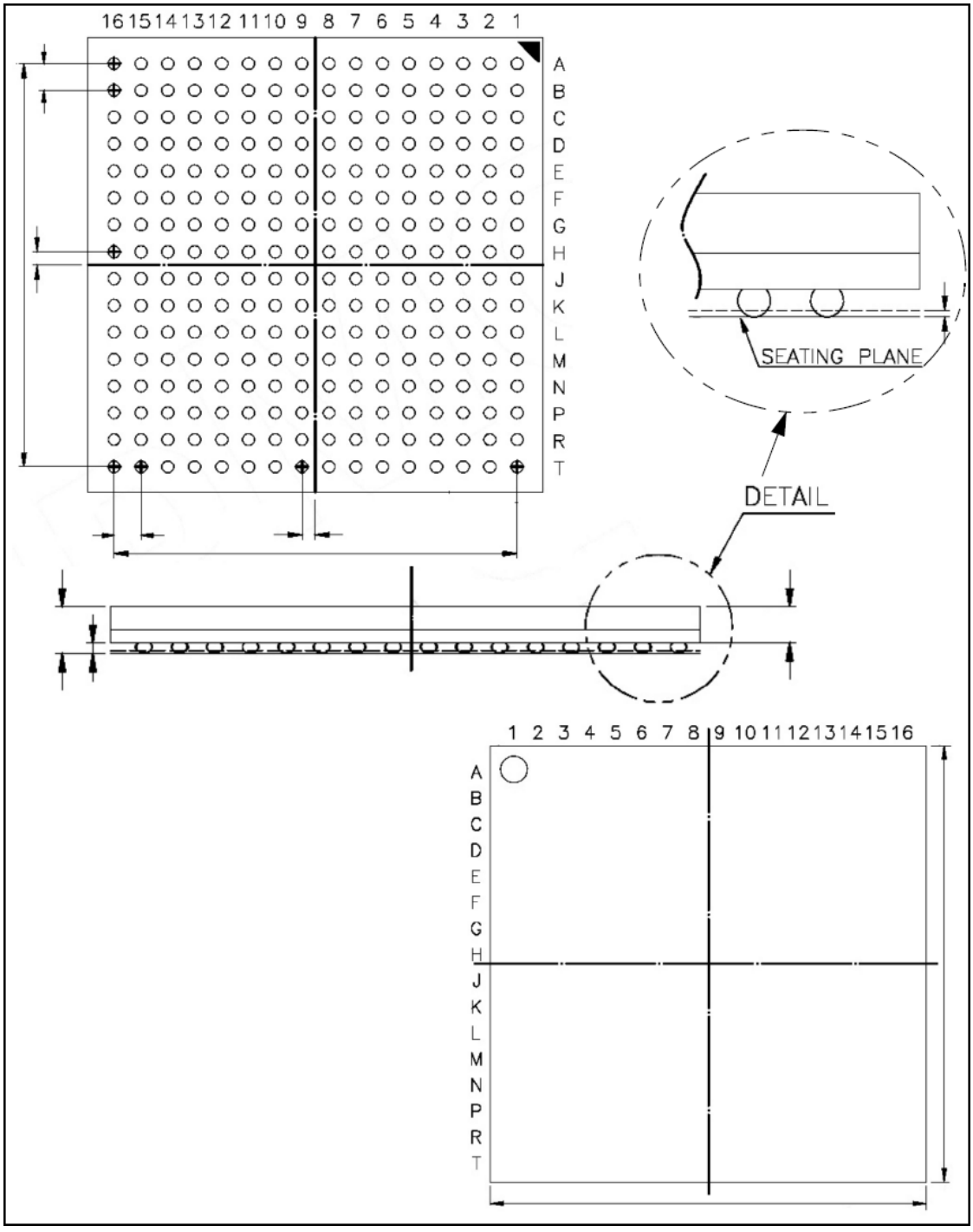
Table 2-4: 256-Ball TBGA Package Dimensions

Feature	Min	Nom	Max	Units
Overall Height (Including Ball Stand-Off)	--	--	1.20	mm
Ball Array Pattern		16 x 16		Balls
Pad Diameter	--	0.325	--	mm
Ball Pitch	--	0.800	--	mm
Ball Width	--	0.30	--	mm
Ball SRO	--	0.25	--	mm
Ball Height (Stand-Off)	0.20	0.25	0.30	mm
Side Dimension	13.90	14.00	14.10	mm
Ball Matrix Side Dimension (Ball Center to Ball Center)	--	12.000	--	mm

2.2.2 256-Ball TBGA Mechanical Drawing

Figure 2-2 provides the 256-ball TBGA package drawing.

Figure 2-2: 256-Ball TBGA Package Drawing



2.2.3 256-Ball TBGA Thermal Specification

Table 2-5 provides the 256-ball TBGA thermal design parameters.

Table 2-5: 256-Ball TBGA Thermal Design Parameters

Parameter	Value	Units
$T_{J\text{-}MAX}$ - Maximum Junction Temperature	115	°C
Θ_{JC} - Junction to Case Thermal Resistance	6.2	°C/W

2.2.4 256-Ball TBGA Ball Material Specification

Table 2-6 provides the materials and finish for the 400-ball TBGA package

Table 2-6: 256-Ball TBGA Materials Specification

Item	Value
Solder Ball Material	M705 / SAC305 (96.5Sn2Ag0.5Cu)
Substrate Solder Mask	Taiyo PSR4000 AUS 308
Surface Finish	COPPER: Min. 15um NICKEL: Min. 5um GOLD: Min. 0.3um
Flux Type	Qualitek PF-708

2.3 Storage Conditions

Table 2-7 provides the maximum and minimum storage temperatures for the SF-2000 family.

Table 2-7: Storage Conditions

Parameter	Absolute Minimum	Absolute Maximum	Units
Storage Temperature	-55	150	°C

3 Package Pinouts

3.1 Ball List - Signals

Table 3-1 provides the signal ball list for both the 400-ball TBGA and 256-ball TBGA packages.

Table 3-1: Ball List

Ball Name	400-Ball TBGA Ball	256-Ball TBGA Ball
ACTIVITY / GPIO0	K4	J3
ATEST	K2	G2
FAULT / GPIO1	L4	K3
FLASH_0_ALE	V5	N3
FLASH_0_CLE	W5	N2
FLASH_0_DQS	Y4	P4
FLASH_0_IO0	V1	R1
FLASH_0_IO1	W1	T2
FLASH_0_IO2	V2	R2
FLASH_0_IO3	W2	R3
FLASH_0_IO4	Y2	T3
FLASH_0_IO5	V3	R4
FLASH_0_IO6	V4	P1
FLASH_0_IO7	Y5	P2
FLASH_1_ALE	V10	P8
FLASH_1_CLE	Y10	R8
FLASH_1_DQS	Y9	R7
FLASH_1_IO0	Y6	T5
FLASH_1_IO1	W6	R5
FLASH_1_IO2	Y7	P5
FLASH_1_IO3	W7	T6
FLASH_1_IO4	V7	T7
FLASH_1_IO5	Y8	R6
FLASH_1_IO6	W8	P6
FLASH_1_IO7	V8	T8
FLASH_10_ALE	T17	--
FLASH_10_CLE	U18	--
FLASH_10_DQS	T14	--
FLASH_10_IO0	V17	--
FLASH_10_IO1	U17	--
FLASH_10_IO2	T16	--
FLASH_10_IO3	U16	--
FLASH_10_IO4	V16	--
FLASH_10_IO5	U15	--

Ball Name	400-Ball TBGA Ball	256-Ball TBGA Ball
FLASH_10_IO6	U14	--
FLASH_10_IO7	U13	--
FLASH_11_ALE	R16	--
FLASH_11_CLE	R17	--
FLASH_11_DQS	N17	--
FLASH_11_IO0	K17	--
FLASH_11_IO1	L17	--
FLASH_11_IO2	L18	--
FLASH_11_IO3	M18	--
FLASH_11_IO4	N18	--
FLASH_11_IO5	P18	--
FLASH_11_IO6	R18	--
FLASH_11_IO7	T18	--
FLASH_12_ALE	H17	--
FLASH_12_CLE	J17	--
FLASH_12_DQS	E16	--
FLASH_12_IO0	H18	--
FLASH_12_IO1	G18	--
FLASH_12_IO2	F18	--
FLASH_12_IO3	F17	--
FLASH_12_IO4	E17	--
FLASH_12_IO5	E18	--
FLASH_12_IO6	D17	--
FLASH_12_IO7	D18	--
FLASH_13_ALE	C15	--
FLASH_13_CLE	C14	--
FLASH_13_DQS	E14	--
FLASH_13_IO0	D16	--
FLASH_13_IO1	D15	--
FLASH_13_IO2	D14	--
FLASH_13_IO3	D13	--
FLASH_13_IO4	E12	--
FLASH_13_IO5	D12	--
FLASH_13_IO6	C12	--
FLASH_13_IO7	C13	--
FLASH_14_ALE	C11	--
FLASH_14_CLE	C9	--
FLASH_14_DQS	E10	--
FLASH_14_IO0	E7	--
FLASH_14_IO1	D7	--
FLASH_14_IO2	D8	--
FLASH_14_IO3	E8	--
FLASH_14_IO4	E9	--

Ball Name	400-Ball TBGA Ball	256-Ball TBGA Ball
FLASH_14_IO5	D9	--
FLASH_14_IO6	D10	--
FLASH_14_IO7	D11	--
FLASH_15_ALE	C6	--
FLASH_15_CLE	D6	--
FLASH_15_DQS	E6	--
FLASH_15_IO0	D3	--
FLASH_15_IO1	E1	--
FLASH_15_IO2	E2	--
FLASH_15_IO3	E3	--
FLASH_15_IO4	E4	--
FLASH_15_IO5	C4	--
FLASH_15_IO6	C5	--
FLASH_15_IO7	D5	--
FLASH_2_ALE	V13	P11
FLASH_2_CLE	W13	R11
FLASH_2_DQS	Y19	R14
FLASH_2_IO0	Y16	R13
FLASH_2_IO1	W16	P13
FLASH_2_IO2	Y15	T13
FLASH_2_IO3	W15	T12
FLASH_2_IO4	V15	T11
FLASH_2_IO5	V14	T10
FLASH_2_IO6	W14	P12
FLASH_2_IO7	Y14	R12
FLASH_3_ALE	T19	M14
FLASH_3_CLE	T20	M16
FLASH_3_DQS	M19	J14
FLASH_3_IO0	K19	H15
FLASH_3_IO1	K20	K14
FLASH_3_IO2	L19	K16
FLASH_3_IO3	L20	K15
FLASH_3_IO4	P19	L14
FLASH_3_IO5	P20	L15
FLASH_3_IO6	R19	L16
FLASH_3_IO7	R20	M15
FLASH_4_ALE	D20	D16
FLASH_4_CLE	E20	E15
FLASH_4_DQS	G19	F14
FLASH_4_IO0	K18	G16
FLASH_4_IO1	J18	G14
FLASH_4_IO2	J19	G15
FLASH_4_IO3	J20	F15

Ball Name	400-Ball TBGA Ball	256-Ball TBGA Ball
FLASH_4_IO4	H19	F16
FLASH_4_IO5	H20	E16
FLASH_4_IO6	E19	E13
FLASH_4_IO7	D19	E14
FLASH_5_ALE	A13	A12
FLASH_5_CLE	B13	C11
FLASH_5_DQS	C17	A14
FLASH_5_IO0	B12	B11
FLASH_5_IO1	A12	A11
FLASH_5_IO2	B14	D12
FLASH_5_IO3	A14	C12
FLASH_5_IO4	B15	B12
FLASH_5_IO5	A15	A13
FLASH_5_IO6	A16	B13
FLASH_5_IO7	A17	C13
FLASH_6_ALE	B7	A6
FLASH_6_CLE	C7	B7
FLASH_6_DQS	A5	B10
FLASH_6_IO0	C8	A9
FLASH_6_IO1	B8	B9
FLASH_6_IO2	A8	C9
FLASH_6_IO3	B9	A8
FLASH_6_IO4	A9	B8
FLASH_6_IO5	A10	C8
FLASH_6_IO6	B11	C7
FLASH_6_IO7	A11	A7
FLASH_7_ALE	B5	B6
FLASH_7_CLE	B6	C6
FLASH_7_DQS	A4	A5
FLASH_7_IO0	D1	B1
FLASH_7_IO1	C1	A2
FLASH_7_IO2	B1	B2
FLASH_7_IO3	D2	B3
FLASH_7_IO4	C2	C4
FLASH_7_IO5	B2	B4
FLASH_7_IO6	A2	A3
FLASH_7_IO7	A3	A4
FLASH_8_ALE	R2	--
FLASH_8_CLE	T3	--
FLASH_8_DQS	T6	--
FLASH_8_IO0	U1	--
FLASH_8_IO1	U2	--
FLASH_8_IO2	U3	--

Ball Name	400-Ball TBGA Ball	256-Ball TBGA Ball
FLASH_8_IO3	U4	--
FLASH_8_IO4	U5	--
FLASH_8_IO5	T1	--
FLASH_8_IO6	T2	--
FLASH_8_IO7	R1	--
FLASH_9_ALE	T8	--
FLASH_9_CLE	T9	--
FLASH_9_DQS	T11	--
FLASH_9_IO0	U11	--
FLASH_9_IO1	U10	--
FLASH_9_IO2	U9	--
FLASH_9_IO3	U8	--
FLASH_9_IO4	U7	--
FLASH_9_IO5	V6	--
FLASH_9_IO6	T7	--
FLASH_9_IO7	U6	--
FLASH_CE[0]	W20	R16
FLASH_CE[1]	V20	P16
FLASH_CE[10]	W19	N15
FLASH_CE[11]	V19	N16
FLASH_CE[12]	C18	C15
FLASH_CE[13]	B18	B15
FLASH_CE[14]	A18	A15
FLASH_CE[15]	A19	B16
FLASH_CE[2]	U20	R15
FLASH_CE[3]	U19	P14
FLASH_CE[4]	B19	C16
FLASH_CE[5]	B20	D13
FLASH_CE[6]	C19	D14
FLASH_CE[7]	C20	D15
FLASH_CE[8]	V18	N14
FLASH_CE[9]	W18	P15
FLASH_REN_N[0]	W3	T4
FLASH_REN_N[1]	V9	P7
FLASH_REN_N[10]	T15	--
FLASH_REN_N[11]	M17	--
FLASH_REN_N[12]	G17	--
FLASH_REN_N[13]	E13	--
FLASH_REN_N[14]	C10	--
FLASH_REN_N[15]	D4	--
FLASH_REN_N[2]	Y17	T14
FLASH_REN_N[3]	N20	J16
FLASH_REN_N[4]	F20	H16

Ball Name	400-Ball TBGA Ball	256-Ball TBGA Ball
FLASH_REN_N[5]	B16	B14
FLASH_REN_N[6]	A7	C10
FLASH_REN_N[7]	B3	B5
FLASH_REN_N[8]	T4	--
FLASH_REN_N[9]	T12	--
FLASH_WEN_N[0]	Y3	P3
FLASH_WEN_N[1]	W9	T9
FLASH_WEN_N[10]	T13	--
FLASH_WEN_N[11]	P17	--
FLASH_WEN_N[12]	F16	--
FLASH_WEN_N[13]	E15	--
FLASH_WEN_N[14]	E11	--
FLASH_WEN_N[15]	E5	--
FLASH_WEN_N[2]	Y18	T15
FLASH_WEN_N[3]	M20	J15
FLASH_WEN_N[4]	G20	H14
FLASH_WEN_N[5]	C16	C14
FLASH_WEN_N[6]	A6	A10
FLASH_WEN_N[7]	C3	C5
FLASH_WEN_N[8]	T5	--
FLASH_WEN_N[9]	T10	--
FLASH_WP0 / GPIO6	L3	J2
FLASH_WP1 / GPIO7	R3	K2
GPIO10	V11	R9
GPIO11	Y12	P9
GPIO12	Y13	P10
GPIO13	U12	N10
GPIO14	V12	L13
GPIO15	W12	M13
GPIO8	Y11	N9
GPIO9	W11	R10
I2C_SCLK / GPIO2	N4	M3
I2C_SDA / GPIO3	M4	L3
JTAG_TCK	G3	D3
JTAG_TDI	F1	C1
JTAG_TDO	F3	C3
JTAG_TMS	F4	E3
JTAG_TRST	F2	C2
PAC	K3	F3
PFAIL	P3	M2
PLL_CLK_OUT	F5	D5
POR_N	J3	H3
PORC_N	H3	G3

Ball Name	400-Ball TBGA Ball	256-Ball TBGA Ball
PWR_GOOD	H4	H4
PWR_GOODC	G4	G4
RS232_RXD / GPIO5	R4	M1
RS232_TXD / GPIO4	P4	N1
SATA_RREF	N2	L2
SATA_RX_N	K1	G1
SATA_RX_P	J1	F1
SATA_TX_N	M1	J1
SATA_TX_P	N1	K1
TEST_EN	J4	F2
VDDQ_EFUSE	R6	N4
XTAL1	G1	D1
XTAL2	G2	D2
No Connect	M3	--
No Connect	N3	--

3.2 No Connect Pins

Balls listed as “no connect” (NC) are not internally connected (electrical opens).

3.3 Ball List – Power and Ground

3.3.1 400-Ball TBGA Power and Ground Ball List

Table 3-2 provides the power and ground ball list for the 400-ball TBGA package.

Table 3-2: 400-Ball TBGA Power and Ground Balls

Ball Name	400-Ball TBGA Ball(s)
VSS	A1, A20, G7, G8, G9, G10, G11, G12, G13, G14, G15, H7, H8, H9, H10, H11, H12, H13, H14, H15, J7, J8, J9, J10, J11, J12, J13, J14, J15, K7, K8, K9, K10, K11, K12, K13, K14, K15, L6, L7, L8, L9, L10, L11, L12, L13, L14, L15, M6, M7, M8, M9, M10, M11, M12, M13, M14, M15, N6, N7, N8, N9, N10, N11, N12, N13, N14, N15, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15, Y1, Y20
VSSA	H1, L1, P1
VCCA_1V	H2, M2, P2
VCCA_3V	J2, L2
VDDC	F6, F8, F9, F11, F12, F14, F15, H16, J16, K16, L5, M16, N16, P5, R8, R9, R11, R12, R14, R15
VDD_GPIO	R5
VDD_FIO	B4, B10, B17, F7, F10, F13, F19, G16, L16, N19, P16, R7, R10, R13, W4, W10, W17
VDD_LPA_IO	M5
VDD_LPA_C	N5
VSSA_PLL	K6
VSSA2_PLL	J6
VSSA3_PLL	H6
VSSA4_PLL	G6
VDDA_PLL	K5
VDDA2_PLL	J5
VDDA3_PLL	H5
VDDA4_PLL	G5

3.3.2 256-Ball TBGA Power and Ground Ball List

Table 3-3 provides the power and ground ball list for the 256-ball TBGA package.

Table 3-3: 256-Ball TBGA Power and Ground Balls

Ball Name	256-Ball TBGA Ball(s)
VSS	A1, A16, E6, E7, E8, E9, E10, E11, E12, F6, F7, F8, F9, F10, F11, F12, G6, G7, G8, G9, G10, G11, G12, H5, H6, H7, H8, H9, H10, H11, H12, J6, J7, J8, J9, J10, J11, J12, K5, K6, K7, K8, K9, K10, K11, K12, L5, L6, L7, L8, L9, L10, L11, L12, M5, M6, M7, M8, M9, M10, M11, M12, T1, T16
VSSA	E1, H1, L1
VCCA_1V	H2
VCCA_3V	E2
VDDC	D7, D8, D10, G13, H13, J13, K4, N7, N8, N12
VDD_GPIO	N4
VDD_FIO	D6, D9, D11, F13, K13, N6, N11, N13
VDD_LPA_IO	L4
VDD_LPA_C	M4
VSSA_PLL	J5
VSSA2_PLL	G5
VSSA3_PLL	F5
VSSA4_PLL	E5
VDDA_PLL	J4
VDDA2_PLL	F4
VDDA3_PLL	E4
VDDA4_PLL	D4

3.4 Ballout Diagrams

3.4.1 400-Ball TBGA Ballout Diagram

Figures 3-1 to 3-4 illustrate the ball assignments for the 400-ball TBGA package. The view is of the PCB foot print through the top of the package.

Figure 3-1: 400-Ball TBGA Ball Assignments (1)

	1	2	3	4	5	6	7	8	9	10
A	VSS	FLASH_7_IO6	FLASH_7_IO7	FLASH_7_DQS	FLASH_6_DQS	FLASH_WEN_N[6]	FLASH_REN_N[6]	FLASH_6_IO2	FLASH_6_IO4	FLASH_6_IO5
B	FLASH_7_IO2	FLASH_7_IO5	FLASH_REN_N[7]	VDD_FIO	FLASH_7_ALE	FLASH_7_CLE	FLASH_6_ALE	FLASH_6_IO1	FLASH_6_IO3	VDD_FIO
C	FLASH_7_IO1	FLASH_7_IO4	FLASH_WEN_N[7]	FLASH_15_IO5	FLASH_15_IO6	FLASH_15_ALE	FLASH_6_CLE	FLASH_6_IO0	FLASH_14_CLE	FLASH_REN_N[14]
D	FLASH_7_IO0	FLASH_7_IO3	FLASH_15_IO0	FLASH_REN_N[15]	FLASH_15_IO7	FLASH_15_CLE	FLASH_14_IO1	FLASH_14_IO2	FLASH_14_IO5	FLASH_14_IO6
E	FLASH_15_IO1	FLASH_15_IO2	FLASH_15_IO3	FLASH_15_IO4	FLASH_WEN_N[15]	FLASH_15_DQS	FLASH_14_IO0	FLASH_14_IO3	FLASH_14_IO4	FLASH_14_DQS
F	JTAG_TDI	JTAG_TRST	JTAG_TDO	JTAG_TMS	PLL_CLK_OUT	VDDC	VDD_FIO	VDDC	VDDC	VDD_FIO
G	XTAL1	XTAL2	JTAG_TCK	PWR_GOODC	VDDA4_PLL	VSSA4_PLL	VSS	VSS	VSS	VSS
H	VSSA	VCCA_1V	PORC_N	PWR_GOOD	VDDA3_PLL	VSSA3_PLL	VSS	VSS	VSS	VSS
J	SATA_RX_P	VCCA_33V	POR_N	TEST_EN	VDDA2_PLL	VSSA2_PLL	VSS	VSS	VSS	VSS
K	SATA_RX_N	ATEST	PAC	GPIO0	VDDA_PLL	VSSA_PLL	VSS	VSS	VSS	VSS

Figure 3-2: 400-Ball TBGA Ball Assignments (2)

	11	12	13	14	15	16	17	18	19	20
A	FLASH_6_IO7	FLASH_5_IO1	FLASH_5_ALE	FLASH_5_IO3	FLASH_5_IO5	FLASH_5_IO6	FLASH_5_IO7	FLASH_CE14	FLASH_CE15	VSS
B	FLASH_6_IO6	FLASH_5_IO0	FLASH_5_CLE	FLASH_5_IO2	FLASH_5_IO4	FLASH_REN_N[5]	VDD_FIO	FLASH_CE13	FLASH_CE4	FLASH_CE5
C	FLASH_14_ALE	FLASH_13_IO6	FLASH_13_IO7	FLASH_13_CLE	FLASH_13_ALE	FLASH_WEN_N[5]	FLASH_5_DQS	FLASH_CE12	FLASH_CE6	FLASH_CE7
D	FLASH_14_IO7	FLASH_13_IO5	FLASH_13_IO3	FLASH_13_IO2	FLASH_13_IO1	FLASH_13_IO0	FLASH_12_I06	FLASH_12_IO7	FLASH_4_IO7	FLASH_4_ALE
E	FLASH_WEN_N[14]	FLASH_13_IO4	FLASH_REN_N[13]	FLASH_13_DQS	FLASH_WEN_N[13]	FLASH_12_DQS	FLASH_12_I04	FLASH_12_I05	FLASH_4_IO6	FLASH_4_CLE
F	VDDC	VDDC	VDD_FIO	VDDC	VDDC	FLASH_WEN_N[12]	FLASH_12_I03	FLASH_12_IO2	VDD_FIO	FLASH_REN N[4]
G	VSS	VSS	VSS	VSS	VSS	VDD_FIO	FLASH_REN_N[12]	FLASH_12_I01	FLASH_4_DQS	FLASH_WEN N[4]
H	VSS	VSS	VSS	VSS	VSS	VDDC	FLASH_12_ALE	FLASH_12_I00	FLASH_4_IO4	FLASH_4_IO5
J	VSS	VSS	VSS	VSS	VSS	VDDC	FLASH_12_CLE	FLASH_4_IO1	FLASH_4_IO2	FLASH_4_IO3
K	VSS	VSS	VSS	VSS	VSS	VDDC	FLASH_11_IO0	FLASH_4_IO0	FLASH_3_IO0	FLASH_3_IO1

Figure 3-3: 400-Ball TBGA Ball Assignments (3)

	1	2	3	4	5	6	7	8	9	10
L	VSSA	VCCA_33V	FLASH_WP0	GPIO1	VDDC	VSS	VSS	VSS	VSS	VSS
M	SATA_TX_N	VCCA_1V	NC	I2C_SDA	VDD_LPA_IO	VSS	VSS	VSS	VSS	VSS
N	SATA_TX_P	SATA_RREF	NC	I2C_SCLK	VDD_LPA_C	VSS	VSS	VSS	VSS	VSS
P	VSSA	VCCA_1V	PFAIL	RS232_TXD/GPIO4	VDDC	VSS	VSS	VSS	VSS	VSS
R	FLASH_8_IO7	FLASH_8_ALE	FLASH_WP1	RS232_RXD/GPIO5	VDD_GPIO	VDDQ_EFUSE	VDD_FIO	VDDC	VDDC	VDD_FIO
T	FLASH_8_IO5	FLASH_8_IO6	FLASH_8_CLE	FLASH_REN_N[8]	FLASH_WEN_N[8]	FLASH_8_DQS	FLASH_9_IO6	FLASH_9_ALE	FLASH_9_CLE	FLASH_WEN_N[9]
U	FLASH_8_IO0	FLASH_8_IO1	FLASH_8_IO2	FLASH_8_IO3	FLASH_8_IO4	FLASH_9_IO7	FLASH_9_IO4	FLASH_9_IO3	FLASH_9_IO2	FLASH_9_IO1
V	FLASH_0_IO0	FLASH_0_IO2	FLASH_0_IO5	FLASH_0_IO6	FLASH_0_ALE	FLASH_9_IO5	FLASH_1_IO4	FLASH_1_IO7	FLASH_REN_N[1]	FLASH_1_ALE
W	FLASH_0_IO1	FLASH_0_IO3	FLASH_REN N[0]	VDD_FIO	FLASH_0_CLE	FLASH_1_IO1	FLASH_1_IO3	FLASH_1_IO6	FLASH_WEN_N[1]	VDD_FIO
Y	VSS	FLASH_0_IO4	FLASH_WEN N[0]	FLASH_0_DQS	FLASH_0_IO7	FLASH_1_IO0	FLASH_1_IO2	FLASH_1_IO5	FLASH_1_DQS	FLASH_1_CLE

Figure 3-4: 400-Ball TBGA Ball Assignments (4)

	11	12	13	14	15	16	17	18	19	20
L	VSS	VSS	VSS	VSS	VSS	VDD_FIO	FLASH_11_IO1	FLASH_11_IO2	FLASH_3_IO2	FLASH_3_IO3
M	VSS	VSS	VSS	VSS	VSS	VDDC	FLASH_REN_N[11]	FLASH_11_IO3	FLASH_3_DQS	FLASH_WEN_N[3]
N	VSS	VSS	VSS	VSS	VSS	VDDC	FLASH_11_DQS	FLASH_11_IO4	VDD_FIO	FLASH_REN_N[3]
P	VSS	VSS	VSS	VSS	VSS	VDD_FIO	FLASH_WEN_N[11]	FLASH_11_IO5	FLASH_3_IO4	FLASH_3_IO5
R	VDDC	VDDC	VDD_FIO	VDDC	VDDC	FLASH_11_ALE	FLASH_11_CLE	FLASH_11_IO6	FLASH_3_IO6	FLASH_3_IO7
T	FLASH_9_DQS	FLASH_REN_N[9]	FLASH_WEN_N[10]	FLASH_10_DQS	FLASH_REN_N[10]	FLASH_10_IO2	FLASH_10_ALE	FLASH_11_IO7	FLASH_3_ALE	FLASH_3_CLE
U	FLASH_9_IO0	GPIO13	FLASH_10_IO7	FLASH_10_IO6	FLASH_10_IO5	FLASH_10_IO3	FLASH_10_IO1	FLASH_10_CLE	FLASH_CE3	FLASH_CE2
V	GPIO10	GPIO14	FLASH_2_ALE	FLASH_2_IO5	FLASH_2_IO4	FLASH_10_IO4	FLASH_10_IO0	FLASH_CE8	FLASH_CE11	FLASH_CE1
W	GPIO9	GPIO15	FLASH_2_CLE	FLASH_2_IO6	FLASH_2_IO3	FLASH_2_IO1	VDD_FIO	FLASH_CE9	FLASH_CE10	FLASH_CE0
Y	GPIO8	GPIO11	GPIO12	FLASH_2_IO7	FLASH_2_IO2	FLASH_2_IO0	FLASH_REN N[2]	FLASH_WEN N[2]	FLASH_2_DQS	VSS

3.4.2 256-Ball TBGA Ballout Diagram

Figures 3-5 to 3-8 illustrate the ball assignments for the 256-ball TBGA package. The view is of the PCB foot print through the top of the package.

Figure 3-5: 256-Ball TBGA Ball Assignments (1)

	1	2	3	4	5	6	7	8
A	VSS	FLASH_7_IO1	FLASH_7_IO6	FLASH_7_IO7	FLASH_7_DQS	FLASH_6_ALE	FLASH_6_IO7	FLASH_6_IO3
B	FLASH_7_IO0	FLASH_7_IO2	FLASH_7_IO3	FLASH_7_IO5	FLASH_REN_N[7]	FLASH_7_ALE	FLASH_6_CLE	FLASH_6_IO4
C	JTAG_TDI	JTAG_TRST	JTAG_TDO	FLASH_7_IO4	FLASH_WEN_N[7]	FLASH_7_CLE	FLASH_6_IO6	FLASH_6_IO5
D	XTAL1	XTAL2	JTAG_TCK	VDDA4_PLL	PLL_CLK_OUT	VDD_FIO	VDDC	VDDC
E	VSSA	VCCA_33V	JTAG_TMS	VDDA3_PLL	VSSA4_PLL	VSS	VSS	VSS
F	SATA_RX_P	TEST_EN	PAC	VDDA2_PLL	VSSA3_PLL	VSS	VSS	VSS
G	SATA_RX_N	ATEST	PORC_N	PWR_GOODC	VSSA2_PLL	VSS	VSS	VSS
H	VSSA	VCCA_1V	POR_N	PWR_GOOD	VSS	VSS	VSS	VSS

Figure 3-6: 256-Ball TBGA Ball Assignments (2)

	9	10	11	12	13	14	15	16
A	FLASH_6_IO0	FLASH_WEN_N[6]	FLASH_5_IO1	FLASH_5_ALE	FLASH_5_IO5	FLASH_5_DQS	FLASH_CE14	VSS
B	FLASH_6_IO1	FLASH_6_DQS	FLASH_5_IO0	FLASH_5_IO4	FLASH_5_IO6	FLASH_REN_N[5]	FLASH_CE13	FLASH_CE15
C	FLASH_6_IO2	FLASH_REN_N[6]	FLASH_5_CLE	FLASH_5_IO3	FLASH_5_IO7	FLASH_WEN_N[5]	FLASH_CE12	FLASH_CE4
D	VDD_FIO	VDDC	VDD_FIO	FLASH_5_IO2	FLASH_CE5	FLASH_CE6	FLASH_CE7	FLASH_4_ALE
E	VSS	VSS	VSS	VSS	FLASH_4_IO6	FLASH_4_IO7	FLASH_4_CLE	FLASH_4_IO5
F	VSS	VSS	VSS	VSS	VDD_FIO	FLASH_4_DQS	FLASH_4_IO3	FLASH_4_IO4
G	VSS	VSS	VSS	VSS	VDDC	FLASH_4_IO1	FLASH_4_IO2	FLASH_4_IO0
H	VSS	VSS	VSS	VSS	VDDC	FLASH_WEN_N[4]	FLASH_3_IO0	FLASH_REN_N[4]

Figure 3-7: 256-Ball TBGA Ball Assignments (3)

	1	2	3	4	5	6	7	8
J	SATA_TX_N	FLASH_WP0	GPIO0	VDDA_PLL	VSSA_PLL	VSS	VSS	VSS
K	SATA_TX_P	FLASH_WP1	GPIO1	VDDC	VSS	VSS	VSS	VSS
L	VSSA	SATA_RREF	I2C_SDA	VDD_LPA_IO	VSS	VSS	VSS	VSS
M	GPIO5_RS232_RXD	PFAIL	I2C_SCLK	VDD_LPA_C	VSS	VSS	VSS	VSS
N	GPIO4_RS232_TXD	FLASH_0_CLE	FLASH_0_ALE	VDD_GPIO	VDDQ_EFUSE	VDD_FIO	VDDC	VDDC
P	FLASH_0_IO6	FLASH_0_IO7	FLASH_WEN_N[0]	FLASH_0_DQS	FLASH_1_IO2	FLASH_1_IO6	FLASH_REN_N[1]	FLASH_1_ALE
R	FLASH_0_IO0	FLASH_0_IO2	FLASH_0_IO3	FLASH_0_IO5	FLASH_1_IO1	FLASH_1_IO5	FLASH_1_DQS	FLASH_1_CLE
T	VSS	FLASH_0_IO1	FLASH_0_IO4	FLASH_REN_N[0]	FLASH_1_IO0	FLASH_1_IO3	FLASH_1_IO4	FLASH_1_IO7

Figure 3-8: 256-Ball TBGA Ball Assignments (4)

	9	10	11	12	13	14	15	16
J	VSS	VSS	VSS	VSS	VDDC	FLASH_3_DQS	FLASH_WEN_N[3]	FLASH_REN_N[3]
K	VSS	VSS	VSS	VSS	VDD_FIO	FLASH_3_IO1	FLASH_3_IO3	FLASH_3_IO2
L	VSS	VSS	VSS	VSS	GPIO14	FLASH_3_IO4	FLASH_3_IO5	FLASH_3_IO6
M	VSS	VSS	VSS	VSS	GPIO15	FLASH_3_ALE	FLASH_3_IO7	FLASH_3_CLE
N	GPIO8	GPIO13	VDD_FIO	VDDC	VDD_FIO	FLASH_CE8	FLASH_CE10	FLASH_CE11
P	GPIO11	GPIO12	FLASH_2_ALE	FLASH_2_IO6	FLASH_2_IO1	FLASH_CE3	FLASH_CE9	FLASH_CE1
R	GPIO10	GPIO9	FLASH_2_CLE	FLASH_2_IO7	FLASH_2_IO0	FLASH_2_DQS	FLASH_CE2	FLASH_CE0
T	FLASH_WEN_N[1]	FLASH_2_IO5	FLASH_2_IO4	FLASH_2_IO3	FLASH_2_IO2	FLASH_REN_N[2]	FLASH_WEN_N[2]	VSS

4 Power Supply Specification

4.1 Power Supply Operating Conditions

Table 4-1 describes the operating conditions for each power supply of the SF-2000. Supply voltage levels must not violate the minimum and maximum conditions during normal operation.

Table 4-1: Power Supply Operating Conditions

Supply	Voltage Level [V]			I_{DD} [mA]		
	Min	Typ	Max	Min	Typ (Note 1)	Max (Note 2)
V_{DDC} Core Supply	0.95	1.0	1.05	--	1250	2100
$V_{DD\_LPA\_C}$ Core Supply (Low Power Active)	0.95	1.0	1.05	--	20	21
$V_{DDA\_PLL[4:1]}$ PLL Supply	0.95	1.0	1.05	--	15	16
V_{CCA_1V} SATA PHY Supply	0.95	1.0	1.05	--	220	231
V_{CCA_33V} SATA PHY IO Supply	2.7	2.8	2.9	--	168	176
V_{DD_GPIO} GPIO Supply	2.7	2.8	2.9	--	28	29
$V_{DD\_LPA\_IO}$ GPIO Supply (Low Power Active)	2.7	2.8	2.9	--	56	59
V_{DD_FIO} Flash IO Supply	2.7	2.8	2.9	--	TBD	TBD
	1.7	1.8	1.9	--	350	368

Note 1 – Typical Conditions: 55°C case temperature, IOMeter 2006 100% 128k aligned sequential writes with 32 outstanding IOs, typical voltage values, 83 MHz flash interface at 1.8V.

Note 2 – Max Conditions: 110°C case temperature, IOMeter 2006 100% 128k aligned sequential writes with 32 outstanding IOs, max voltage values, 83 MHz flash interface at 1.8V.

4.1.1 Power Consumption

Table 4-2 contains the total power consumption of the SF-2000 device.

Table 4-2: Power Consumption

Signal	Min	Typ	Max	Units
Total Power Consumption (All Supplies)	--	2.11 (Note 1)	3.0 (Note 2)	W

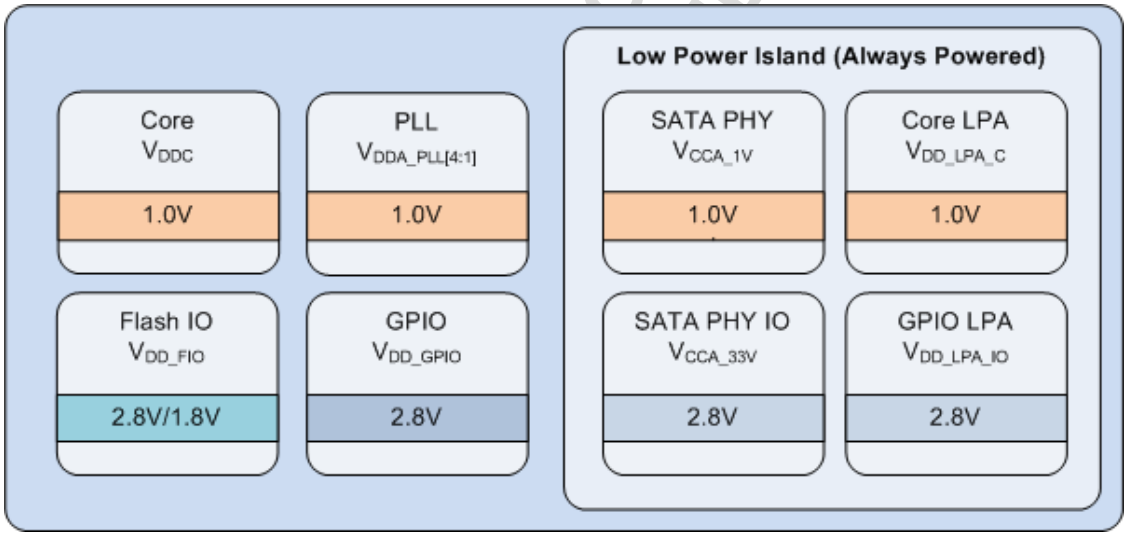
Note 1: Conditions follow from Table 4-1.

Note 2: Conditions follow from Table 4-1.

4.2 Power Domains and Voltage Rail Requirements

Figure 4-1 illustrates the power domains of the SF-2000. The number of external voltage rails depends on the flash interface voltage and sleep/standby configuration.

Figure 4-1: Power Domains



4.2.1 Minimum Rail Configuration

The minimum rail configuration requires two supply rails: a 1.0V rail that is connected to all 1.0V power supplies and a 2.8V rail that is connected to all 2.8V supplies. This basic configuration does not support low power standby. An additional 1.8V Flash IO rail is required to support synchronous Flash interfaces (ONFI, Toggle).

4.2.2 Low Power Standby Configuration

The supplies associated with the low power island must always remain powered. The supplies that are not associated with the low power island can be shut down during sleep and standby modes via the PAC (Power Application Control) signal. This optional configuration requires two independent 1.0V rails and two independent 2.8V rails. One 1.0V rail is connected to V_{DDC} and $V_{DDA\_PLL[4:1]}$, while the other 1.0V rail is connected to V_{CCA_1V} and $V_{DD\_LPA\_C}$. Similarly, one 2.8V rail is connected to V_{DD_GPIO} and (if applicable) V_{DD_FIO}, while the other 2.8V rail is connected to V_{CCA_33V} and $V_{DD\_LPA\_IO}$. When the PAC signal is active, the rails that are not associated with the low power island can be shut down to conserve power during sleep and standby.

4.2.3 Flash Interface IO Supply

Synchronous flash interfaces operate with a 1.8V Flash IO interface, requiring an additional 1.8V supply rail. If the legacy 2.8V asynchronous interface is used, the Flash IO rail can be shared with the existing 2.8V rail. Note that the V_{DD_GPIO} supply can be shared with Flash core power.

4.2.4 Supply Rail Configuration Summary

Table 4-3 summarizes the possible supply rail configurations of the SF-2000.

Table 4-3: Power Supply Rails

<table>
<tr><th>Supply</th><th>Configuration A</th><th>Configuration B</th><th>Configuration C</th><th>Configuration D</th></tr>
<tr><td rowspan="2"></td><td colspan="2">Low Power Mode Not Supported</td><td colspan="2">Low Power Mode Supported</td></tr>
<tr><td>2.8V Flash IO</td><td>1.8V Flash IO</td><td>2.8V Flash IO</td><td>1.8V Flash IO</td></tr>
<tr><td>V_{DDC}</td><td rowspan="4">1.0V Rail
(Always Active)</td><td rowspan="4">1.0V Rail
(Always Active)</td><td rowspan="2">1.0V Rail
(PAC Controlled)</td><td rowspan="2">1.0V Rail
(PAC Controlled)</td></tr>
<tr><td>$V_{DDA\_PLL[4:1]}$</td></tr>
<tr><td>$V_{DD\_LPA\_C}$</td><td rowspan="2">1.0V Rail
(Always Active)</td><td rowspan="2">1.0V Rail
(Always Active)</td></tr>
<tr><td>V_{CCA_1V}</td></tr>
<tr><td>V_{DD_FIO}</td><td rowspan="4">2.8V Rail
(Always Active)</td><td>1.8V Flash Rail
(Always Active)</td><td rowspan="2">2.8V Rail
(PAC Controlled)</td><td>1.8V Flash Rail
(PAC Controlled)</td></tr>
<tr><td>V_{DD_GPIO}</td><td rowspan="3">2.8V Rail
(Always Active)</td><td>2.8V Rail
(PAC Controlled)</td></tr>
<tr><td>$V_{DD\_LPA\_IO}$</td><td rowspan="2">2.8V Rail
(Always Active)</td><td rowspan="2">2.8V Rail
(Always Active)</td></tr>
<tr><td>V_{CCA_33V}</td></tr>
</table>

4.3 Power Supply Rail Sequencing

The following guidelines must be met for supply rail sequencing during power-on:

- The 2.8V supply rail should not ramp up earlier than the 1.0V rail or the 1.8V supply rail. The 1.0V rail should ramp to 80% of nominal before the 2.8V or 1.8V rails ramp to a value greater than the 1.0V rail. This can be achieved by simultaneous ramp-up, or by sequencing the 1.0V power rail to ramp up ahead of the 2.8V rail.
- The 1.8V supply rail should not ramp up earlier than the 1.0V rail. The 1.0V rail should ramp to 80% of nominal before the 1.8V rail ramps to a value greater than the 1.0V rail. This can be achieved by simultaneous ramp-up, or by sequencing the 1.0V power rail to ramp up ahead of the 1.8V rail.
- It is recommended to ramp the 1.8V at the same time or later than the 2.8V rail. Please consult the power sequencing requirements for the Flash devices used in the design.

Figure 4-2 illustrates a simultaneous ramp-up sequence. Figure 4-3 illustrates a staggered ramp-up sequence. A simultaneous ramp-up sequence is recommended for simplicity.

Figure 4-2: Simultaneous Ramp-Up Sequence

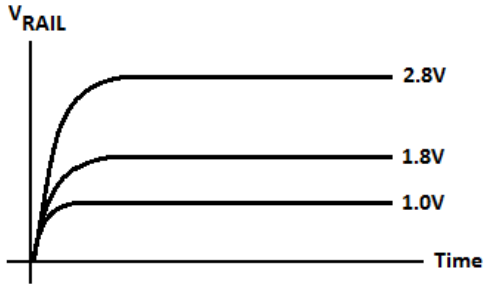
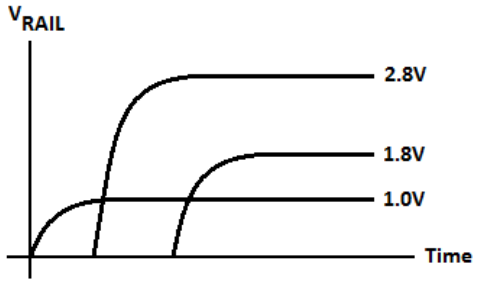


Figure 4-3: Sequential Ramp-Up Sequence



4.3.1 Power Supply Ramp Rate

There is no minimum or maximum power supply rail ramp rate. Any overshoot or undershoot should be confined to the minimum and maximum operating conditions for the rail. Power rail transitions should be monotonic.

4.4 Absolute Maximum Ratings

Table 4-4 describes the absolute maximum and minimum voltage levels which, if exceeded, could result in permanent damage to the device.

Table 4-4: Absolute Maximum Ratings

Supply	Description	Absolute Min	Absolute Max
V_{DDC}	Core Logic Supply	-0.3V	1.4V
$V_{DD\_LPA\_C}$	Core Logic Supply (Low Power Active)	-0.3V	1.4V
$V_{DDA\_PLL[4:1]}$	PLL Power	-0.3V	1.4V
V_{CCA_1V}	SATA PHY Power	-0.3V	1.4V
V_{CCA_33V}	SATA PHY IO Power	-0.3V	3.6V
V_{DD_GPIO}	GPIO Power	-0.3V	3.6V
$V_{DD\_LPA\_IO}$	GPIO Power (Low Power Active)	-0.3V	3.6V
V_{DD_FIO}	Flash IO Power	-0.3V	3.6V

4.5 Ground Connections

Table 4-5 describes the ground connections of the SF-2000.

Table 4-5: Ground Connections

Supply	Description
V_{SS}	**Device / Thermal Ground** These ground connections should be tied directly to the PCB ground plane.
V_{SSA}	**Analog Ground** These ground connections should be tied directly to the same ground plane as V_{SS}. It is recommended that V_{SSA} balls do not share vias.
$V_{SSA\_PLL[4:1]}$	**PLL Analog Ground** These ground connections should be tied directly to the same ground plane as V_{SS}. It is recommended that V_{SSA_PLL} balls do not share vias.

5 Signal Descriptions

5.1 Clock Signals

The clock signals are presented in Table 5-1.

Table 5-1: Clock Signals

Signal	Direction	Type	Description
XTAL_IN	Input	Analog Input	**Crystal/Oscillator Input** If generating the clock via a crystal, connect this pin as the XTAL IN signal. If generating the clock via an oscillator, connect the oscillator output to this pin.
XTAL_OUT	Output / NC	Analog Output	**Crystal Output** If generating the clock via a crystal, connect this pin as the XTAL OUT signal. If using an external oscillator to generate the clock, this signal should be left unconnected.
PLL_CLK_OUT	Output / NC	NA	**SandForce Reserved** Manufacturing test point.

5.1.1 Clock Requirements

The clock requirements are outlined in Table 5-2.

Table 5-2: Clock Input Requirements

Clock Parameter	Value	Unit
Frequency	30	MHz
Frequency Tolerance	+/- 30	ppm
Maximum ESR	TBD	Ohms
Maximum Jitter	+/- 5	ps
Voltage Level	Consistent with $V_{DD\_LPA\_IO}$	
Spread Spectrum Input	Not Supported	
Frequency Tolerance Over Temperature	TBD	

5.2 Reset Signals

The reset signals are presented in table 5-3.

Table 5-3: Reset Signals

Signal	Direction	Type	Description
PORC_N	Input	Logic Input with Internal Hysteresis Active Low	**Power-On Reset for Core Logic** This active-low input resets logic outside the always active island. PORC_N is implemented with a Schmitt Trigger input cell to establish hysteresis. There are no integrated pull-up or pull-down resistors on this signal.
POR_N	Input	Logic Input with Internal Hysteresis Active Low	**Power-On Reset for Always Active Island** This active-low input resets logic within the always active island. POR_N is implemented with a Schmitt Trigger input cell to establish hysteresis. There are no integrated pull-up or pull-down resistors on this signal.
PWR_GOODC	Output	Logic Output Active Low	**Power Good Indicator for Core Logic** Power good indicator for PORC_N domain. If desired, this may be tied to PORC_N instead of using an external reset circuit.
PWR_GOOD	Output	Logic Output Active Low	**Power Good Indicator for Always Active Island** Power good indicator for the POR_N domain. If desired, this may be tied to POR_N instead of using an external reset circuit.

5.2.1 Power-On Reset Usage (External Generation)

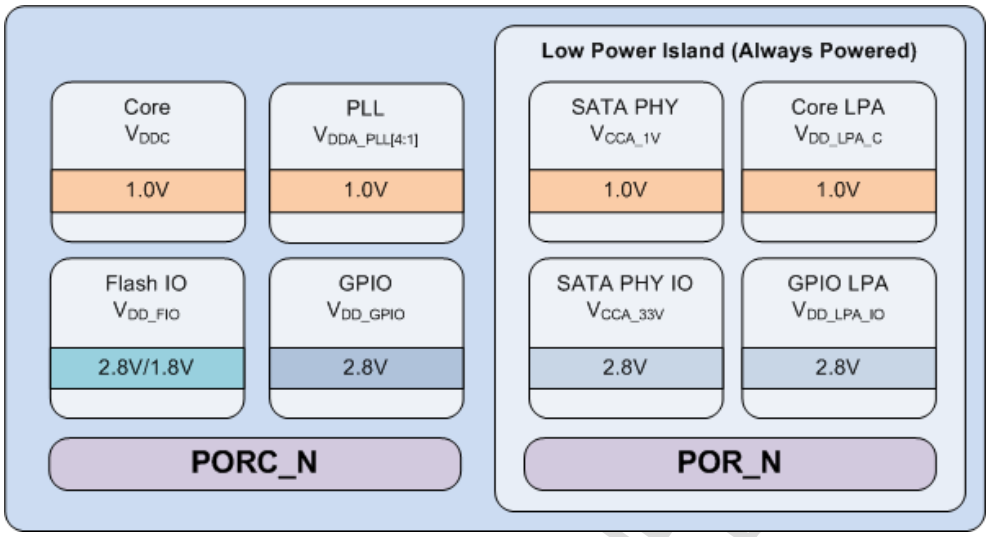
If the low power standby configuration is not implemented (see Section 4.2.1), PORC_N and POR_N should be tied together and treated as a single reset. Otherwise, PORC_N should be generated independently of POR_N.

PORC_N allows the low power island to be reset when its 1.0V supply rail is controlled by the PAC signal, without subjecting the always active island (which sources the PAC signal) to reset. PORC_N must be asserted when POR_N transitions from an asserted state to a negated state.

Any external reset circuit must ensure a logic low on PORC_N and POR_N for a duration equal to or greater than the minimum required assertion time, followed by a clean, noise-free deassertion. Deassertion should ensure that PORC_N and POR_N are pulled or driven to 2.5V or higher. If PORC_N and POR_N are both asserted, PORC_N should not deassert before POR_N.

Figure 5-1 shows the reset domain associated with each supply.

Figure 5-1: Reset Domains



5.2.2 Reset Requirements

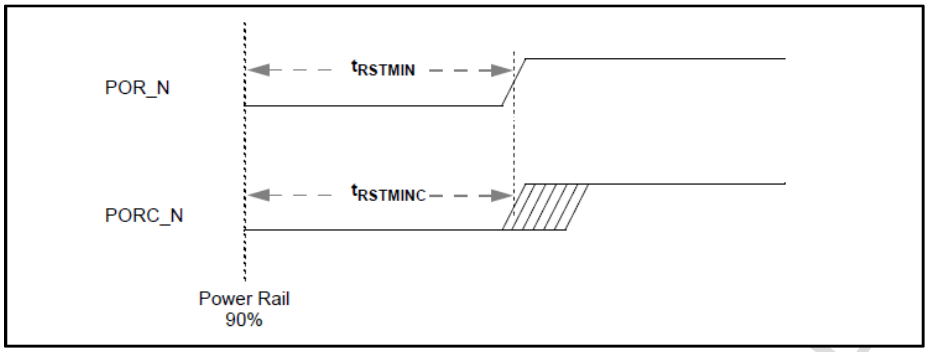
Table 5-4 contains the reset signal requirements. Reset must be asserted for the minimum pulse with after all power supplies have reached at least 90% of nominal (power stable condition).

Table 5-4: Reset Pin Requirements

Reset Parameter	Value	Unit
POR_N assertion from Power Stable Condition (t_{RSTMIN})	100	µsec
PORC_N assertion from Power Stable Condition ($t_{RSTMINC}$)	t_{RSTMIN} (Note 1)	µsec

Note 1: PORC_N must always be asserted when POR_N is asserted.

Figure 5-2: Reset Timing



5.3 Power Conditions

The power condition signals are presented in table 5-5.

Table 5-5: Power Condition Signals

Signal	Direction	Type	Description
PFAIL	Input	Logic Input Active Low Internal Pull-Up (50-100 kOhm)	**Power Fail** This active-low input is used as an "interrupt" to the SF-2000 by external circuitry to indicate that a potentially catastrophic condition exists (such as a loss of supply voltage, or rapidly rising temperature). The SF-2000 reacts to assertion of this signal by conserving power, hardening data immediately, and placing itself in a reset state. This Input cell is powered by V_{DD_GPIO}.
DATA_HARDENED (GPIO9)	Output (Input During and After Reset)	Logic Output Active High Internal Pull-Down	**Data Hardened Indicator** After the PFAIL signal is asserted to the SF-2000 in an emergency shutdown scenario, the SF-2000 hardens data and then asserts this output signal to indicate to the host system or external subsystem components that data is safe. The output cell is powered by V_{DD_GPIO}.
PAC	Output	Logic Output Active High Internal Pull-Up (50-100 kOhm)	**Power Application Control** This active-high output signal may be used to enable/disable voltage regulators or control power switching devices. When the SF-2000 drives this signal high, it enables (and expects) power to be applied to the low power island. When driven low, the supply rail for the low power island can be shut off to conserve power. The output cell is powered by $V_{DD\_LPA\_IO}$.
TESTCAP (GPIO12)	IO (Input During and After Reset)	Logic Output Active High Internal Pull-Down	**Test SuperCapacitor** This signal is used as an output to trigger discharge of the SuperCapacitor during an in-system SuperCapacitor test. When the chip asserts this signal, external circuitry switches to SuperCapacitor test mode. This IO cell is powered by V_{DD_GPIO}.

5.3.1 PFAIL and DATA_HARDENED Timing Parameters

The power condition signals are presented in table 5-6.

Table 5-6: PFAIL and DATA_HARDENED Timing

Signal	Min	Typ	Max	Units
PFAIL Assertion Width (t_{PFHIGH})	1000	--	--	us
Supply Rail Hold-up Time ($t_{SRHOLDUP}$)	Varies (Note 1)	--	--	ms
Data_Hardened Assertion Duration (t_{DHARD})	--	--	5000 (Note 2)	ms

Note 1: Please refer to the SF-25xx SF-26xx Power Fail Calculator to derive the minimum required hold up time and energy storage requirements. This specification must be met or exceeded regardless of age or condition of supply rail hold-up mechanism; also regardless of age or type of Flash memory.

Note 2: DATA_HARDENED is asserted by the SF-2000 until it is reset. If external circuitry fails to reset the SF-2000 (via PORC_N assertion) within the specified maximum, the SF-2000 auto-resets itself after the specified maximum, at which time DATA_HARDENED is deasserted.

5.4 I²C Signals

The I²C signals are presented in table 5-7.

Table 5-7: I²C Signals

Signal	Direction	Type	Description
I2C_SCLK (GPIO2)	IO (Input During and After Reset)	Logic IO Internal Pull-Up (50-100 kOhm)	**I2C Serial Clock** This bidirectional signal represents the I²C interface clock. This IO cell is powered by V_{DD_GPIO}.
I2C_SDA (GPIO3)	IO (Input During and After Reset)	Logic IO Internal Pull-Up (50-100 kOhm)	**I2C Serial Data** This bidirectional signal represents the I²C interface serial data line. This IO cell is powered by $_{VDD\_GPIO}$.

5.5 Serial Debug Port Signals

The serial debug port signals are presented in table 5-9.

Table 5-8: Serial Debug Port Signals

Signal	Direction	Type	Description
RS232_TXD (GPIO4)	IO (Input During and After Reset)	Logic IO Internal Pull-Up (50-100 kOhm)	**RS232 Transmit Data** The transmit signal for the RS-232 port. This IO cell is powered by V_{DD_GPIO}.
RS232_RXD (GPIO5)	IO (Input During and After Reset)	Logic IO Internal Pull-Up (50-100 kOhm)	**RS232 Receive Data** The receive signal for the RS-232 port. This IO cell is powered by V_{DD_GPIO}.

Note: The serial debug port signals must be made accessible for failure analysis purposes. Convenient test points are strongly recommended.

5.6 Indicator Signals

The indicator signals are presented in table 5-10.

Table 5-9: Indicator Signals

Signal	Direction	Type	Description
Activity (GPIO0)	IO (Input During and After Reset)	Logic IO Internal Pull-Up (50-100 kOhm)	**Activity Indicator** This signal is the default LED driver signal to reflect drive activity See the Software Reference Manual for specifics of LED behavior. This IO cell is powered by $V_{DD\_LPA\_IO}$.
Fault (GPIO1)	IO (Input During and After Reset)	Logic IO Internal Pull-Up (50-100 kOhm)	**Fault Indicator** This signal is the default fault signal, to drive LEDs and/or alert the system to fault conditions. See the Software Reference Manual for specifics of fault signal behavior. This IO cell is powered by $V_{DD\_LPA\_IO}$. **Force Download Mode**: This is the input of the force download mode. GPIO6 is temporarily shorted to GPIO1 at reset deassertion to support force download. Firmware drives GPIO6 and monitors GPIO1. When the arriving "message" matches sending "message", force download is enabled. Force download mode is a safety mechanism that prevents the drive from loading firmware from the media.

5.7 Flash Write Protect Signals

The write protect signals are presented in table 5-11.

Table 5-10: Write Protect Signals

Signal	Direction	Type	Description
FLASH_WP0 (GPIO6)	Output (Input During and After Reset)	Logic Output Internal Pull-Down	**Flash Write Protect 0** This active-low output serves as the Write Protect 0 (WP0_N) signal for the Flash interface. When FLASH_WP0 is active (LOW), Flash devices connected to it cannot be written. This WP signal may be used for one Flash Interface channel, or alternatively as a common WP signal for multiple channels. This pin includes a weak internal pull-down resistor. Thus, when the SF-2000 is powered on, the default state of this signal is "Flash protected." Typically Flash devices disable writes during power-on initialization. For additional security, an external pull-down resistor may be applied to this signal to ensure a "Flash protected" level during power-on initialization. This IO cell is powered by $V_{DD\_LPA\_IO}$. **Force download mode**: This is the output of the force download mode. GPIO6 is temporarily shorted to GPIO1 at reset deassertion to support force download. Firmware drives GPIO6 and monitors GPIO1. When the arriving “message” matches sending “message”, force download is enabled. Force download mode is a safety mechanism that prevents the drive from loading firmware from the media.
FLASH_WP1 (GPIO7)	Output (Input During and After Reset)	Logic Output Internal Pull-Down	**Flash Write Protect 1** See FLASH_WP0. Note that this pin is **not** associated with force download mode. This IO cell is powered by VDD_LPA_IO.

6 Flash Memory Interface

6.1 Supported Interface Standards

The SF-2000 processor supports the following Flash Memory access modes:

- ONFI-2 Access Mode
- Toggle Access Mode
- Asynchronous Access Mode

6.1.1 Asynchronous Access Modes

SF-2000 devices support the following two asynchronous Flash access modes:

- Standard asynchronous mode
- ONFI-1 asynchronous mode

The asynchronous Flash access modes represent the legacy access mechanisms.

- They are not synchronous mechanisms.
- They support standard (> 2.7V) signaling.
- They run at up to 50 MHz.

6.1.2 ONFI-2 Access Mode

ONFI-2 Flash access mode differs from the former Asynchronous mode in several important respects:

- It is a Source Synchronous transfer mode.
- It supports 1.8V signaling for greater data rates.
- It can run at up to 83 MHz (CLK signal).
- It supports dual data rate transfer, for a total of 166 MBps data rate.

ONFI-2 mode changes Flash Memory signals as compared to legacy Asynchronous mode; the list below summarizes the changes:

- Write Enable (active low) → CLK
- Read Enable (active low) → Write Enable (active high)/Read Enable (active low)
- DQS (data strobe signal) added

As a Source Synchronous transfer mechanism, ONFI-2 Mode supplies a strobe (DQS) from the device sending data. However, unlike Toggle mode, ONFI-2 uses a CLK signal for accurate control of not only data phase transfers but also of address phase, command phase, and control signaling. To save the power, since the DQS strobe is “clocking” data during write or read data transfers, the CLK signal toggling can be stopped during the write data transfer period; if stopped, it resumes near the end of the write data burst. The Read Enable and Write Enable signals are combined; depending on the operation initiated, this signal represents the active high Write Enable or the active low Read Enable. While the CLK signal is stopped during write data transfer,

the state of the combined Write Enable/Read Enable signal does not change the ongoing operation; its effect resumes when the CLK toggling resumes. DQS uses a dual-data-rate (DDR) scheme, strobing data transfer on both rising and falling edges. The DQS strobe is used only for data transfers; it is not used in the Address or Command phases, and so those transfers, being synchronized by the CLK signal, employ a single data rate (SDR) mechanism.

6.1.3 Toggle Access Mode

Similar to ONFI-2 mode, Toggle Flash access mode also differs from the former Asynchronous mode in several important respects:

- It is a Source Synchronous transfer mode.
- It supports 1.8V signaling for greater data rates.
- Its first specification allows it to run at up to 66 MHz (SF-2000 supports up to 83 MHz).
- It supports DDR transfer, for a total data rate (in MBps) of twice the interface speed.

Toggle mode changes Flash Memory signaling as compared to legacy Asynchronous mode; the following change summarizes:

- DQS (data strobe signal) added

As a Source Synchronous transfer mechanism, Toggle Mode supplies a strobe (DQS) from the device sending data. It uses this strobe signal for accurate control of data transfer. Per the definition of source synchronous strobe behavior, DQS is driven by the device sending data on the bus. DQS uses a dual-data-rate (DDR) scheme, strobing data transfer on both rising and falling edges. The DQS strobe is used only for data transfers; it is not used in the Address or Command phases, and so only data phase transfers occur at DDR rates. Address phase and Command phase transfers, which (in contrast to the ONFI-2 mode) use the legacy asynchronous signaling mechanism, run at single data rates (SDR).

6.2 Flash Interface Signals

The flash interface signals are presented in table 6-1. All flash interface signals are powered by the V_{DD_FIO} supply. For maximum speed of operation, see the trace length matching guidelines in the SF-2000 PCB design guide.

Table 6-1: Flash Interface Signals

Signal	Direction	Type	Description
FLASH_0_IO[7:0]	IO	Logic IO	**Flash Bus 0 IO** These eight bidirectional signals carry address and data between the SF-2000 and the Flash memory deployed at Flash Site 0. These pins are applicable to Asynchronous, Toggle, and ONFI-2 Flash Access modes.

FLASH_1_IO[7:0]	IO	Logic IO	**Flash Bus 1 IO** These eight bidirectional signals carry address and data between the SF-2000 and the Flash memory deployed at Flash Site 1. These pins are applicable to Asynchronous, Toggle, and ONFI-2 Flash Access modes.
FLASH_2_IO[7:0]	IO	Logic IO	**Flash Bus 2 IO** These eight bidirectional signals carry address and data between the SF-2000 and the Flash memory deployed at Flash Site 2. These pins are applicable to Asynchronous, Toggle, and ONFI-2 Flash Access modes.
FLASH_3_IO[7:0]	IO	Logic IO	**Flash Bus 3 IO** These eight bidirectional signals carry address and data between the SF-2000 and the Flash memory deployed at Flash Site 3. These pins are applicable to Asynchronous, Toggle, and ONFI-2 Flash Access modes.
FLASH_4_IO[7:0]	IO	Logic IO	**Flash Bus 4 IO** These eight bidirectional signals carry address and data between the SF-2000 and the Flash memory deployed at Flash Site 4. These pins are applicable to Asynchronous, Toggle, and ONFI-2 Flash Access modes.
FLASH_5_IO[7:0]	IO	Logic IO	**Flash Bus 5 IO** These eight bidirectional signals carry address and data between the SF-2000 and the Flash memory deployed at Flash Site 5. These pins are applicable to Asynchronous, Toggle, and ONFI-2 Flash Access modes.
FLASH_6_IO[7:0]	IO	Logic IO	**Flash Bus 6 IO** These eight bidirectional signals carry address and data between the SF-2000 and the Flash memory deployed at Flash Site 6. These pins are applicable to Asynchronous, Toggle, and ONFI-2 Flash Access modes.
FLASH_7_IO[7:0]	IO	Logic IO	**Flash Bus 7 IO** These eight bidirectional signals carry address and data between the SF-2000 and the Flash memory deployed at Flash Site 7. These pins are applicable to Asynchronous, Toggle, and ONFI-2 Flash Access modes.

FLASH_8_IO[7:0]	IO	Logic IO	**Flash Bus 8 IO** These eight bidirectional signals carry address and data between the SF-2000 and the Flash memory deployed at Flash Site 8. These pins are applicable to Asynchronous, Toggle, and ONFI-2 Flash Access modes.
FLASH_9_IO[7:0]	IO	Logic IO	**Flash Bus 9 IO** These eight bidirectional signals carry address and data between the SF-2000 and the Flash memory deployed at Flash Site 9. These pins are applicable to Asynchronous, Toggle, and ONFI-2 Flash Access modes.
FLASH_10_IO[7:0]	IO	Logic IO	**Flash Bus 10 IO** These eight bidirectional signals carry address and data between the SF-2000 and the Flash memory deployed at Flash Site 10. These pins are applicable to Asynchronous, Toggle, and ONFI-2 Flash Access modes.
FLASH_11_IO[7:0]	IO	Logic IO	**Flash Bus 11 IO** These eight bidirectional signals carry address and data between the SF-2000 and the Flash memory deployed at Flash Site 11. These pins are applicable to Asynchronous, Toggle, and ONFI-2 Flash Access modes.
FLASH_12_IO[7:0]	IO	Logic IO	**Flash Bus 12 IO** These eight bidirectional signals carry address and data between the SF-2000 and the Flash memory deployed at Flash Site 12. These pins are applicable to Asynchronous, Toggle, and ONFI-2 Flash Access modes.
FLASH_13_IO[7:0]	IO	Logic IO	**Flash Bus 13 IO** These eight bidirectional signals carry address and data between the SF-2000 and the Flash memory deployed at Flash Site 13. These pins are applicable to Asynchronous, Toggle, and ONFI-2 Flash Access modes.
FLASH_14_IO[7:0]	IO	Logic IO	**Flash Bus 14 IO** These eight bidirectional signals carry address and data between the SF-2000 and the Flash memory deployed at Flash Site 14. These pins are applicable to Asynchronous, Toggle, and ONFI-2 Flash Access modes.

FLASH_15_IO[7:0]	IO	Logic IO	**Flash Bus 15 IO** These eight bidirectional signals carry address and data between the SF-2000 and the Flash memory deployed at Flash Site 15. These pins are applicable to Asynchronous, Toggle, and ONFI-2 Flash Access modes.
FLASH_CLK [15:0] / FLASH_WEN_N [15:0]	Output	Logic Output	**Flash Clock [15:0] / Flash Write Enable [15:0]** **Flash Clock [15:0]** In ONFI-2 or Toggle Flash Access mode, these sixteen outputs serve as Flash Clock for each of the Flash interface channels. These outputs should be connected such that each one drives the CLK input of a logical Flash device (i.e., a single Flash device, or multiple Flash devices parallelled to represent a single device, or that portion of a single Flash device that represents an autonomous logical device). **Flash Write Enable [15:0]** In Asynchronous Flash Access mode, these sixteen outputs serve as active-low Write Enable signals for the Flash interface. These outputs should be connected such that each one drives a logical Flash device (i.e., a single Flash device, or multiple Flash devices parallelled to represent a single device, or that portion of a single Flash device that represents an autonomous logical device). All four WEN_N signals for a given quad of logical Flash devices are typically asserted and deasserted together.

FLASH_R/WN [15:0] / FLASH_REN_N [15:0]	Output	Logic Output	**Flash Read_Enable / Write_Enable_NOT [15:0]** In ONFI-2 or Toggle Flash Access mode, these sixteen outputs serve as combination Read Enable / active-low Write Enable signals for the Flash interface. These outputs should be connected such that each one drives a logical Flash device (i.e., a single Flash device, or multiple Flash devices parallelled to represent a single device, or that portion of a single Flash device that represents an autonomous logical device). All four R/WN signals for a given quad of logical Flash devices are typically asserted and deasserted together. **Flash Read Enable [15:0]:** In Asynchronous Flash Access mode, these sixteen outputs serve as active-low Read Enable signals for the Flash interface. These outputs should be connected such that each one drives a logical Flash device (i.e., a single Flash device, or multiple Flash devices parallelled to represent a single device, or that portion of a single Flash device that represents an autonomous logical device). All four REN_N signals for a given quad of logical Flash devices are typically asserted and deasserted together.
FLASH_DQS[15:0]	Output	Logic Output	**Flash DQ Strobe[15:0]** In ONFI-2 or Toggle Flash Access mode, these sixteen outputs serve as DQS signals for the Flash interface. These outputs should be connected such that each one drives a logical Flash device (i.e., a single Flash device, or multiple Flash devices parallelled to represent a single device, or that portion of a single Flash device that represents an autonomous logical device). In Asynchronous Flash Access mode, these sixteen pins have no meaning and may be left unconnected.

FLASH_ALE[3:0]	Output	Logic Output	**Flash Address Latch Enable [3:0]** These active-high outputs serve as Address Latch Enable (ALE) signals for the Flash interface. Each ALE signal serves the four 8-bit IO buses ("byte lanes") for one quad of logical Flash devices.
FLASH_CLE[3:0]	Output	Logic Output	**Flash Command Latch Enable [3:0]** These active-high outputs serve as Command Latch Enable (CLE) signals for the Flash interface. Each CLE signal serves the four 8-bit IO buses ("byte lanes") for one quad of logical Flash devices. Logic levels comply with the voltage supplied into the V_{DD_FIO} pins.
FLASH_CE[3:0]	Output	Logic Output	**Flash Chip Enable [3:0]** These four outputs comprise the four Chip Enable signals for Flash memory Quad 0 (i.e., Flash "byte lanes" 0 through 3).
FLASH_CE[7:4]	Output	Logic Output	**Flash Chip Enable [7:4]** These four outputs comprise the four Chip Enable signals for Flash memory Quad 1 (i.e., Flash "byte lanes" 4 through 7).
FLASH_CE[11:8]	Output	Logic Output	**Flash Chip Enable [11:8]** These four outputs comprise the four Chip Enable signals for Flash memory Quad 2 (i.e., Flash "byte lanes" 8 through 11).
FLASH_CE[15:12]	Output	Logic Output	**Flash Chip Enable [15:12]** These four outputs comprise the four Chip Enable signals for Flash memory Quad 3 (i.e., Flash "byte lanes" 12 through 15).

6.3 Flash Memory Connectivity

For information on flash memory configurations, please refer to the SF-2000 PCB Design Guide.

7 Serial ATA (SATA) Interface

The SF-2000 utilizes a SATA 3.0 compliant interface. For information about supported commands, please consult the Software Reference Manual. For recommended design parameters, see the trace length matching guidelines in the SF-2000 PCB Design Guide.

7.1 SATA Signals

The SATA signals are presented in table 7-1.

Table 7-1: SATA Signals

Signal	Direction	Type	Description
SATA_RX_P	Input	Analog Input	**Serial ATA (SATA) Receive +** This signal together with SATA_RX_N comprises the differential input pair for the SATA interface. SATA_RX_P is SATA Rx+.
SATA_RX_N	Input	Analog Input	**Serial ATA (SATA) Receive -** This signal together with SATA_RX_P comprises the differential input pair for the SATA interface. SATA_RX_N is SATA Rx-.
SATA_TX_P	Output	Analog Output	**Serial ATA (SATA) Transmit +** This signal together with SATA_TX_N comprises the differential output pair for the SATA interface. SATA_TX_P is SATA Tx+.
SATA_TX_N	Output	Analog Output	**Serial ATA (SATA) Transmit –** This signal together with SATA_TX_P comprises the differential output pair for the SATA interface. SATA_TX_N is SATA Tx-.
SATA_RREF	Input	Analog Input	**Serial ATA Reference Resistor** The Reference Resistor connection pin for the SATA PHY should be connected to this pin. Details are TBD (see reference design and SF-2000 PCB Design Guide for examples).