SiliconMotion

ZOOM FAMILY

SM2246EN

SATA Solid-State Drive Controller

Datasheet

Revision 0.3 Jan 2014

Revision History

Revision	Date	Description
0.1	Jun 25, 2013	Preliminary release
0.2	Set 10, 2013	• Updated Production Description (1.1) • Updated the signal types and descriptions: V18_PAD, GPIO1[0], GPIO1[1], GPIO1[2], GPIO1[3], GPIO1[4], GPIO2[0], GPIO2[2], and GPIO2[5] (2.2) • Updated the DC Characteristics tables (3.1)
0.3	Jan 17, 2014	• Updated the features of flash memory support (1.2) • Updated the flash signal descriptions: F0_DQS, F0_DQS#, F1_DQS, F1_DQS#, F2_DQS, F2_DQS#, F3_DQS, F3_DQS#, F0_RE, F0_RE#, F1_RE, F1_RE#, F2_RE, F2_RE#, F3_RE, F3_RE#, F0_EW#, F1_WE#, F2_WE# and F3_WE# (2.2) • Updated the DRAM and miscellaneous signal types and descriptions: DDR_ZQ, GPIO1[2], GPIO2[3], GPIO2[6], and GPIO2[7] (2.2) • Updated SMART Feature Set (4.3) • Updated minor text descriptions

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Table of Contents

List of Tables

List of Figures

1. Overview

1.1 Product Description

The SM2246EN is a high-performance SATA 6Gb/s SSD controller ideally suited for both client SSDs as well as NAND-cache drives used in performance-enhancing hybrid storage solutions for PCs, Ultrabooks and Tablets. Its ultra-low power consumption effectively extends battery life and optimizes using habit. The SM2246EN fully supports high-speed Toggle, ONFI, and Async NAND, as well as the latest generation NAND flash, enabling the realization of high capacity and highly reliable SSDs on the market.

1.2 Key Features

- Host Interface
  - Industrial Standard SATA Revision 3.1 compliant
  - Industrial Standard ATA/ATAPI-8 and ACS-2 command compliant
  - Supports SATA interface rate of 6Gb/s (backward compatible to 1.5Gb/s and 3Gb/s)
  - Native Command Queuing up to 32 commands
  - SATA Device Sleep (DevSleep)
  - Data Set Management command (TRIM)
  - Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.)
  - Supports PHY Sleep mode (CFast PHYSLP)
  - Supports 28-bit and 48-bit LBA (Logical Block Addressing) mode commands
- NAND Flash Support
  - Supports 1x/1y/2x/2y/3xnm SLC and MLC
  - Supports ONFI 3.0, Toggle 2.0 interface, and Asynchronous interface
  - Supports 1.8V/3.3V Flash I/O
  - Supports 4KB, 8KB, and 16KB page size
  - Supports 1-plane, 2-plane, and 4-plane operation
  - 4-channel flash interface supports up to 32 NAND flash devices
- DRAM Interface
  - 16-bit wide DRAM interface
  - Supports DDR2/DDR3/DDR3L
- Data Protection and Reliability
  - Supports ATA8 security feature set
  - Supports data security erase and quick erase
  - Hardware BCH ECC capable of correcting errors up to 66-bit/1KB
  - Internal data shaping technique increases data endurance
  - Software/Hardware write protect option
  - StaticDataRefresh technology ensures data integrity
  - Early weak block retirement option
  - Global wear leveling algorithm evens program/erase count and maximizes SSD lifespan

- Architecture
  - 32-bit RISC CPU
  - High-efficiency 64-bit system bus
  - Automatic sleep and wake-up mechanism to save power
  - Built-in voltage detectors for power failure protection
  - Built-in power-on reset and voltage regulators
  - Built-in temperature sensor for SSD temperature detection
  - Supports JTAG interface, UART (RS-232) interface, and I^2C interface for on-system debug
- Upgradeable Firmware
  - Supports firmware in-system programming (ISP) function for firmware upgrade
- Enhanced Security[1]
  - Real time full drive encryption with Advanced Encryption Standard (AES)
  - Trusted Computing Group (TCG) Opal protocol
  - Hardware SHA 256 and True Random Number Generator (TRNG)
- High Performance
  - Sequential Read: 530 MB/s (synchronous mode)
  - Sequential Write: 410 MB/s (synchronous mode)
- Operating Temperature
  - Commercial Grade: 0°C ~ 70°C
  - Industrial Grade: -40°C ~ +85°C
- Package
  - 288-ball TFBGA
  - Lead-free and RoHS compliant

[1] The Enhanced Security firmware support will be available in the future.

1.3 Functional Description

Host Interface

The high-speed SATA interface is compliant with SATA Revision 3.1 and ATA-8 ACS-2 specifications, and supports CFast PHYSLP and SATA DEVSLP to greatly save power consumption.

Flash Interface and Data Transfer

The flash interface enables 2-way and 4-way interleaving for a multi-bank NAND flash connection to obtain optimal performance. The SM2246EN uses a superior DMA technology to transfer data between the host and the NAND flash interface. The DMA technology transfers data at a very high rate in both directions (read and write) and in doing so, effectively decreases the loading of micro processor.

Flash Memory Support and Error Management

The SM2246EN fully supports high-speed Toggle, ONFI, and legacy Asynchronous NAND. The hardware Error Correction Coding (ECC) engine executes parity generation and error detection/ correction features, and enhances decoding throughput and data reliability. With multi-mode correction capability up to 66 bits, the powerful ECC engine is able to support the latest generation NAND.

Data Security

Security commands can be used to lock and unlock the drive by password or through a hardware switch. For those users who require the highest level of security, the SM2246EN provides an enhanced data security[1] option. Incorporated various data management techniques such as AES and TCG Opal, full data encryption eventually achieves confidential and secure data protection.

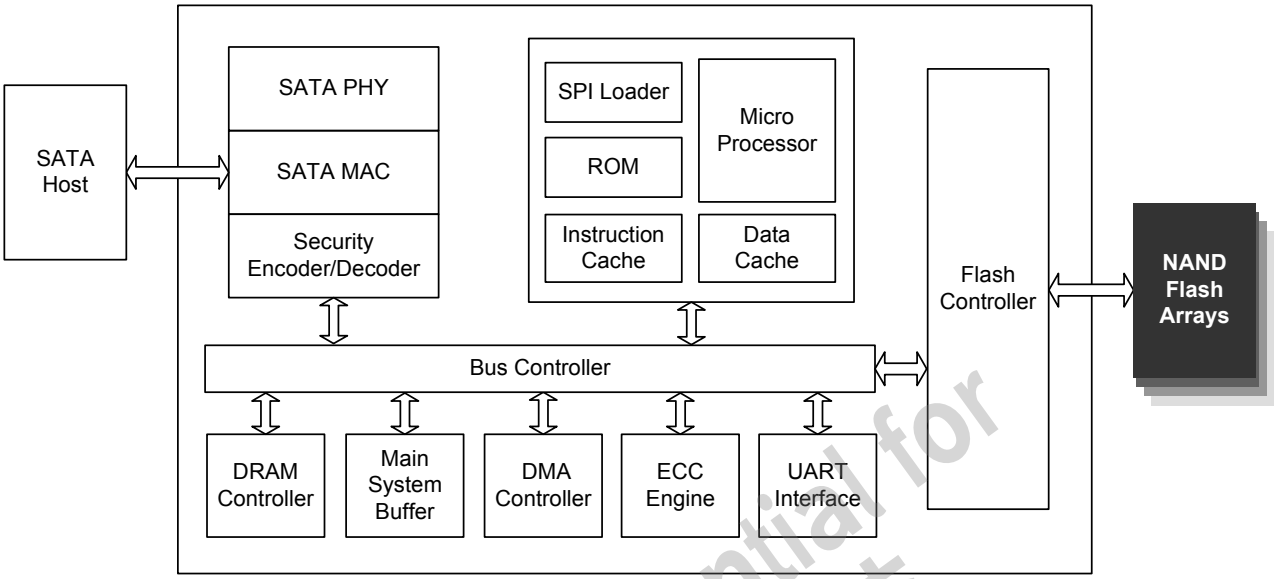
SMART

The SM2246EN supports SMART commands that allow users to read spare and bad block information. The users can thus evaluate drive health at run time and receive an early warning before the drive life ends.

[1] The Enhanced Security firmware support will be available in the future.

1.4 Block Diagram

Figure 1: SM2246EN Block Diagram



2. Signal Descriptions

2.1 Ball Assignments

Figure 2: 288-Ball TFBGA Assignments (Top View – Balls Down)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A		TX0_N	TX0_P	PHY_GD	RX0_N	RX0_P	PHY_GD	DDR_CS0#	DDR_CKE0	DDR_A9	DDR_CK#	DDR_A12	DDR_A1	DDR_WE#	DDR_VREF	DDR_ZQ	DDR_DQ2
B	RESREF	PHY_GD	PHY_GD	VCCK	PHY_GD	PHY_GD	VCCK	DDR_BA1	DDR_A4	DDR_A7	DDR_CK	DDR_A13	DDR_A2	DDR_A10	DDR_ODT1	DDR_DML	DDR_DQ3
C	V12A_PAD	PHY_VPH	PHY_VPH	PHY_VPTX	PHY_VP	VCCK	VCCK	DDR_CKE1	DDR_BA0	DDR_A6	DDR_A8	DDR_A14	DDR_A3	DDR_RAS#	DDR_VDDQ	DDR_DQ0	DDR_DQ1
D	V12A_PAD	V18_PAD	V18_PAD	VCCAH	VCCK	VCCK	VCCK	DDR_CS1#	DDR_CAS#	DDR_A0	DDR_A15	DDR_A11	DDR_BA2	DDR_RST#	DDR_ODT0	VSSFQ	DDR_DQSL#
E	XIN	VDTD_VIN	VDTF_VIN	VCCAH	VCCK	VCCK	VCCK	VCCK	VCCK	DDR_A5	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR_DQ13	DDR_DQ5	DDR_DQ4	DDR_DQSL
F	XOUT	VGNDA	CRY_VDD33	EXCLK	TEST2	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	VSSFQ	VSSFQ	VSSFQ	DDR_DQ11	DDR_DQ7	DDR_DQ6
G	VCC_5V	CRY_VSS33	GPIO2[0]	GPIO2[1]	CGND	CGND	CGND	CGND	CGND	VSSFQ	VSSFQ	VSSFQ	DDR_DQ14	DDR_DQ8	DDR_DQ12	DDR_DMU	DDR_VDDQ
H	VCCGQ	VCCGQ	GPIO2[3]	GPIO2[5]	GPIO1[1]	CGND	CGND	CGND	CGND	CGND	VSSFQ	VSSFQ	DDR_DQ15	DDR_DQ10	DDR_DQ9	DDR_DQSU	DDR_DQSU#
J	TEST0	GPIO2[4]	GPIO1[2]	GPIO1[3]	GPIO1[5]	VSSFQ	VSSFQ	CGND	CGND	VSSFQ	VSSFQ	VSSFQ	F3_DQ7	F3_DQ1	F3_DQ4	F3_DQ6	F3_DQ5
K	GPIO2[2]	GPIO1[4]	SPI_CLK	GPIO1[7]	GPIO0[1]	VSSFQ	VSSFQ	VSSFQ	VSSFQ	VSSFQ	VSSFQ	VCCFQ	VCCFQ	F3_DQ2	F3_DQ0	F3_DQS	F3_DQS#
L	GPIO2[6]	SPI_CS#	J_TDO	SPI_MOSI	CGND	VSSFQ	VSSFQ	VSSFQ	VSSFQ	VSSFQ	VCCFQ	VCCFQ	F1_DQ4	F3_ALE	F3_DQ3	F3_RE#	F3_RE
M	EXRST#	SPI_MISO	F0_CE6#	J_TRST#	I2C_SCL	VCCFQ	VCCFQ	VCCFQ	VCCFQ	VCCFQ	VCCFQ	VCCFQ	F1_DQ2	F2_DQ1	F3_CLE	FSH_VREF	F3_WE#
N	TEST1	I2C_SDA	F0_CE4#	J_TMS	F0_CE2#	F1_CE7#	F2_CE4#	F3_CE2#	F3_CE5#	FSH_R/B#	F0_DQ1	F0_DQ2	VCCFQ	F1_DQ6	F2_DQ6	F2_DQ5	F2_DQ7
P	GPIO2[7]	J_TCK	F1_CE5#	F0_CE5#	F1_CE1#	F2_CE1#	F2_CE2#	F3_CE3#	FSH_WP#	F0_ALE	F0_DQ6	F0_DQ7	F1_ALE	F1_DQ5	F2_DQ2	F2_DQ4	F2_DQS#
R	GPIO1[0]	J_TDI	F1_CE2#	F0_CE7#	F2_CE0#	F2_CE5#	F2_CE7#	F3_CE6#	F0_CLE	F0_DQ3	F0_DQ5	F1_CLE	F1_DQ1	F1_DQ3	F2_CLE	F2_DQ0	F2_DQS
T	GPIO1[6]	F0_CE1#	F0_CE3#	F1_CE0#	F1_CE6#	F2_CE6#	F3_CE1#	F3_CE7#	F0_WE#	F0_RE	F0_DQS	F1_DQ0	F1_RE	F1_DQS	F2_WE#	F2_ALE	F2_RE#
U	GPIO0[0]	F0_CE0#	F1_CE3#	F1_CE4#	F2_CE3#	F3_CE0#	F3_CE4#	F0_DQ0	F0_DQ4	F0_RE#	F0_DQS#	F1_WE#	F1_RE#	F1_DQS#	F1_DQ7	F2_DQ3	F2_RE

2.2 Signal Description Table

Table 1: Flash Interface Signals

Signal	Ball No.	Type	Description
F0_DQ0	U8	I/O	Flash data bus connected to flash channel 0.
F0_DQ1	N11		
F0_DQ2	N12		
F0_DQ3	R10		
F0_DQ4	U9		
F0_DQ5	R11		
F0_DQ6	P11		
F0_DQ7	P12		
F1_DQ0	T12	I/O	Flash data bus connected to flash channel 1.
F1_DQ1	R13		
F1_DQ2	M13		
F1_DQ3	R14		
F1_DQ4	L13		
F1_DQ5	P14		
F1_DQ6	N14		
F1_DQ7	U15		
F2_DQ0	R16	I/O	Flash data bus connected to flash channel 2.
F2_DQ1	M14		
F2_DQ2	P15		
F2_DQ3	U16		
F2_DQ4	P16		
F2_DQ5	N16		
F2_DQ6	N15		
F2_DQ7	N17		
F3_DQ0	K15	I/O	Flash data bus connected to flash channel 3.
F3_DQ1	J14		
F3_DQ2	K14		
F3_DQ3	L15		
F3_DQ4	J15		
F3_DQ5	J17		
F3_DQ6	J16		
F3_DQ7	J13		

Signal	Ball No.	Type	Description
F0_ALE	P10	O	Flash address latch enable.
F1_ALE	P13		
F2_ALE	T16		
F3_ALE	L14		
F0_CLE	R9	O	Flash command latch enable.
F1_CLE	R12		
F2_CLE	R15		
F3_CLE	M15		
F0_CE0#	U2	I/O PU[1]	Flash chip enable for flash channel 0.
F0_CE1#	T2		
F0_CE2#	N5		
F0_CE3#	T3		
F0_CE4#	N3		
F0_CE5#	P4		
F0_CE6#	M3		
F0_CE7#	R4		
F1_CE0#	T4	I/O PU[1]	Flash chip enable for flash channel 1.
F1_CE1#	P5		
F1_CE2#	R3		
F1_CE3#	U3		
F1_CE4#	U4		
F1_CE5#	P3		
F1_CE6#	T5		
F1_CE7#	N6		
F2_CE0#	R5	I/O PU[1]	Flash chip enable for flash channel 2.
F2_CE1#	P6		
F2_CE2#	P7		
F2_CE3#	U5		
F2_CE4#	N7		
F2_CE5#	R6		
F2_CE6#	T6		
F2_CE7#	R7		

Signal	Ball No.	Type	Description
F3_CE0#	U6	I/O PU[1]	Flash chip enable for flash channel 3.
F3_CE1#	T7		
F3_CE2#	N8		
F3_CE3#	P8		
F3_CE4#	U7		
F3_CE5#	N9		
F3_CE6#	R8		
F3_CE7#	T8		
F0_DQS	T11	I/O	Fx_DQS/Fx_DQS#: Flash data strobe/Flash data strobe complement. • For SDR access mode, these signals are not used (no connect). • For NV-DDR and Toggle DDR 1.0 access modes, the Fx_DQS indicates the data valid window. Input with read data, output with write data. Edge-aligned with read data, centered in write data. • In NV-DDR2 and Toggle DDR 2.0 access modes, the Fx_DQS indicates the data valid window. Input with read data, output with write data. Edge-aligned with read data, centered in write data. The Fx_DQS is paired with differential signal Fx_DQS# to provide differential pair signaling to the system during reads and writes (e.g., F0_DQS and F0_DQS#).
F0_DQS#	U11		
F1_DQS	T14		
F1_DQS#	U14		
F2_DQS	R17		
F2_DQS#	P17		
F3_DQS	K16		
F3_DQS#	K17		
F0_RE	T10	O	Fx_RE/Fx_RE#: Flash read enable/Flash read enable complement. • For SDR access mode, the Fx_RE# enables serial data output. • For NV-DDR2 and Toggle DDR 1.0/2.0 access modes, the Fx_RE# signal is the serial data-out control, and when active, drives the data onto the DQ buses. Data is valid after tDQSRE of rising edge and falling edge of Fx_RE#, which also increments the internal column address counter by each one. The read enable Fx_RE is paired with differential signal Fx_RE# (only in NV-DDR2 and Toggle DDR 2.0 modes) to provide differential pair signaling to the system during reads. Fx_W/R#: Write/read direction control • For NV-DDR access mode, when this signal is latched high, the controller is driving the DQ bus and DQS (data is being written to the bus). When this signal is latched low, the NAND flash is driving the DQ bus and DQS (data is being read from the bus). (This signal shares the same pin with Fx_RE#.)
F0_RE#/ F0_W/R#	U10		
F1_RE	T13		
F1_RE#/ F1_W/R#	U13		
F2_RE	U17		
F2_RE#/ F2_W/R#	T17		
F3_RE	L17		
F3_RE#/ F3_W/R#	L16		

Signal	Ball No.	Type	Description
F0_WE#/ F0_CLK	T9	O	Fx_WE#: Flash write enable. • For SDR access mode, the write enable signal controls the latching of output data. Data, commands, and addresses are latched on the rising edge of Fx_WE#. • For NV-DDR2 and Toggle DDR 1.0/2.0 access modes, this signal controls writes to the DQ bus. Commands and addresses are latched on the rising edge of the WE pulse. Fx_CLK: Clock. • For NV-DDR access mode, this signal is used as the clock. (This signal shares the same pin with Fx_WE#.)
F1_WE#/ F1_CLK	U12		
F2_WE#/ F2_CLK	T15		
F3_WE#/ F3_CLK	M17		
FSH_WP#	P9	O	Flash write protect signal directly connected to the flash memory write protect signal.
FSH_R/B#	N10	I	Flash ready/busy signals indicating the state, ready or busy of flash memory.

Table 2: DRAM Signals

Signal	Ball No.	Type	Description
DDR_DQ0	C16	I/O	DRAM data bits. Bidirectional data bus for the x16 configuration.
DDR_DQ1	C17		
DDR_DQ2	A17		
DDR_DQ3	B17		
DDR_DQ4	E16		
DDR_DQ5	E15		
DDR_DQ6	F17		
DDR_DQ7	F16		
DDR_DQ8	G14		
DDR_DQ9	H15		
DDR_DQ10	H14		
DDR_DQ11	F15		
DDR_DQ12	G15		
DDR_DQ13	E14		
DDR_DQ14	G13		
DDR_DQ15	H13		

Signal	Ball No.	Type	Description
DDR_A0	D10	O	DRAM address. DDR_A[15:0] provide the row address for Active commands, and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank.
DDR_A1	A13		
DDR_A2	B13		
DDR_A3	C13		
DDR_A4	B9		
DDR_A5	E10		
DDR_A6	C10		
DDR_A7	B10		
DDR_A8	C11		
DDR_A9	A10		
DDR_A10	B14		
DDR_A11	D12		
DDR_A12	A12		
DDR_A13	B12		
DDR_A14	C12		
DDR_A15	D11		
DDR_BA0	C9	O	DRAM bank address. DDR_BA[2:0] define the bank to which an Active, Read, Write or Precharge command is being applied.
DDR_BA1	B8		
DDR_BA2	D13		
DDR_CKE0	A9	O	DRAM clock enable.
DDR_CKE1	C8		
DDR_RST#	D14	O	DRAM reset signal. DDR_RST# is an active Low CMOS input.
DDR_ZQ	A16	I	External reference for output drive calibration (for DDR3 only).
DDR_CS0#	A8	O	Chip select. DDR_CSx# enables (registered Low) and disables (registered High) the command decoder. All commands are masked when DDR_CSx# is registered High. The DDR_CSx# provides for external rank selection on systems with multiple ranks. The DDR_CSx# is considered part of the command code.
DDR_CS1#	D8		
DDR_ODT0	D15	O	On die termination. DDR_ODTx enables (registered High) and disables (registered Low) termination resistance internal to the DDR3 DRAM. When enabled in normal operation, this signal is applied to each of the following balls: DDR_DQ[15:0], DDR_DQSL, DDR_DQSL#, DDR_DQSU, DDR_DQSU#, DDR_DML and DDR_DMU.
DDR_ODT1	B15		
DDR_CK	B11	O	Differential clock output pair.
DDR_CK#	A11		

Signal	Ball No.	Type	Description
DDR_DQSL	E17	I/O	Data strobe - lower byte. Input with read data, output with write data. Edge-aligned with read data, center-aligned to write data. The data strobe DDR_DQSL and DDR_DQSU are paired with differential signals DDR_DQSL# and DDR_DQSU#, respectively, to provide differential pair signaling to the system during reads and writes. For the x16, DDR_DQSL and DDR_DQSL# corresponds to the data on DDR_DQ[7:0].
DDR_DQSL#	D17		
DDR_DQSU	H16	I/O	Data strobe - upper byte. Input with read data, output with write data. Edge-aligned with read data, center-aligned to write data. The data strobe DDR_DQSL and DDR_DQSU are paired with differential signals DDR_DQSL# and DDR_DQSU#, respectively, to provide differential pair signaling to the system during reads and writes. For the x16, DDR_DQSU and DDR_DQSU# corresponds to the data on DDR_DQ[15:8].
DDR_DQSU#	H17		
DDR_DML	B16	O	Output data mask. Output data is masked when the DDR_DML (lower byte) or the DDR_DMU (upper byte) is sampled High along with that output data during a write access.
DDR_DMU	G16		
DDR_RAS#	C14	O	Row address select. Command inputs: DDR_RAS#, DDR_CAS# and DDR_WE# (along with DDR_CS0# or DDR_CS1#) define the command being entered.
DDR_CAS#	D9	O	Column address select. Command inputs: DDR_RAS#, DDR_CAS# and DDR_WE# (along with DDR_CS0# or DDR_CS1#) define the command being entered.
DDR_WE#	A14	O	Write enable. Command inputs: DDR_RAS#, DDR_CAS# and DDR_WE# (along with DDR_CS0# or DDR_CS1#) define the command being entered.

Table 3: SATA Interface Signals

Signal	Ball No.	Type	Description
RX0_P	A6	I	Positive input of receiver differential signal.
RX0_N	A5	I	Negative input of receiver differential signal.
TX0_P	A3	O	Positive output of transmitter differential signal.
TX0_N	A2	O	Negative output of transmitter differential signal.

Table 4: Power Signals

Signal	Ball No.	Type	Description
DDR_VDDQ	C15, E11, E12, E13, F6, F7, F8, F9, F10, F11, G17	PWR	Power supply for external DRAM. DDR2: 1.8V. DDR3: 1.5V. DDR3L: 1.35V.
DDR_VREF	A15	PWR	External DRAM reference voltage (0.5 x DDR_VDDQ).
VCCK	B4, B7, C6, C7, D5, D6, D7, E5, E6, E7, E8, E9	PWR	Power supply 1.2V for core logic.
VCCGQ	H1, H2	PWR	Power supply for general I/O.
PHY_VP	C5	PWR	Power supply 1.2V for SATA PHY Rx.
PHY_VPTX	C4	PWR	Power supply 1.2V for SATA PHY Tx.
PHY_VPH	C2, C3	PWR	Power supply 3.3V for SATA PHY.
RESREF	B1	I	Reference resistor connection for SATA PHY.
VCCFQ	K12, K13, L11, L12, M6, M7, M8, M9, M10, M11, M12, N13	PWR	Power supply 3.3V/1.8V for flash I/O.
FSH_VREF	M16	PWR	External flash reference voltage (0.5 x VCCFQ).
V12A_PAD	C1, D1	PWR	Analog power supply 1.2V.
VCCAH	D4, E4	PWR	Analog power supply 3.3V for regulator.
CRY_VDD33	F3	PWR	Analog power supply 3.3V for crystal cell.
VDTD_VIN	E2	PWR	Voltage detector input for DRAM power.
VDTF_VIN	E3	PWR	Voltage detector input for flash power.
VCC_5V	G1	PWR	Voltage detector input for host power.
V18_PAD	D2, D3	PWR	Voltage regulator 1.8V output.
CGND	G5, G6, G7, G8, G9, H6, H7, H8, H9, H10, J8, J9, L5	GND	Core ground.

Signal	Ball No.	Type	Description
VSSFQ	D16, F12, F13, F14, G10, G11, G12, H11, H12, J6, J7, J10, J11, J12, K6, K7, K8, K9, K10, K11, L6, L7, L8, L9, L10	GND	Ground for GPIO, DDR DRAM I/O and flash I/O.
CRY_VSS33	G2	GND	Analog ground for crystal.
VGNDA	F2	GND	Analog ground for regulator.
PHY_GD	A4, A7, B2, B3, B5, B6	GND	Analog ground for SATA PHY.

Table 5: Miscellaneous Signals

Signal	Ball No.	Type	Description
J_TRST#	M4	I PU	JTAG test reset.
J_TMS	N4	I PU	JTAG test mode select.
J_TDI	R2	I PU	JTAG test data input.
J_TDO	L3	O PD	JTAG test data output.
J_TCK	P2	I PU	JTAG test clock.
SPI_CS#	L2	O	SPI select enable.
SPI_CLK	K3	O	SPI clock input.
SPI_MISO	M2	I	SPI data input.
SPI_MOSI	L4	O	SPI data output.
I^2C_SCL	M5	I/O PU	I^2C serial bus clock.
I^2C_SDA	N2	I/O PU	I^2C serial bus data.
GPIO0[0]	U1	I/O PD[1]	Invert SATA Rx signal (High active).
GPIO0[1]	K5	I/O PD[1]	Invert SATA Tx signal (High active).
GPIO1[0]	R1	I/O PU[1]	This signal drives LED indicator for SSD operation. The LED blinks during read/write operations.
GPIO1[1]	H5	I/O PU[1]	Hardware write protect (Low active).

Signal	Ball No.	Type	Description
GPIO1[2]	J3	I/O PU[1]	• This signal can be used to drive LED indicator for the SATA link status between the device and the host (only supported in the CFast form factor). • This signal shares the same pin as UART Rx output.
GPIO1[3]	J4	I/O PU[1]	• Force the device to run ROM code (Low active, for debug only). • This signal shares the same pin as UART Tx output.
GPIO1[4]	K2	I/O PU[1]	DEVSLP (device sleep mode) enable.
GPIO1[5]	J5	I/O PD[1]	Quick erase control (Low active).
GPIO1[6]	T1	I/O PD[1]	Reserved. Do not connect (N.C.) for normal operation.
GPIO1[7]	K4	I/O PD[1]	Reserved. Do not connect (N.C.) for normal operation.
GPIO2[0]	G3	I/O PD[1]	Set the driving strength of flash I/O (High active). This setting is low by default.
GPIO2[1]	G4	I/O PD[1]	GPIO2[1] is used to enable AES function (High active). When the encryption is not enabled, this signal is reserved.
GPIO2[2]	K1	I/O PD[1]	NAND flash power supply. "**0**": Supports 3.3V flash memory. "**1**": Supports 1.8V flash memory.
GPIO2[3]	H3	I/O PD[1]	Toggle NAND configuration. "**0**": Legacy. "**1**": Native Toggle NAND.
GPIO2[4]	J2	I/O PD[1]	Reserved. Do not connect (N.C.) for normal operation.
GPIO2[5]	H4	I/O PU[1]	This signal determines the operation mode. "**0**": Reliable mode. "**1**": Normal mode (default).
GPIO2[6]	L1	I/O PU[1]	GPIO2[6] is used to enable power supply (MOS switch) for DRAM.
GPIO2[7]	P1	I/O PU[1]	Card detect in.
XIN	E1	I	50MHz external crystal input.
XOUT	F1	O	50MHz external crystal output.
EXRST#	M1	I PU	External/Test Reset input. Tie high for normal operation.
EXCLK	F4	I PD	External/Test Clock input. Tie low for normal operation.

Signal	Ball No.	Type	Description
TEST0	J1	I PD	Test signal. Tie to ground for normal operation.
TEST1	N1	I PD	Test signal. Tie to ground for normal operation.
TEST2	F5	I PD	Test signal. Tie to ground for normal operation.

Notes: The following describes the signal types used in this section.
1. PU: Internal fixed pull-up
2. PU[1]: Internal pull-up controlled by firmware
3. PD: Internal fixed pull-down
4. PD[1]: Internal pull-down controlled by firmware

3. Electrical Characteristics

3.1 DC Characteristics

Table 6: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Core Power Supply	VCCK	1.08	1.2	1.32	V
DDR2 Power Supply	DDR_VDDQ	1.7	1.8	1.9	V
DDR3 Power Supply	DDR_VDDQ	1.43	1.5	1.57	V
DDR3L Power Supply	DDR_VDDQ	1.29	1.35	1.45	V
DRAM Reference Voltage	DDR_VREF	0.49 x DDR_VDDQ	0.5 x DDR_VDDQ	0.51 x DDR_VDDQ	V
I/O Pad Power Supply	VCCGQ	2.7	3.3	3.6	V
Flash I/O Power Supply	VCCFQ	1.7	1.8	1.95	V
		2.7	3.3	3.6	V
Flash I/O Reference Voltage	FSH_VREF	0.5 x VCCFQ			V
Analog Power Supply	V12A_PAD	1.08	1.2	1.32	V
	VCCAH	2.7	3.3	3.6	V
	CRY_VDD33	2.7	3.3	3.6	V
SATA PHY Power Supply	PHY_VPH	3.07	3.3	3.63	V
	PHY_VPTX	1.12	1.2	1.32	V
	PHY_VP	1.12	1.2	1.32	V

Table 7: Operating Temperature

Controller Version	Min	Max	Unit
Commercial	0	70	°C
Industrial	-40	+85	°C

Table 8: General DC Characteristics for 3.3V I/O Interface

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Supply Voltage (V_{IO})	VCCGQ	2.6	3.3	3.6	V	
	VCCFQ	2.6	3.3	3.6	V	
High Level Output Voltage	V_{OH}	0.9 x V_{IO}			V	
Low Level Output Voltage	V_{OL}			0.1 x V_{IO}	V	
High Level Input Voltage	V_{IH}		1.65		V	Non-schmitt trigger
		0.8 x V_{IO}		V_{IO} + 0.3	V	Schmitt trigger[1]
Low Level Input Voltage	V_{IL}		1.65		V	Non-schmitt trigger
		V_{SS} - 0.3		0.2 x V_{IO}	V	Schmitt trigger[1]
Pull-up Resistance	R_{PU}	21	70	119	kΩ	
Pull-down Resistance	R_{PD}	21	70	119	kΩ	

Table 9: General DC Characteristics for 1.8V I/O Interface

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Supply Voltage (V_{IO})	VCCFQ	1.6	1.8	2.0	V	
High Level Output Voltage	V_{OH}	0.9 x V_{IO}			V	
Low Level Output Voltage	V_{OL}			0.1 x V_{IO}	V	
High Level Input Voltage	V_{IH}		0.90		V	Non-schmitt trigger
		0.8 x V_{IO}		V_{IO} + 0.3	V	Schmitt trigger[1]
Low Level Input Voltage	V_{IL}		0.90		V	Non-schmitt trigger
		V_{SS} - 0.3		0.2 x V_{IO}	V	Schmitt trigger[1]
Pull-up Resistance	R_{PU}	47.7	159	270.3	kΩ	
Pull-down Resistance	R_{PD}	44.1	147	249.9	kΩ	

Note[1]: Applies to the EXRST# signal.

Table 10: Power-on Reset

Parameter		Min	Typ	Max	Unit
Detect Voltage	VRR		0.93		V
	VFR		0.76		V
Delay Time	Rise	2.12	2.62	3.27	µs
	Fall	4.06	5.32	6.96	µs

Table 11: Host Voltage Detection

Parameter		Min	Max	Unit
Detect Voltage	VRR		4.14	V
	VFR		4.0	V
Delay Time	Rise	1.5	4.5	µs
	Fall	0.5	1.5	µs

Table 12: DRAM Voltage Detection

Parameter		Min	Max	Unit
Detect Voltage (DDR2)	VRR	1.6	1.8	V
	VFR	1.5	1.7	V
Detect Voltage (DDR3)	VRR	1.3	1.5	V
	VFR	1.2	1.4	V
Delay Time	Rise	2.5	3.0	µs
	Fall	0.9	1.5	µs

Table 13: Flash Voltage Detection

Parameter		Min	Max	Unit
Detect Voltage (3.3V)	VRR	2.7	2.9	V
	VFR	2.6	2.8	V
Detect Voltage (1.8V)	VRR	1.6	1.8	V
	VFR	1.5	1.7	V
Delay Time	Rise	2.5	3.0	µs
	Fall	0.9	1.5	µs

Table 14: PLL

Parameter	Min	Typ	Max	Unit	Condition
Output Clock	12.5		400	MHz	
Lock-in Time		101.2		µs	
Duty Cycle	45		55	%	
Jitter			10%	UI[1]	
Disable, Power-down Current (1.2V)			1	µA	Regulator Disable
Operating Current (1.2V)			2	mA	f_{CLK} = 400 MHz

Note[1]: UI = output frequency.

3.2 Flash Interface AC Characteristics

3.2.1 Legacy NAND (SDR) Interface

Table 15: Flash Interface AC Characteristics for Legacy NAND

Parameter	Symbol	Min	Max	Unit
CE# Setup Time	tCS	15.0		ns
CE# Hold Time	tCH	5.0		ns
CLE Setup Time	tCLS	10.0		ns
CLE Hold Time	tCLH	5.0		ns
ALE Setup Time	tALS	10.0		ns
ALE Hold Time	tALH	5.0		ns
Write Cycle Time	tWC	20.0		ns
WE# Pulse Width	tWP	10.0		ns
WE# High Hold Time	tWH	7.0		ns
Write Data Setup Time	tDS	7.0		ns
Write Data Hold Time	tDH	5.0		ns
Read Cycle Time	tRC	20.0		ns
Ready to RE# Low	tRR	20.0		ns
RE# Pulse Width	tRP	10.0		ns
RE# High Hold Time	tREH	7.0		ns

Figure 3: Command Latch Timing

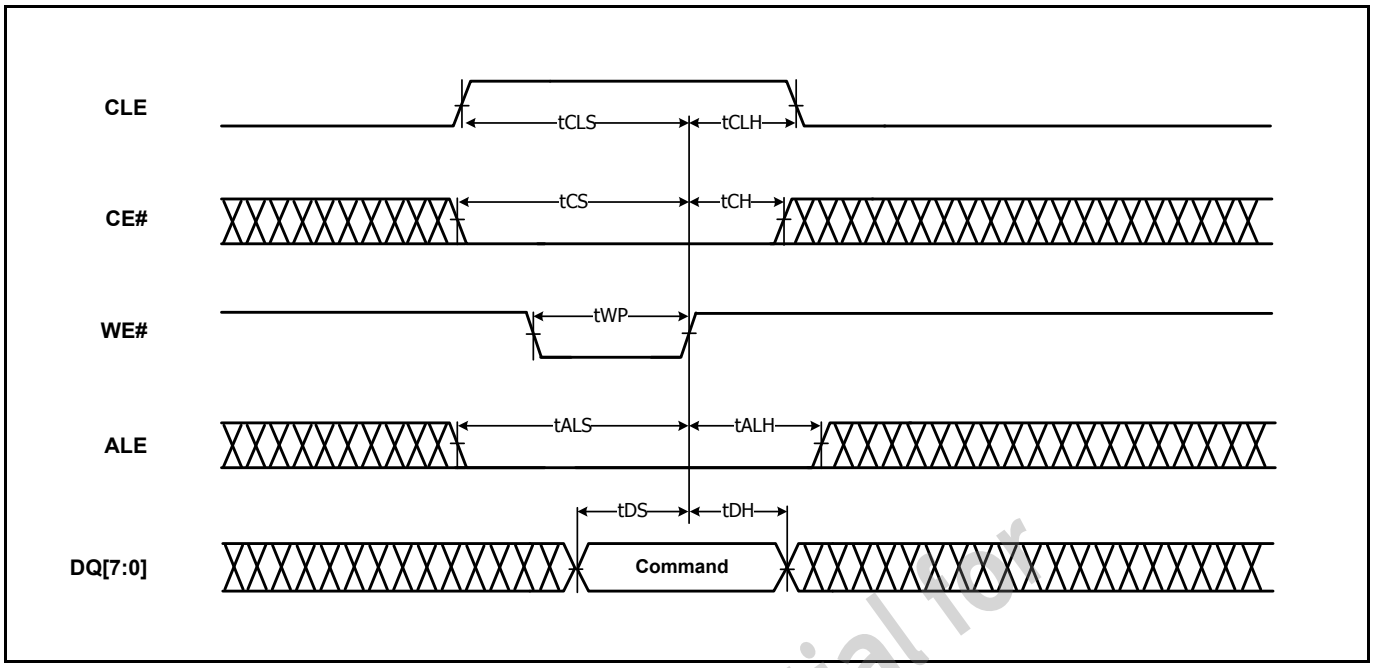


Figure 4: Address Latch Timing

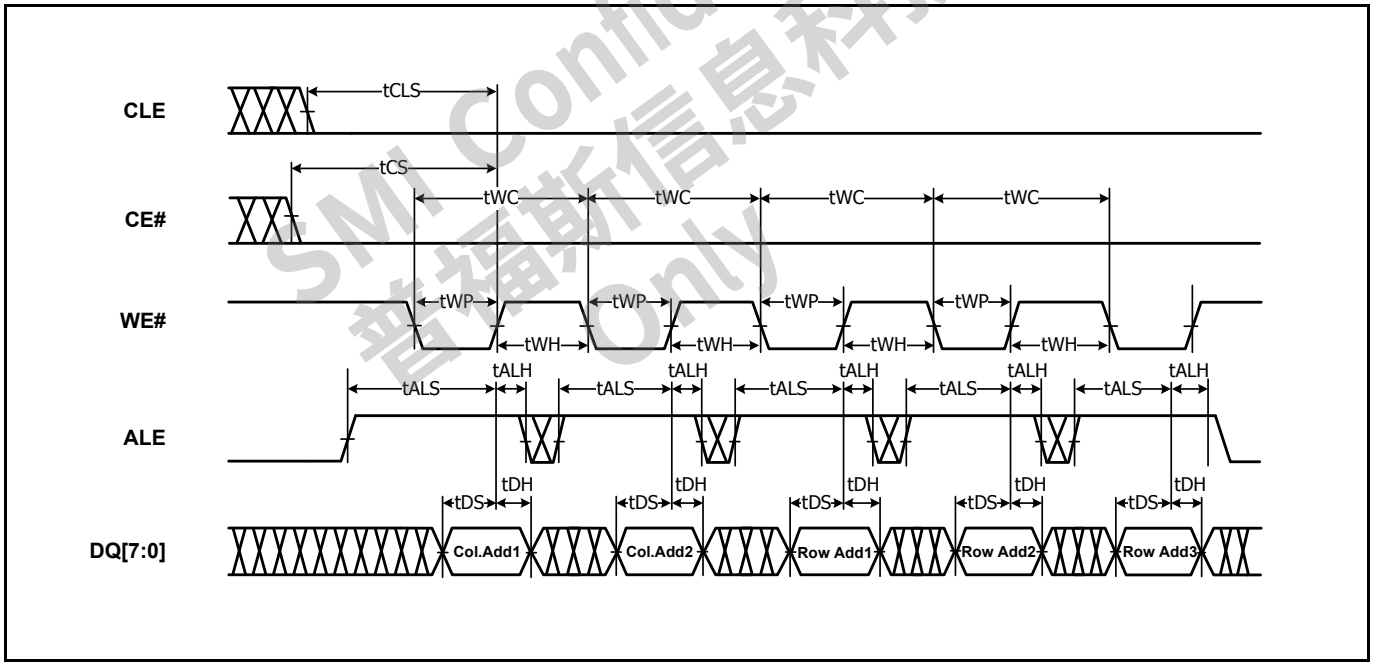


Figure 5: Data Output (Write) Cycle Timing

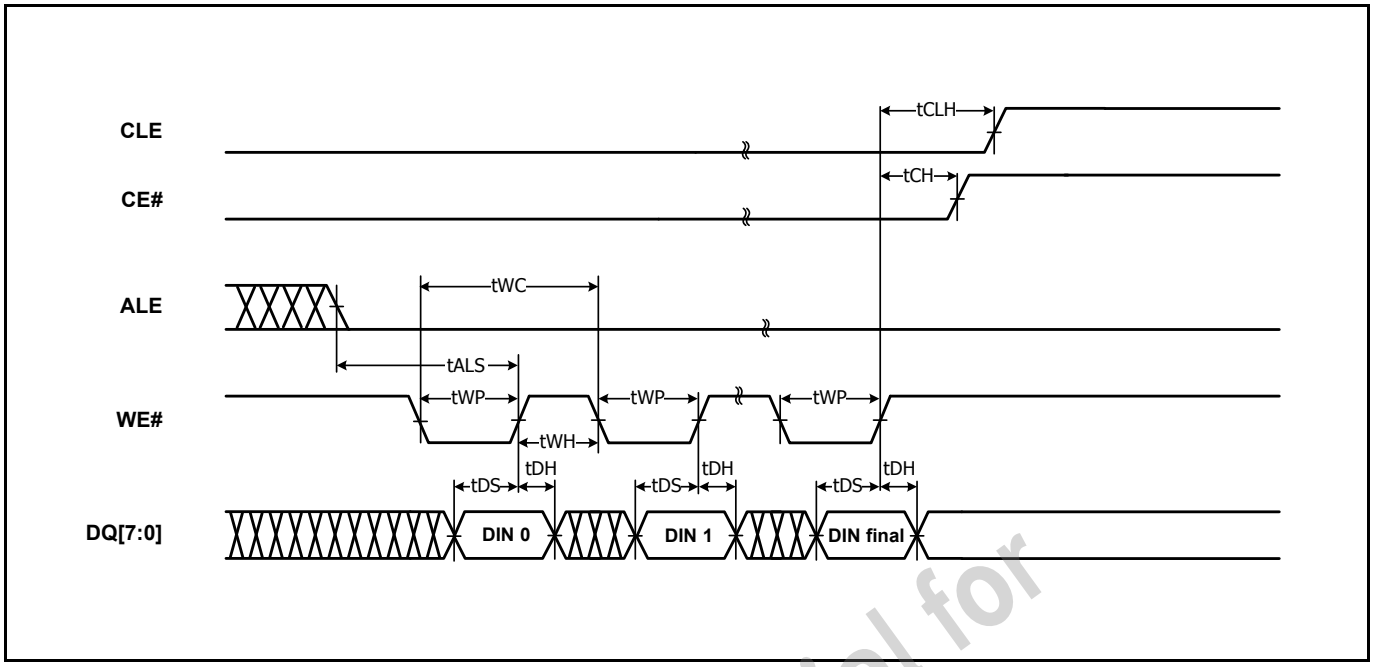
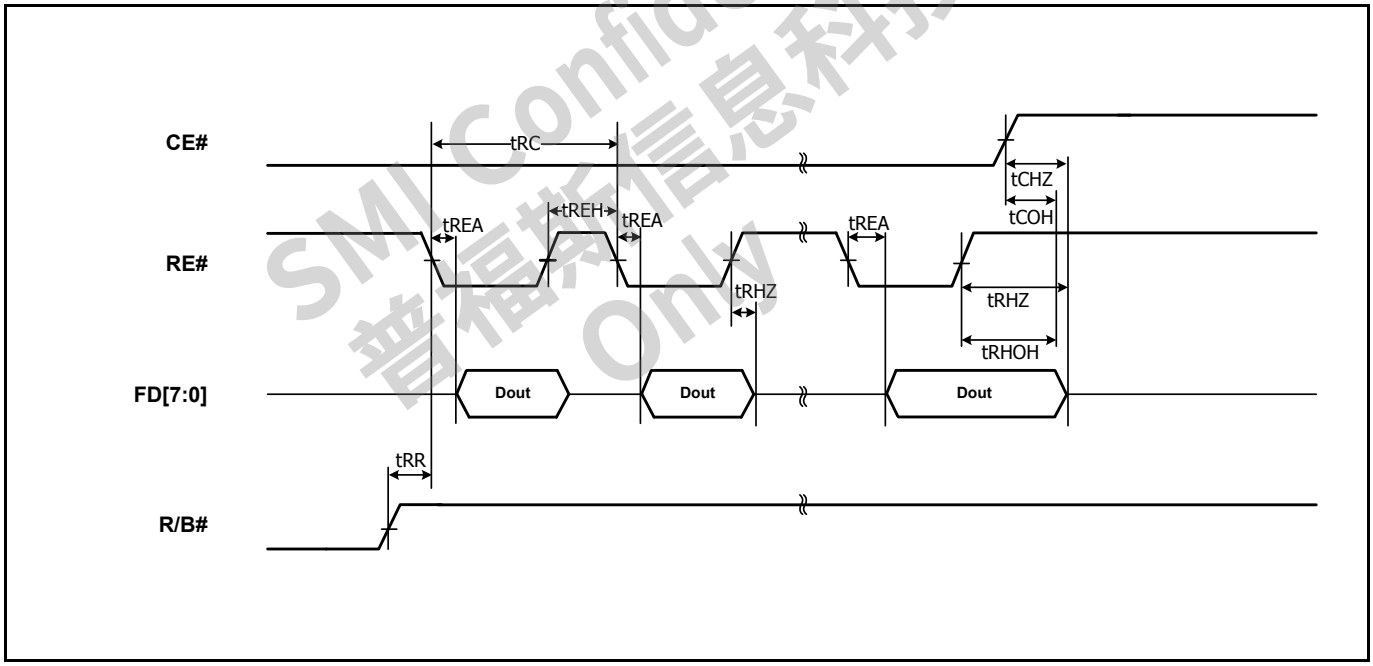


Figure 6: Data Input (Read) Cycle Timing



3.2.2 NV-DDR Interface

Table 16: Flash Interface AC Characteristics for NV-DDR

Parameter	Symbol	Min	Max	Unit
CLK Cycle Time	tCK	10.0		ns
CLK Low Time	tCKL	0.43	0.57	tCK
CLK High Time	tCKH	0.43	0.57	tCK
CE# Setup Time	tCS	15.0		ns
CE# Hold Time	tCH	2.0		ns
CLE, ALE, W/R# Setup Time	tCALS	2.0		ns
CLE, ALE, W/R# Hold Time	tCALH	2.0		ns
Command & Address DQ Setup Time	tCAS	2.0		ns
Command & Address DQ Hold Time	tCAH	2.0		ns
Data Output (Write) Setup Time	tDS	0.9		ns
Data Output (Write) Hold Time	tDH	0.9		ns
DQS Falling Edge to CLK Rising Setup Time	tDSS	0.2		tCK
DQS Falling Edge to CLK Rising Hold Time	tDSH	0.2		tCK
DQS Low Pulse Width	tDQSL	0.4	0.6	tCK
DQS High Pulse Width	tDQSH	0.4	0.6	tCK
Data to the 1st DQS Latching Transition	tDQSS	0.75	1.25	tCK
DQS Write Preamble	tWPRE	1.5		tCK
DQS Write Postamble	tWPST	1.5		tCK
W/R# Low To Data Input Cycle	tWRCK	20.0		ns
W/R# Low to DQS/DQ Driven by Flash Memory	tDQSD	0	18.0	ns
Access Window of DQ[7:0] from CLK	tAC	3.0	20.0	ns
Access Window of DQS from CLK	tDQSCK		20.0	ns
DQS-DQ Skew, DQS to Last DQ Valid, Per Access	tDQSQ		0.85	ns
DQ-DQS Hold, DQS to The 1st DQ to Go No-valid	tQH	0.33		tCK
DQ Input Data Valid Window	tDVW	0.24		tCK

Figure 7: NV-DDR Command Cycle Timing

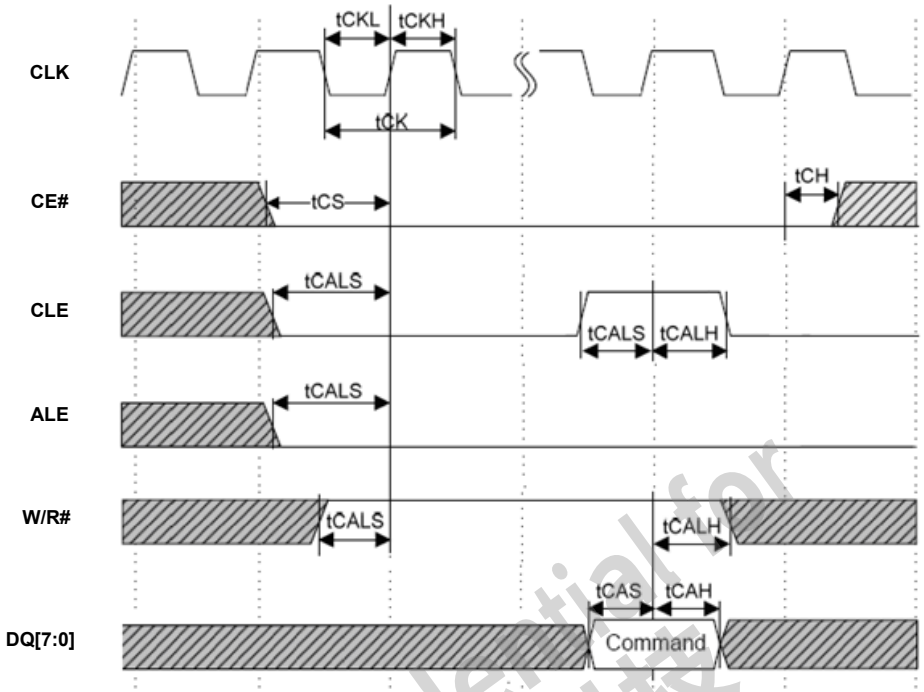


Figure 8: NV-DDR Address Cycle Timing

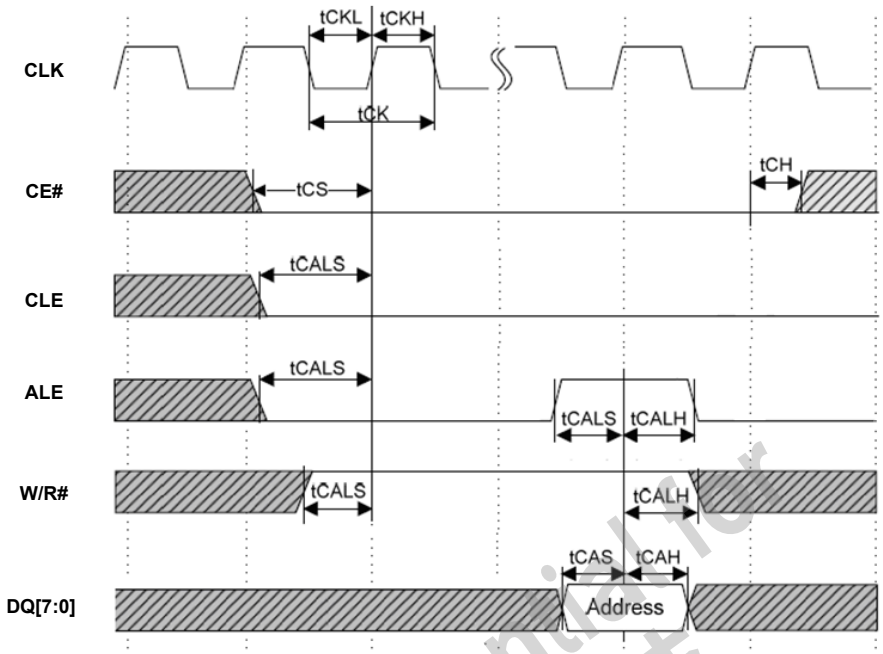


Figure 9: NV-DDR Data Output (Write) Cycle Timing

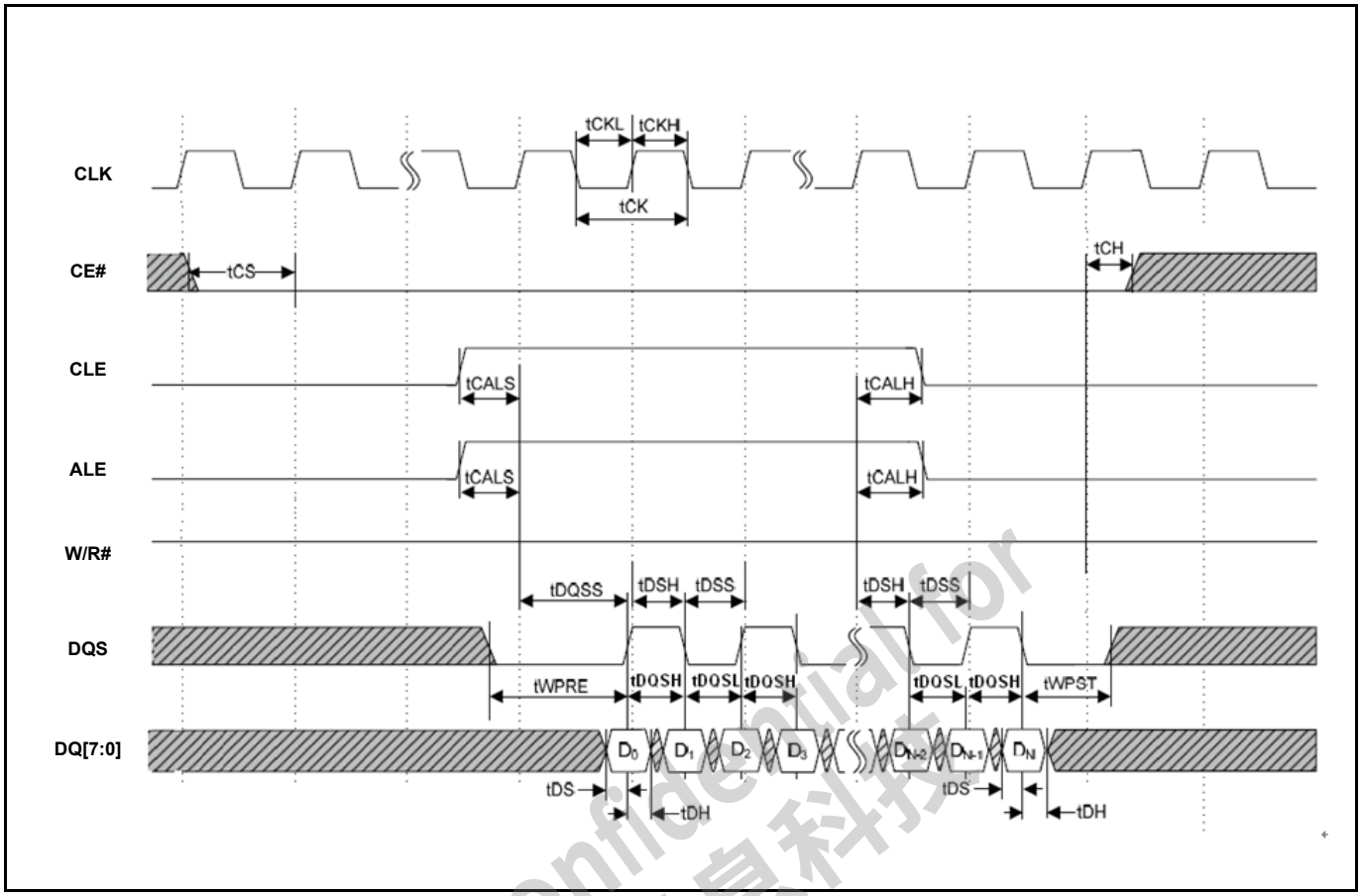
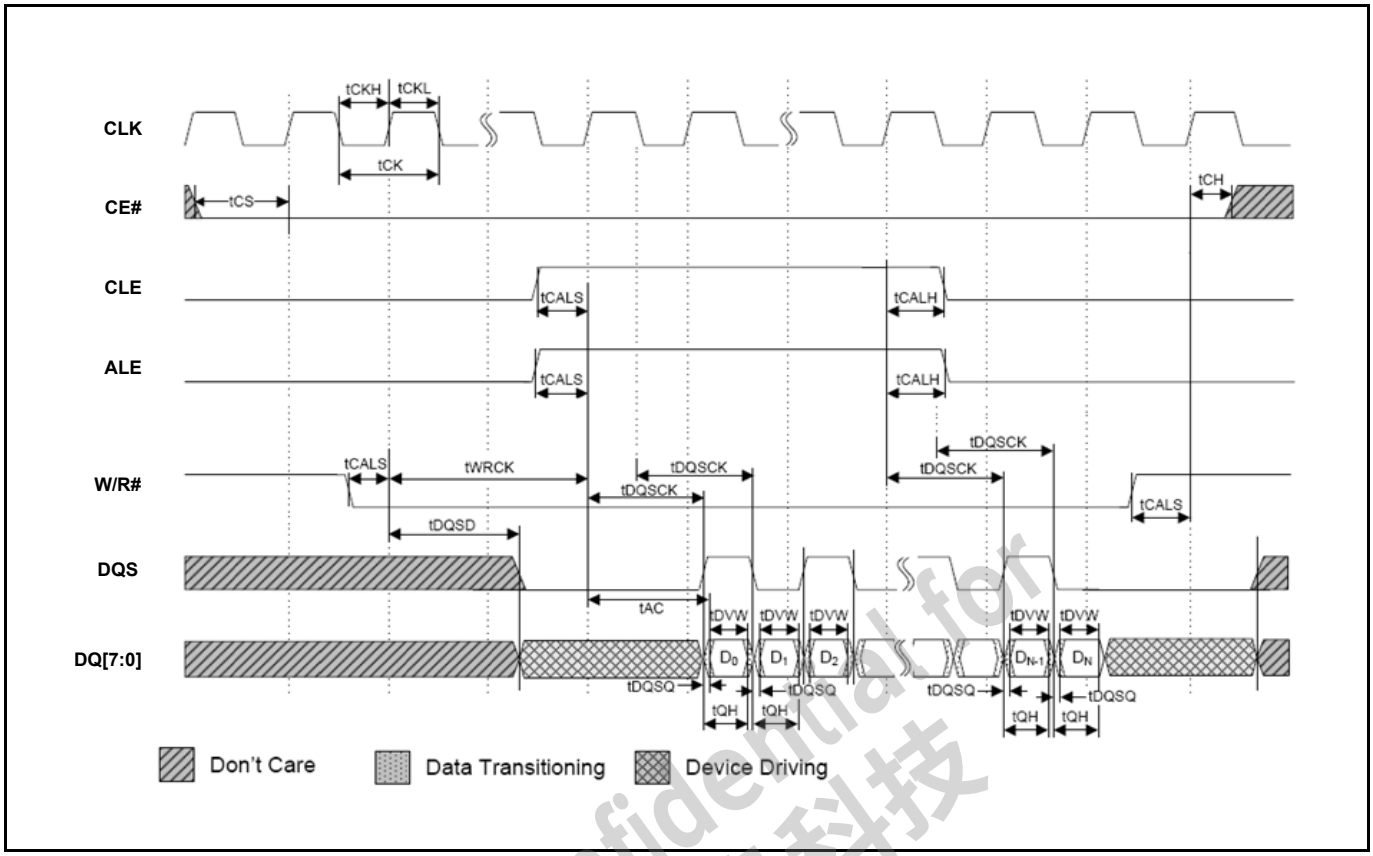


Figure 10: NV-DDR Data Input (Read) Cycle Timing



4. Software Interface

4.1 Command Set

Table 17: Command Set

Command	Code	Protocol
General Feature Set		
Execute Device Diagnostic	90h	Execute device diagnostic
Flush Cache	E7h	Non-data
Identify Device	ECh	PIO data-in
Initialize Drive Parameters	91h	Non-data
Read DMA	C8h	DMA
Read Log Ext	2Fh	PIO data-in
Read Multiple	C4h	PIO data-in
Read Sector(s)	20h	PIO data-in
Read Verify Sector(s)	40h or 41h	Non-data
Set Feature	EFh	Non-data
Set Multiple Mode	C6h	Non-data
Write DMA	CAh	DMA
Write Multiple	C5h	PIO data-out
Write Sector(s)	30h	PIO data-out
NOP	00h	Non-data
Read Buffer	E4h	PIO data-in
Write Buffer	E8h	PIO data-out
Power Management Feature Set		
Check Power Mode	E5h or 98h	Non-data
Idle	E3h or 97h	Non-data
Idle Immediate	E1h or 95h	Non-data
Sleep	E6h or 99h	Non-data
Standby	E2h or 96h	Non-data
Standby Immediate	E0h or 94h	Non-data
Security Mode Feature Set		
Security Set Password	F1h	PIO data-out
Security Unlock	F2h	PIO data-out
Security Erase Prepare	F3h	Non-data
Security Erase Unit	F4h	PIO data-out
Security Freeze Lock	F5h	Non-data
Security Disable Password	F6h	PIO data-out

Command	Code	Protocol
SMART Feature Set		
SMART Disable Operations	B0h	Non-data
SMART Enable/Disable Autosave	B0h	Non-data
SMART Enable Operations	B0h	Non-data
SMART Execute OFF-LINE Immediate	B0h	Non-data
SMART Read Log	B0h	PIO data-in
SMART Read Data	B0h	PIO data-in
SMART Read Threshold	B0h	PIO data-in
SMART Return Status	B0h	Non-data
SMART Save Attribute Values	B0h	Non-data
SMART Write Log	B0h	PIO data-out
Host Protected Area Feature Set		
Read Native Max Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out
48-bit Address Feature Set		
Flush Cache Ext	EAh	Non-data
Read Sector(s) Ext	24h	PIO data-in
Read DMA Ext	25h	DMA
Read Multiple Ext	29h	PIO data-in
Read Native Max Address Ext	27h	Non-data
Read Verify Sector(s) Ext	42h	Non-data
Set Max Address Ext	37h	Non-data
Write DMA Ext	35h	DMA
Write Multiple Ext	39h	PIO data-out
Write Sector(s) Ext	34h	PIO data-out
NCQ Feature Set		
Read FPDMA Queued	60h	DMA Queued
Write FPDMA Queued	61h	DMA Queued
Others		
Data Set Management	06h	DMA
Seek	70h	Non-data

4.2 Identify Device

The Identify Device command enables the host to receive parameter information from the SM2246EN. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in the following table.

Table 18: ID Table Information

Word	F / V	Default Value	Description
0	F	0040h	General configuration
1	X	XXXXh	Default number of cylinders
2	V	0000h	Reserved
3	X	00XXh	Default number of heads
4	X	0000h	Obsolete
5	X	0240h	Obsolete
6	F	XXXXh	Default number of sectors per track
7 - 8	V	XXXXh	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	X	0000h	Obsolete
10 - 19	F	XXXXh	Serial number in ASCII (Right justified)
20	X	0002h	Obsolete
21	X	0002h	Obsolete
22	X	0000h	Obsolete
23 - 26	F	XXXXh	Firmware revision in ASCII Big Endian Byte Order in Word
27 - 46	F	XXXXh	Model number in ASCII (Left justified) Big Endian Byte Order in Word
47	F	8001h	Maximum number of sectors on Read/Write Multiple command
48	F	0000h	Reserved
49	F	0F00h	Capabilities
50	F	4000h	Capabilities
51	F	0200h	PIO data transfer cycle timing mode
52	X	0000h	Obsolete
53	F	0007h	Field validity
54	X	XXXXh	Current numbers of cylinders
55	X	XXXXh	Current numbers of heads
56	X	XXXXh	Current sectors per track
57 - 58	X	XXXXh	Current capacity in sectors (LBAs) (Word 57 = LSW , Word 58 = MSW)
59	F	0101h	Multiple sector setting
60 - 61	F	XXXXh	Total number of user addressable logical sectors for 28-bit commands (DWord)

Word	F / V	Default Value	Description
62	X	0000h	Reserved
63	F	0207h	Multiword DMA transfer Supports MDMA mode 0, 1 and 2
64	F	0003h	Advanced PIO modes supported
65	F	0078h	Minimum Multiword DMA transfer cycle time per word
66	F	0078h	Recommended Multiword DMA transfer cycle time
67	F	0078h	Minimum PIO transfer cycle time without flow control
68	F	0078h	Minimum PIO transfer cycle time with lORDY flow control
69	F	4000h	Additional supported
70 - 74	F	0000h	Reserved
75	F	001Fh	Queue depth
76	F	070Eh	Serial ATA capabilities • Supports Serial ATA Gen3 • Supports Serial ATA Gen2 • Supports Serial ATA Gen1 • Supports Phy event counters log • Supports receipt of host initiated power management requests • Supports Native Command Queuing
77	F	0080h	Serial ATA additional capability • DevSleep_to_ReducedPwerState
78	F	0148h	Serial ATA features supported • Supports Device Sleep • Supports software settings preservation • Device supports initiating power management
79	V	0040h	Reserved
80	F	03F0h	Major version number (ACS-2)
81	F	0000h	Minor version number
82	F	742Bh	Command sets supported 0
83	F	7500h	Command sets supported 1
84	F	4023h	Command sets supported 2
85 - 87	V	XXXXh	Command set/feature enabled
88	V	007Fh	Ultra DMA mode supported and selected
89	F	0003h	Time required for a Normal Erase mode Security Erase Unit command
90	F	0001h	Time required for an Enhanced Erase mode Security Erase Unit command
91	V	0000h	Current advanced power management value
92	V	FFFEh	Master password identifier
93 - 99	V	0000h	Reserved
100 - 103	V	XXXXh	Maximum user LBA for 48-bit address feature set
104	V	0000h	Reserved
105	F	0100h	Maximum number of 512-byte blocks per Data Set Management command

Word	F / V	Default Value	Description
106 - 127	V	0000h	Reserved
128	V	0001h	Security status
129 - 159	X	XXXXh	Vendor specific
160	F	0000h	Power requirement description
161	X	0000h	Reserved
162	F	0000h	Key management schemes supported
163	F	0000h	CF Advanced True IDE Timing mode capability and setting
164 - 168	V	0000h	Reserved
169	F	0001h	Data Set Management supported
170 - 216	V	XXXXh	Reserved
217	F	0001h	Non-rotating media (SSD)
218 - 221	X	0000h	Reserved
222	F	107Fh	Transport major revision (SATA Rev 3.1)
223 - 254	X	0000h	Reserved
255	X	XXXXh	Integrity word

Notes:

1. F = content (byte) is fixed and does not change.
2. V = content (byte) is variable and may change depending on the state of the device or the commands executed by the device.
3. X = content (byte) is vendor specific and may be fixed or variable.

4.3 SMART Feature Set

The SM2246EN supports the SMART command set and defines some vendor-specific data to report spare/bad block numbers in each memory management unit.

Table 19: SMART Feature Register Values

Value	Command	Value	Command
D0h	Read Data	D5h	Read Log
D1h	Read Attribute Threshold	D6h	Write Log
D2h	Enable/Disable Autosave	D8h	Enable SMART Operations
D3h	Save Attribute Values	D9h	Disable SMART Operations
D4h	Execute OFF-LINE Immediate	DAh	Return Status

If the reserved size is below the threshold, the status can be read from the Cylinder Register using the Return Status command (DAh).

4.3.1 SMART Data Structure

The following 512 bytes make up the device SMART data structure. Users can obtain the data using the "Read Data" command (D0h).

Table 20: SMART Data Structure

Byte	F / V	Description
0 - 1	X	Revision code
2 - 361	X	Vendor specific (see 4.3.2)
362	V	Off-line data collection status
363	X	Self-test execution status byte
364 - 365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368 - 369	F	SMART capability
370	F	Error logging capability • 7-1 Reserved • 0 1 = Device error logging supported
371	X	Vendor specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375 - 385	R	Reserved
386 - 395	F	Firmware version/date code
396 - 399	F	Reserved
400 - 405	F	'SM2246'
406 - 510	X	Vendor specific
511	V	Data structure checksum

Notes:

1. F = content (byte) is fixed and does not change.
2. V = content (byte) is variable and may change depending on the state of the device or the commands executed by the device.
3. X = content (byte) is vendor specific and may be fixed or variable.
4. R = content (byte) is reserved and shall be zero.

4.3.2 SMART Attributes

The following table defines the vendor specific data in byte 2 to 361 of the 512-byte SMART data.

Table 21: SMART Data Vendor-specific Attributes

Attribute ID (hex)	Raw Attribute Value							Attribute Name
01	MSB	00	00	00	00	00	00	Read error rate
05	LSB	MSB	00	00	00	00	00	Reallocated sectors count
09	LSB			MSB	00	00	00	Power-on hours
0C	LSB			MSB	00	00	00	Power cycle count
A0	LSB			MSB	00	00	00	Uncorrectable sector count when read/write
A1	LSB	MSB	00	00	00	00	00	Number of valid spare block
A3	LSB	MSB	00	00	00	00	00	Number of initial invalid block
A4	LSB			MSB	00	00	00	Total erase count
A5	LSB			MSB	00	00	00	Maximum erase count
A6	LSB			MSB	00	00	00	Minimum erase count
A7	LSB			MSB	00	00	00	Average erase count
A8	LSB			MSB	00	00	00	Max erase count of spec
A9	LSB			MSB	00	00	00	Remain Life (percentage)
AF	LSB			MSB	00	00	00	Program fail count in worst die
B0	LSB	MSB	00	00	00	00	00	Erase fail count in worst die
B1	LSB			MSB	00	00	00	Total wearlevel count
B2	LSB	MSB	00	00	00	00	00	Runtime invalid block count
B5	LSB			MSB	00	00	00	Total program fail count
B6	LSB	MSB	00	00	00	00	00	Total erase fail count
BB	LSB			MSB	00	00	00	Uncorrectable error count
C0	LSB	MSB	00	00	00	00	00	Power-off retract count
C2	MSB	00	00	00	00	00	00	Controlled temperature
C3	LSB			MSB	00	00	00	Hardware ECC recovered
C4	LSB			MSB	00	00	00	Reallocation event count
C6	LSB			MSB	00	00	00	Uncorrectable error count off-line
C7	LSB	MSB	00	00	00	00	00	UltraDMA CRC error count
E1	LSB						MSB	Total LBAs written (each write unit = 32MB)
E8	LSB	MSB	00	00	00	00	00	Available reserved space
F1	LSB						MSB	Total LBAs written (each write unit = 32MB)
F2	LSB						MSB	Total LBAs read (each read unit = 32MB)

4.4 Capacity

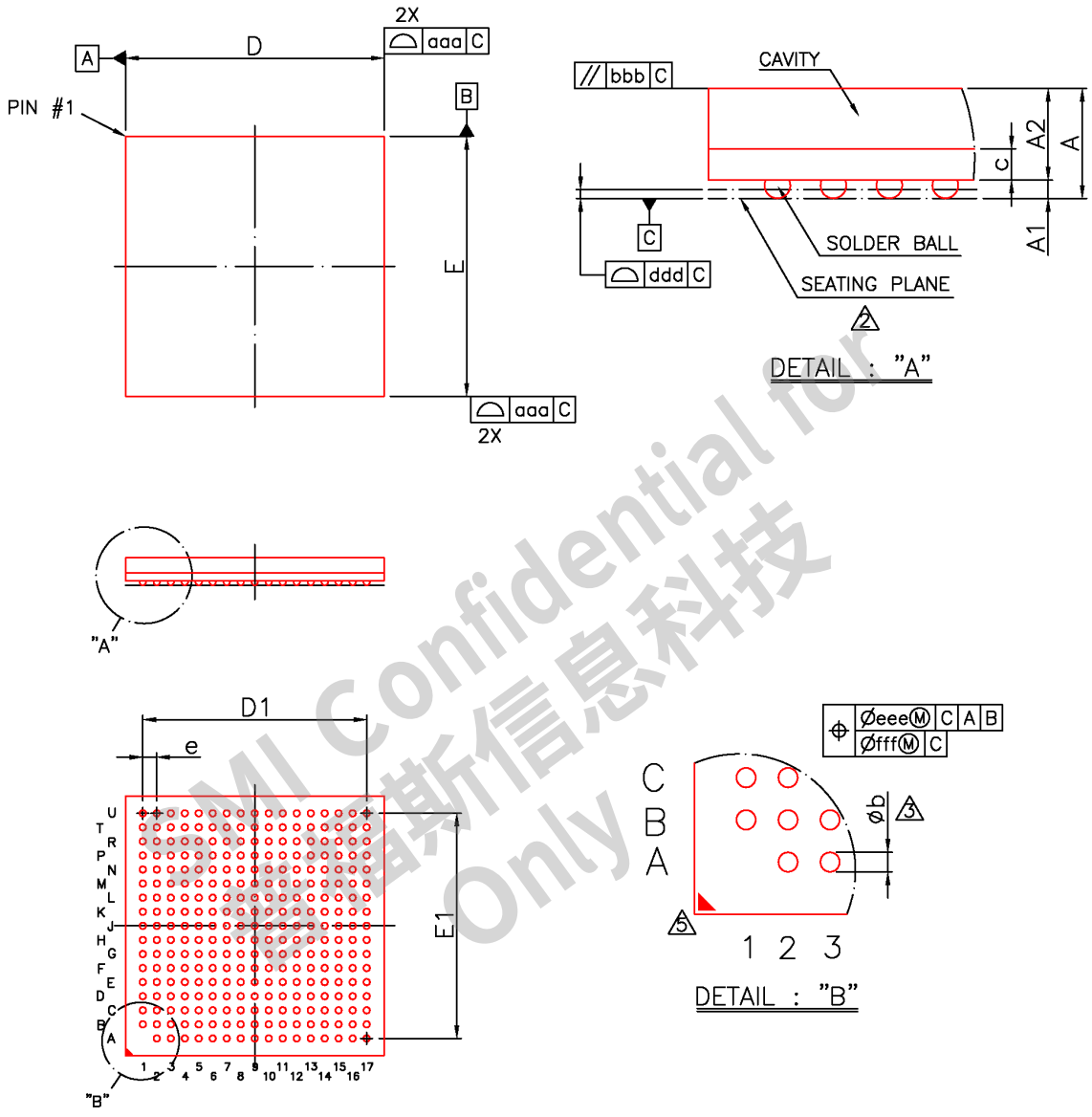
This section depicts the default storage capacity and settings for cylinders, heads, and sectors. Users can change these settings using SMI mass production software.

Table 22: Capacity Information

Capacity	Cylinders	Heads	Sectors	Total Sectors	User Data Size
32GB	16,383	15	63	61,865,984	Depended on file management
64GB	16,383	15	63	123,731,968	
128GB	16,383	15	63	247,463,936	
256GB	16,383	15	63	494,927,872	
512GB	16,383	15	63	989,855,744	
1024GB	16,383	15	63	1,979,711,488	

5. Package Information

5.1 288-Ball TFBGA Package

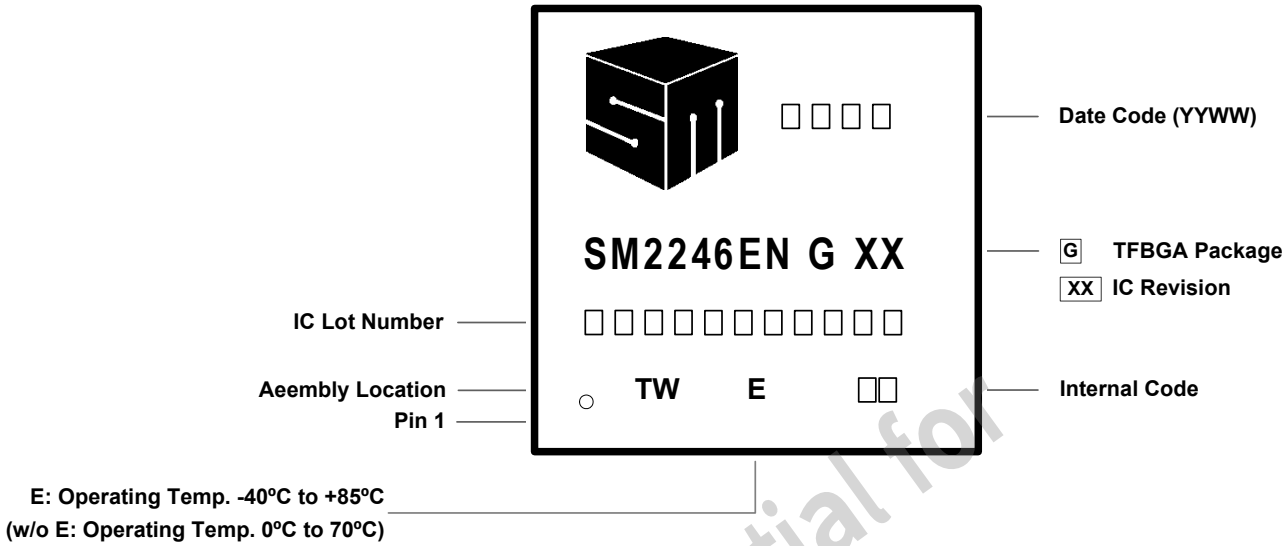


SYMBOL	MIN	NOM	MAX	SYMBOL	MIN	NOM	MAX
A	---	---	1.35	e	---	0.65	---
A1	0.16	0.21	0.25	b	0.25	0.30	0.35
A2	1.01	1.06	1.11	aaa	0.15		
c	0.32	0.36	0.40	bbb	0.10		
D	11.90	12.00	12.10	ddd	0.08		
E	11.90	12.00	12.10	eee	0.15		
D1	---	10.40	---	fff	0.08		
E1	---	10.40	---	MD/ME	17/17		

Notes:
1. Controlling Dimension: Millimeter.
2. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Special characteristics C class: bbb, ddd.
5. The pattern of Pin 1 fiducial is for reference only.

5.2 Top Marking

Figure 11: Top Marking Information



6. Product Ordering Information

Table 23: Ordering Information

Ordering Number	Operating Temperature	Package Type	Descriptions
SM224GX0600EN-XX	0°C ~ 70°C	288-ball TFBGA	12 x 12 x 1.35 (mm), 0.65 mm pitch
SM224GE0600EN-XX	-40°C ~ +85°C	288-ball TFBGA	12 x 12 x 1.35 (mm), 0.65 mm pitch

Note: The suffix “XX” denotes the IC revision.